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New Small Wheel Trigger Processor Electronics

The New Small Wheel is a detector designed for the CERN ATLAS experiment, ensuring tracking resolution and efficiency in the LHC high-luminosity era. Comprising Micromegas and small-strip Thin Gap Chamber technologies, it reduces the rate of invalid data acquisition requests in a cavern background-sensitive region. The focus of this contribution is the electronics of its trigger processor, which evaluates measurements produced by both detectors in a time budget of less than 200 ns. This achievement is made possible by an ATCA-based system featuring 7 reprogrammable devices, around 160 multi-gigabit links, and a highly flexible clocking scheme.

Summary (500 words)

The New Small Wheel (NSW) is a crucial detector designed for the ATLAS experiment at CERN during the high-luminosity LHC era. Operating at a luminosity of 7.5x10ˆ34 Hz/cm2 with a background rate of approximately 20 kHz/cm2, it combines small-strip Thin Gap Chambers (sTGC) and resistive strip Micromegas (MM) technologies, boasting an impressive total of 2.45 million electrodes.
Its primary function is to reject spurious readings by aligning detected hits with trajectory segments originating from the interaction point. Situated in the end-cap region, the NSW is divided into 16 sectors arranged in a circular pattern, covering the full azimuthal angle range. This division is essential for the detector's design as it facilitates the distribution of data processing. In this specific context, the NSW trigger processor (TP) emerges as a key component, responsible for evaluating measurements from both sTGC and MM technologies. Operating within a stringent time constraint of under 200 ns, the TP identifies trigger candidates for further analysis. This contribution provides a comprehensive description of the NSW TP electronics, which are designed in accordance with the Advanced Telecom and Computing Architecture (ATCA) standard. This design choice ensures a robust and scalable platform for efficient data processing. Composed of a carrier board, two mezzanine cards, and a rear transition module (RTM), the TP electronics encompass several essential functionalities, including electronic infrastructure, control and data paths, and debugging resources. To receive and process data from a sector, each mezzanine board houses a pair of Field Programmable Gate Array (FPGA) devices. These devices are interconnected, enabling efficient data exchange and synchronization. This real-time processing and coordination is crucial for the NSW's operation. Additionally, the carrier board, apart from being part of the data path through FPGA devices, provides electronic infrastructure and control paths via a System on a Module (SoM). Acting as an interface between the TP and the back- end components of the NSW chain, the RTM offers the necessary connections and interfaces for data transmission, control signals, and synchronization. To ensure reliable operation, the TP electronics implement redundancy and recovery mechanisms. Spare optical links serve as backup communication channels in the
event of link failures, while additional boot memories allow for recovery and reconfiguration of the TP in case of unexpected events. Furthermore, the TP design incorporates redundant configuration and debug paths to mitigate the impact of potential failures, ensuring smooth operation of the NSW TP. A notable aspect of the TP electronics is the implementation of a highly flexible and intricate clocking scheme, which guarantees precise synchronization of the various components within the TP, facilitating efficient data processing. It includes zero-delay jitter cleaners to eliminate timing inconsistencies, multiple clock domains to handle different data processing tasks, and transceiver reference clocks to maintain reliable data transmission and synchronization. By delving into these details, this contribution highlights how the NSW TP electronics effectively supports the imposed requirements, ensuring efficient data processing, precise synchronization, and reliable operation.

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