



Universidad de Oviedo



Firmware implementation of Phase-2 Overlap Muon Track Finder algorithm for CMS Level-1 trigger

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CMS Overlap Muon Track Finder (OMTF)

- OMTF is one of the subsystems of the CMS L1 Trigger, it was introduced for the Phase-1 CMS upgrade in 2016.
- It covers the pseudorapidity region of 0.83 < |η| < 1.24
- Each processing board will cover 120 degrees of detector in r-φ plane with 30 degrees of overlap (6 boards in total)
- It utilizes three types of detectors: Drift Tubes (DTs) and Resistive Plate Chambers (RPCs) from Barrel and Cathode Strip Chambers (CSCs) and RPCs from Endcap region.
- OMTF identifies the muon tracks, estimates their transverse momentum and sends the found candidates (with associated chamber segments) to the Global Muon Trigger



CMS detector slice for Phase-2 CMS, Source: "The Phase-2 Upgrade of the CMS Level-1 Trigger"

Muon track reconstruction in OMTF region

- The principle of the muon track reconstruction in the Phase-2 OMTF algorithm is the same as in Phase-1
- The muon track recognition algorithm was written in VHDL for Phase-1 and has been ported to C++ HLS for Phase-2
- Inputs: 18 layers of muon detection (DT, RPC and CSC)
- 8 of detector layers with good coverage in φ and η are treated as the reference layers
- The OMTF algorithm begins the muon reconstruction from a reference hit
- The reconstruction is performed using pattern matching, based on the naive Bayes classifier
- Duplicated track candidates are removed by the Ghostbuster functional block
- For Phase-2, pattern recognition algorithm introduces measurement of transverse momentum without beamspot constraint. This allows the triggering on muons coming from the decays of long-lived particles.



Source: Bluj, Michał et al. "From the Physical Model to the Electronic System - OMTF Trigger for CMS."

OMTF Algorithm: Implementation for Phase-2

- The Bunch-Crossing (BX) event rate is 40 MHz, which determines the basic operating frequency of the system
- 15 input BMT-L1 links, 65 CSC links and 12 RPCe links, where BMT-L1 links are now implemented
- Barrel Muon Trigger Layer-1 data rate: up to 8 Trigger Primitives (TPs): 4 φ TPs, 4 θ TPs per BX, per link
- The input data must be converted to achieve common representation of data coming from different types of detectors.
- OMTF Processor and Neural Network (NN) clock frequency is 360 MHz
- Data output rate for Global Muon Trigger (GMT): up to 9 muon candidates per BX, which is determined by the algorithm's clock
- 18 output links to GMT
- Converters, OMTF Processor, Neural Network and Ghostbuster are implemented as IP cores using HLS



Target OMTF Algorithm diagram; Created by Pelayo Leguina, Universidad de Oviedo

NN in OMTF Algorithm for Phase-2 CMS

- Fully-Connected Neural Network is used in Phase-2 OMTF as one of functional blocks
- Estimates the $\boldsymbol{p}_{\scriptscriptstyle T}$ and charge for the muon candidate
- The NN inputs are $\Delta \phi$ versus the reference hit found by pattern logic
- 2 hidden layers: 16 neurons in hidden layer 1 and 9 neurons in hidden layer 2
- 441 multiplications in total
- Multiplication operations utilizes DSP48 blocks built in Ultrascale+ FPGAs
- Weights and activation functions implemented as look-up tables stored in BRAMs, to reduce logic cell utilization





OMTF P2 Algorithm: Implementation for Phase-2

PROCESSOR

OMTF F

RPC

- Target platform: custom ATCA boards (X2O) with AMD Ultrascale+ FPGAs (xcvu13p-fsga2577-1-e)
- Using Blobfish custom firmware interface for link • interface generation and system management
- TCL and Cmake scripts are used in algorithm integration
- The blocks marked with solid lines are fully implemented, while those marked with dashed line are partially implemented or simulated.
- Block colors: Blobfish in purple, input data converters in green OMTF Processor in yellow, NN in red

CONVERTER

RPC CONVERTER

CONVERTER

BMT

NE

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ESI

SCALE)

(OMTF

STUBS (

INPUT

@25Gbps

@25Gbps

@4.8Gbps

CSC

RPCe

ing Phase-2 superprimitives 64b

BMT

Results from Septemb	2024
Parameter	OMTF @360 MHz
LUT	6.3%
FF	5.3%
BRAM	20.5%
DSP	4.3%
Latency	118 clock cycles (~328 ns)
Worst Negative Slack	0.030 ns
Thermal Margin	~71 °C

ER

<u>SHOSTBUST</u>

INPUT STUBS

PACKER

ERIAL

OMTF

To GMT



Piotr Fokow, WUT: "Firmware implementation of Phase-2 Overlap Muon Track Finder algorithm for CMS Level-1 trigger", TWEPP 2024

NN

INPUT

Z

OMTF P2 Algorithm: Implementation challenges

Single SLR vs. dual SLR design

The link configuration overuses available GTY transceivers in a single SLR. Every SLR crossing comes with increased latency and resource utilization. We are expecting multiple SLR crossings for input link data. We conducted a test to get an answer to determine which negative effects might be associated with the SLR crossing. We observed higher latency and clock utilization.

Results from one of earlier builds. Red – OMTF processor, yellow – NN



Single SLR @240 MHz	Dual SLR @240 MHz
345983 [20.02%]	336173 [19.45%]
143556 [4.15%]	145413 [4.21%]
52589 [24.35%]	60567 [28.04%]
252 [9.38%]	252 [9.38%]
441 [3.59%]	441 [3.59%]
0	2
4.139 [0.027 ns]	4.112 [0.117 ns]
	Single SLR @240 MHz 345983 [20.02%] 143556 [4.15%] 52589 [24.35%] 252 [9.38%] 441 [3.59%] 0 441 [3.59%] 0 4.139 [0.027 ns]

Single-clock read-write dependencies

Priority Encoder is one of functions inside OMTFProcessor, which provides a position to the first unique reference hit every clock cycle. Those dependencies for algorithms working at higher frequences are constraining timing performance.



The HLS synthesis result before and after refactorization

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles) Latency(n	s) Iteration Later	ncy Inte	rval Trip Co	ount Pipe	elined	BRAM	DSP	FF	LUT
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Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	1 DSP	FF	LUT	
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Design and verification workflow



Design and verification flow for OMTF algorithm; Created by Pelayo Leguina, Universidad de Oviedo

OMTF Processor and Neural Network simulation results, compared with CMSSW outputs prove, that algorithm handles feeding data properly

OMTF Processor C simultaion

December Output has 1004 and hit and 60 and and a
Processor Output - bx: 1994, ret_nit_nr: 60, retlayer: 2
Best Restricted Stubs:
Layer: Ø - Active: 1, Phi: 935, Eta: 92, Quality: 6, DistPhi Phi: 28
Layer: 1 - Active: 1, Phi: -215, Eta: 92, Quality: 6, DistPhi Phi: -215
Layer: 2 - Active: 1, Phi: 907, Eta: 79, Quality: 6, DistPhi Phi: 0
Layer: 3 - Active: 1, Phi: -182, Eta: 79, Quality: 6, DistPhi Phi: -182
Laver: 4 - Active: 1. Phi: 883. Eta: 69. Quality: 6. DistPhi Phi: -24
Laver: 5 - Active: 1. Phi: -236 Eta: 69 Quality: 6 DistPhi Phi: -236
Layer: 10 - Active: 1 Dbi: 944 Eta: 86 Quality: 2 Distributiva 27
Layer, 10 - Active, 1, Fill, 944, Eta, 60, Quality, 2, District Fill, 57
Layer, 11 - Active, 1, Fill, 920, Eta. 01, Quality, 1, District Fill, 19
Layer: 15 - Active: 1, Phi: 905, Eta: 76, Quality: 2, Distrii Phi: -4
GP Out constrained - Valid_out: 1, best_pat_64: 9, pdrSum: 680, fired_cnt: /
GP Out Unconstrained - valid_out: 1, best_pat_64: 63, pdfSumUnconstr: 791, fired_cnt
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<pre>setStub layer="4" input="4" eta="69" phi="883" quality="6" phiDist="-24" valid="1"/></pre>
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Neural Network C simultaion

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calculated	sign: -0.75» expected sign: -0.75»	result:	passed
calculated	pT: 87.9688» expected pT: 87.9688»	result:	passed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 4.625 » expected pT: 4.625 » res	sult: pass	ed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 75.8438» expected pT: 75.8438»	result:	passed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 60.1172» expected pT: 60.1172»	result:	passed
calculated	<pre>sign: -1>expected sign: -1> result</pre>	: passed	
calculated	pT: 65.1563» expected pT: 65.1563»	result:	passed
calculated	<pre>sign: -1>expected sign: -1> result</pre>	: passed	
calculated	pT: 53.7188» expected pT: 53.7188»	result:	passed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 36.7891» expected pT: 36.7891»	result:	passed
calculated	<pre>sign: -1»expected sign: -1» result</pre>	: passed	
calculated	pT: 52.0938» expected pT: 52.0938»	result:	passed
calculated	sign: -0.4375» expected sign: -0.4	4375» resu	ılt: passed
calculated	pT: 44.5313» expected pT: 44.5313»	result:	passed
calculated	<pre>sign: -1»expected sign: -1» result</pre>	: passed	
calculated	pT: 8.47656» expected pT: 8.47656»	result:	passed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 12.5»expected pT: 12.5» result	: passed	
calculated	<pre>sign: -1»expected sign: -1» result</pre>	: passed	
calculated	pT: 10.4297» expected pT: 10.4297»	result:	passed
calculated	<pre>sign: -1»expected sign: -1» result</pre>	: passed	
calculated	pT: 10.9453» expected pT: 10.9453»	result:	passed
calculated	sign: -1»expected sign: -1» result	: passed	
calculated	pT: 9.47656» expected pT: 9.47656»	result:	passed
calculated	<pre>sign: -1»expected sign: -1» result</pre>	: passed	
calculated	pT: 9.32813 expected pT: 9.32813 area	result:	passed
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Simulation of integrated algorithm results in proper data propagation

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Conclusions

- As for now, the OMTF Processor is ported from Phase-1 and prepared for Phase-2. Neural Network and BMT-L1 input processing blocks are implemented.
- OMTF Processor has been extended to include muon displacement calculation for long-lived particle triggering.
- Neural Network is introduced to improve muon's p_T and charge calculation. Might require further optimization to reduce resource usage, as new calculations eg. beam-spot-unconstrained p_T will be implemented.
- Current design fits into one SLR. We expect to use multiple SLRs due to high input link and BRAM utilization, as well as functional blocks yet to be implemented.
- HLS verification of IP blocks is successful. Verification of integrated algorithm with small input data sampes shows, that data are propagated properly.
- The optimal algorithm's logic placement will be determined in further steps.

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Ministry of Science and Higher Education **Republic of Poland**



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OF WARSAW



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Thank you for your attention