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Firmware implementation of Phase-2 Overlap Muon Track Finder algorithm for CMS Level-1 trigger

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The Overlap Muon Track Finder (OMTF) is one of the subsystems of the CMS L1 Trigger. For the High-Luminosity Large Hadron Collider era (CMS phase-2 upgrade), a new version of the OMTF is currently under development. This upgraded version will be implemented on a custom ATCA board X2O, which houses a Xilinx UltraScale+ FPGA and 25 Gbps optical transceivers. This contribution focuses on the firmware implementation of the muon trigger algorithm and input data pre-processing, leveraging High-Level Synthesis (HLS) technique. The current design and verification results and experience in using both standard and non-standard HLS development workflow are presented.

Summary (500 words)

During the planned Long Shutdown 3, the LHC will undergo a major upgrade, resulting in higher luminosity and, thus, a higher detector occupancy and higher data rate. Major changes in CMS Level-1 trigger system architecture were proposed to assure good performance in these challenging conditions.
The Overlap Muon Track Finder (OMTF) trigger system covers the CMS detector region of the pseudorapidity $0.83<|\eta|<1.24$, and process data from 18 logic layers of the muon chambers, of three different types: DT, CSC and RPC. For the Phase-2, the X2O hardware platform with Virtex UltraScale+
FPGA is used to implement reviewed OMTF firmware. Compared to Phase-1 hardware, the available hardware resource is much greater, which enables the implementation of new types of algorithms, e.g., neural-network-based ones.
The Phase-2 OMTF triggering algorithm is an improved version of the algorithm currently working in the CMS. The algorithm detects both prompt and displaced muons (coming from decays of the long lived particles predicted by some theoretical models) candidates
The algorithm consists of two steps: pattern-recognition-based muon track-finding algorithm (improved version of the current OMTF algorithm), and the new component - regression neural network - which assures better pT and charge estimation, necessary for good performance (high efficiency and purity) of the trigger in high-luminosity conditions. The pattern logic provides inputs for the neural network by selecting segments and hits belonging to one muon track.
In Phase-2 OMTF, 6 X2O boards will be used, three for the negative side of the CMS detector and three for the positive. Each board covers 120° in phi dimension, with an overlap of 30° on one side.
Because the Phase-2 upgrade of the CMS detector changes the Level-1 trigger architecture and data protocols, the algorithm's firmware needed to be entirely reimplemented. The current firmware demonstrator uses DT primitives. GMT data-provider and CSC and RPC primitive processing are under development.
The algorithm is expected to output up to 9 muons per bunch-crossing event,

compared to 4 muons in Phase-1. Therefore, the algorithm's main clock speed is increased to 360 MHz, with input link areas working at lower frequencies. The current implementation divides the main algorithm into several modules, making the architecture more similar to the emulator's architecture of OMTF, improving its readability, and making its verification easier. The revised OMTF algorithm is implemented using the HLS technique. The implementation was verified against data from the OMTF algorithm emulator implemented in the CMS software framework (CMSSW) using Vitis and Vivado tools for simulation. The firmware is also tested in the X2O board: the test data simulating the inputs from the muon detectors are played from the buffers implemented in the firmware and introduced to the algorithm. The algorithm output (muon candidates) is captured by output buffers and compared with the candidates from the CMSSW emulator.
The contribution shows the latest results in algorithm architecture development and the firmware demonstrator. The challenges in algorithm implementation for multiple high clock frequencies are discussed. The paper also proposes an alternative development workflow.

Author: FOKOW, Piotr Andrzej (Warsaw University of Technology (PL))

Co-author: LEGUINA, Pelayo (Universidad de Oviedo (ES))

Presenter: FOKOW, Piotr Andrzej (Warsaw University of Technology (PL))

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