Generic Concept for a Phase Stable Timing Link

An FPGA Agnostic System for Achieving Picosecond-Level Phase Determinism in Timing Distribution Links for High Energy Physics Experiments

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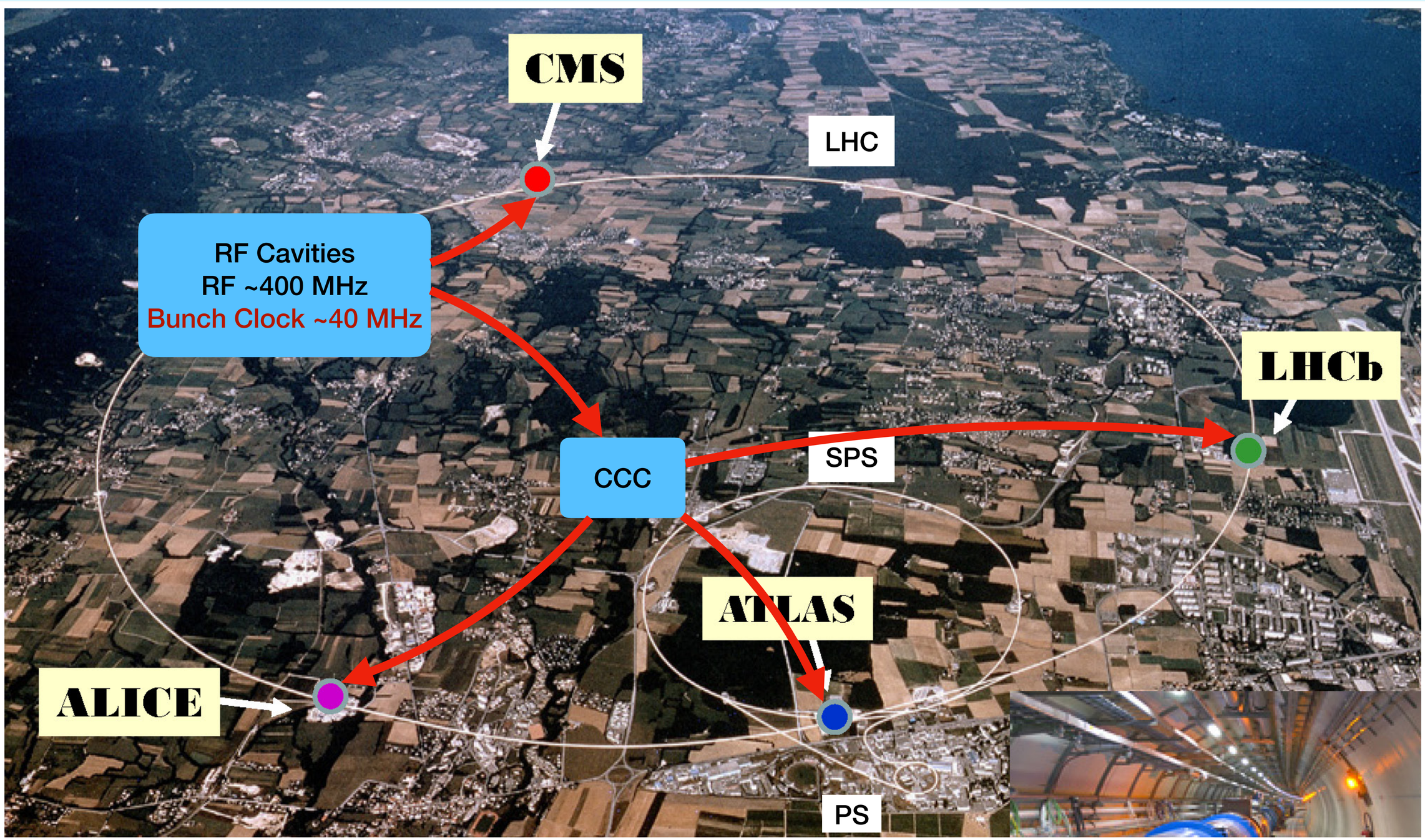
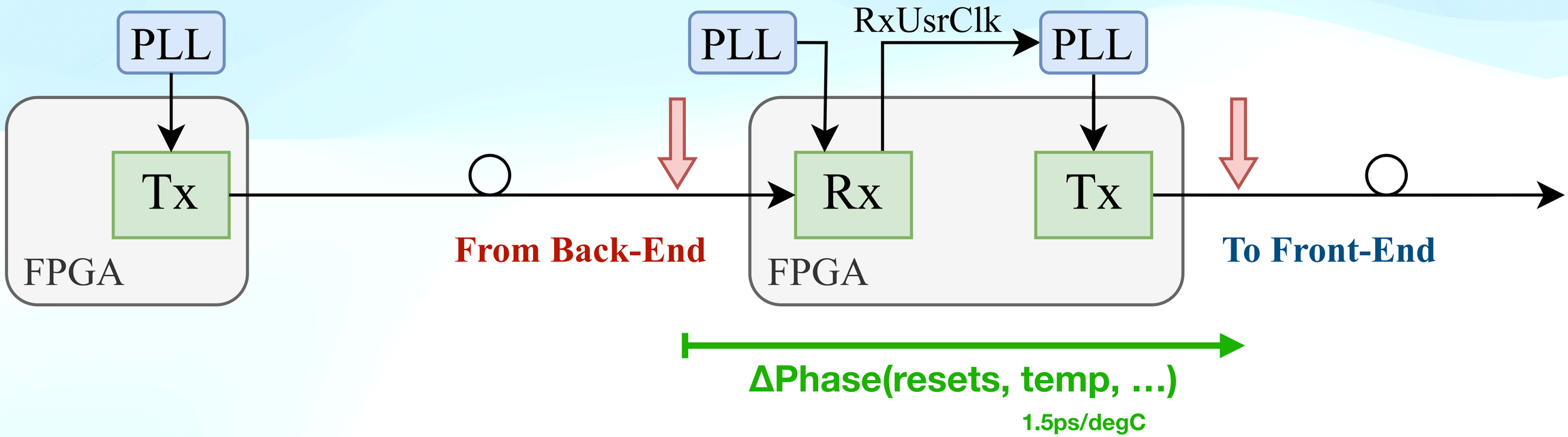
CERN EP-R&D WP6 / ECFA-DRD7 WP3.b2


CMS
LHC
RF Cavities
RF ~400 MHz
Bunch Clock ~40 MHz
LHCb
CCC
SPS
ATLAS
ALICE
PS

Cascade Timing Link

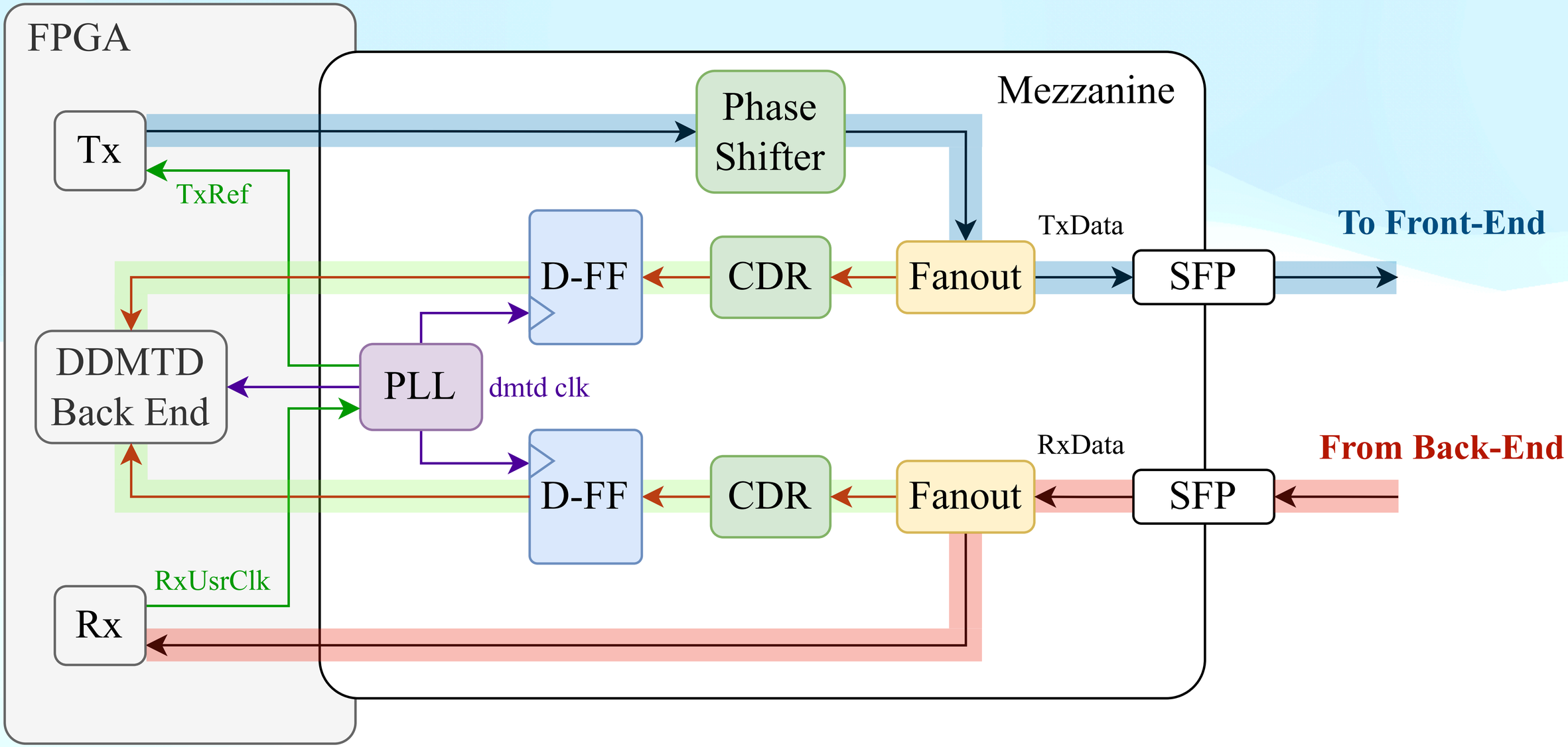
How to compensate for **phase drifts** occurring in a node (FPGA) of the cascade?

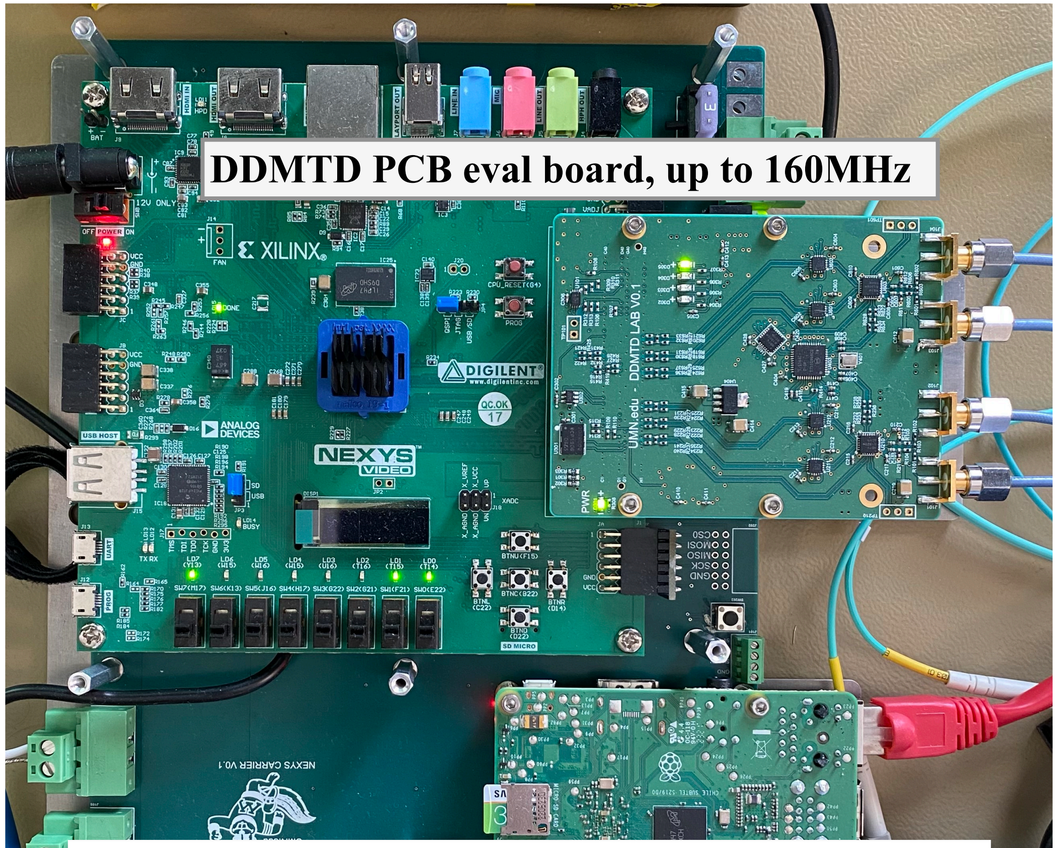
Problem: Phase drifts occur in the FPGA due to PVT variations and resets

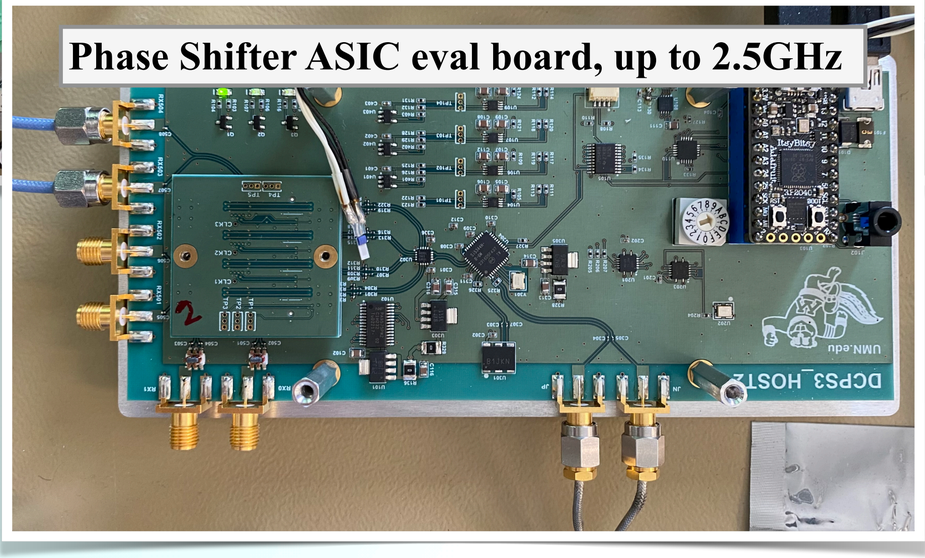


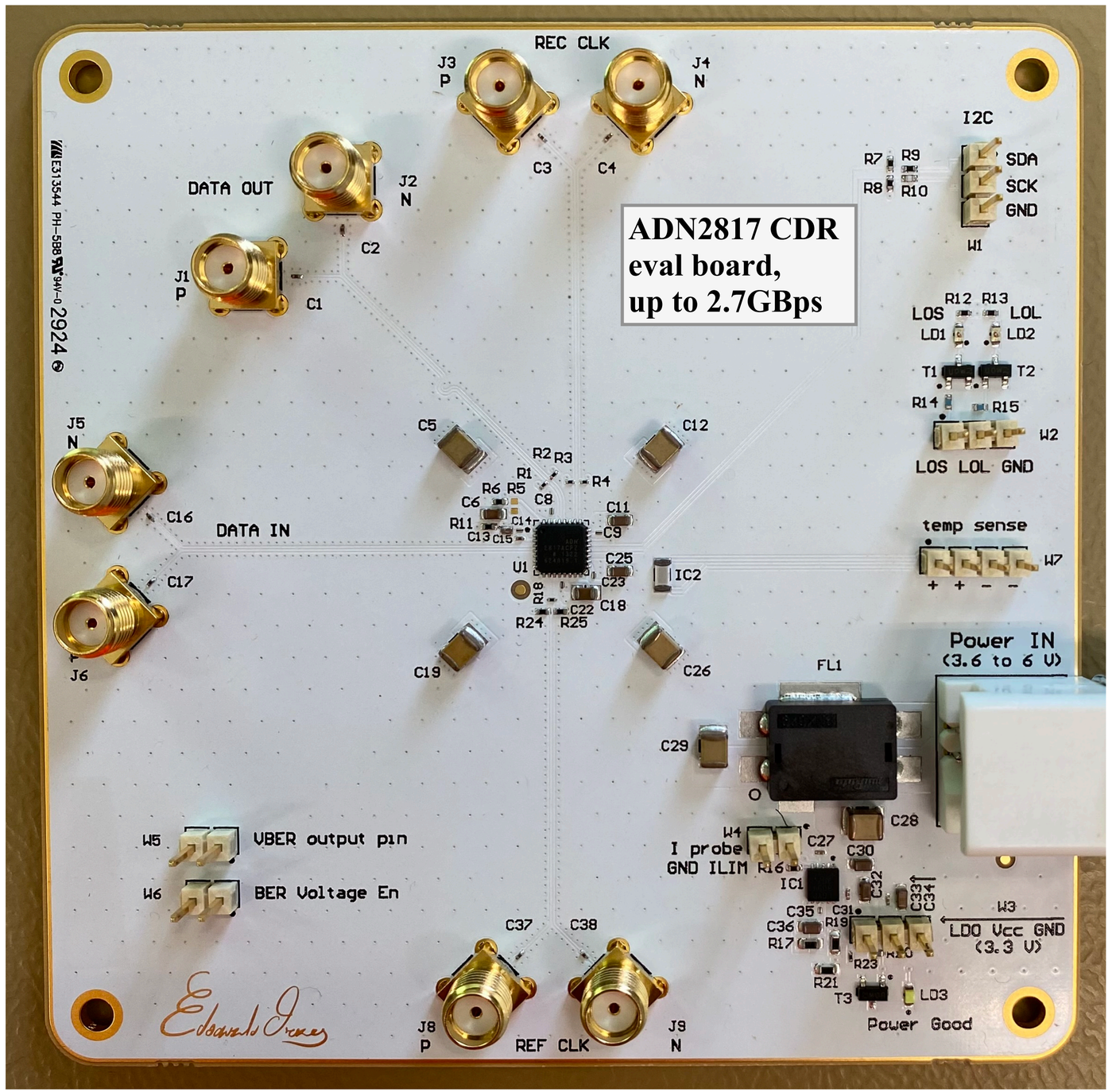
Solution: detect and correct for phase drifts with a phase detector and shifter external to the FPGA

Concept for a Generic Phase Compensation System




DDMTD PCB eval board, up to 160MHz
XILINX
DIGILENT
NEXYS VIDEO
ANALOG DEVICES
UMN.edu - DDMTD_LAB V0.1
NEXYS CARRIER V0.1


Phase Shifter ASIC eval board, up to 2.5GHz
DCPS3_HOST2
UMN.edu


ADN2817 CDR eval board, up to 2.7GBps
REC CLK
J3 P
J4 N
C3
C4
DATA OUT
J2 N
C2
J1 P
C1
I2C
R7 R9
R8 R10
SDA
SCK
GND
W1
R12 R13
LOS LOL
LD1 LD2
T1 T2
R14 R15
W2
LOS LOL GND
J5 N
C16
DATA IN
C17
J6
C5
C12
R2 R3
R1 R4
R6 R5
C6 C8
C11
R11 C14
C13 C15
C9
U1
C25
C23
IC2
R18
C22
C18
R24 R25
C19
C26
temp sense
W7
+ + - -
Power IN
(3.6 to 6 V)
FL1
C29
C28
W4
I probe
GND ILIM R16
C27
C30
IC1
C32
C33
C34
C35 C31
C36 R19
R17
W3
LDO Vcc GND
(3.3 V)
R23
R21
T3
LD3
Power Good
W5
VBER output pin
W6
BER Voltage En
C37
C38
J8 P
REF CLK
J9 N
E313544 PH-5BB 94V-0 2924

FPGA DDMTD Vs PCB DDMTD Comparison @160MHz

1. Linearity test:

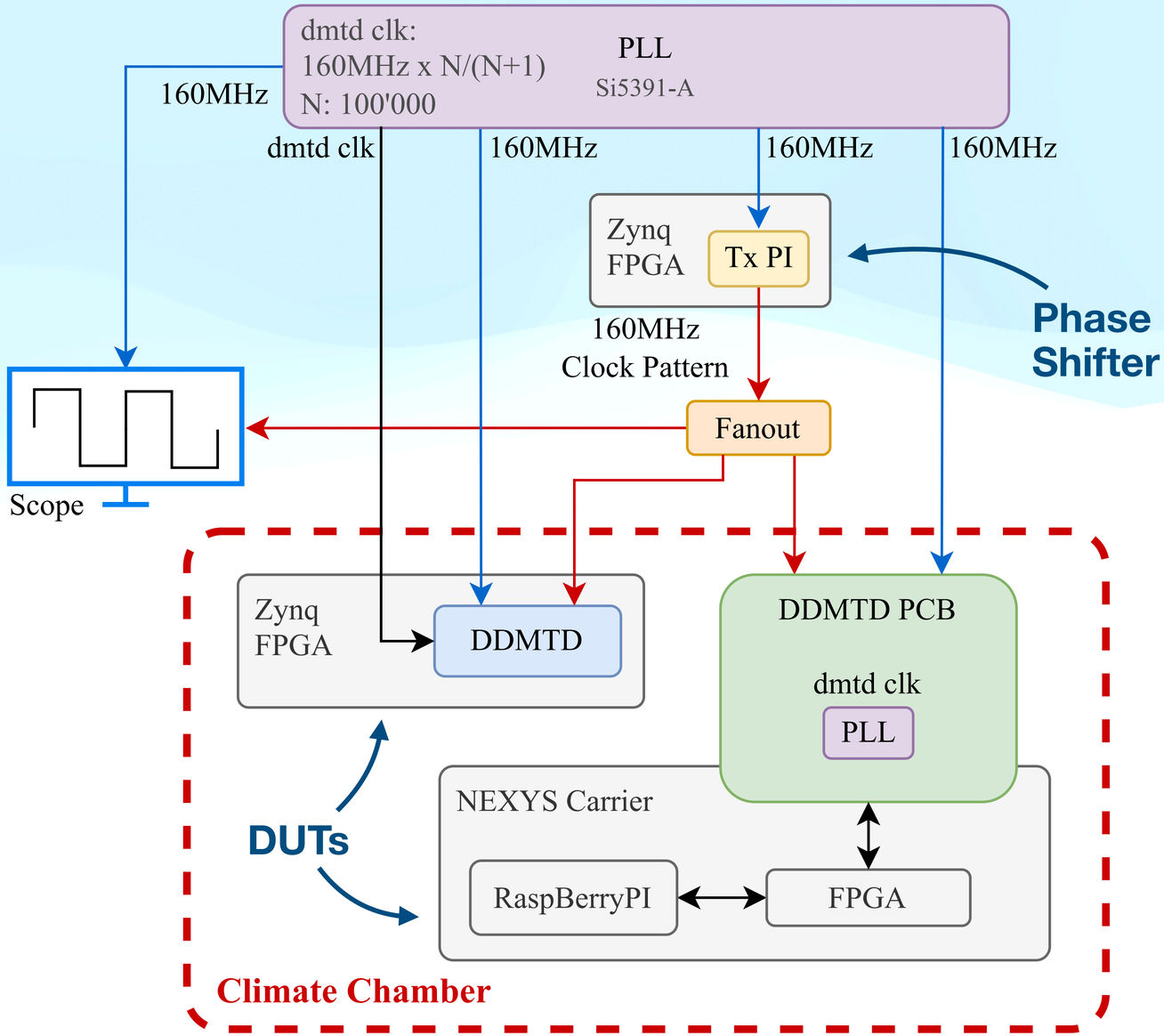
Compare phase measurements of a DDMTD fully embedded in an FPGA Vs a DDMTD with the front-end in a dedicated PCB.

Oscilloscope is the reference.

1023 phase shifts of 6.1ps covering the full clock period.

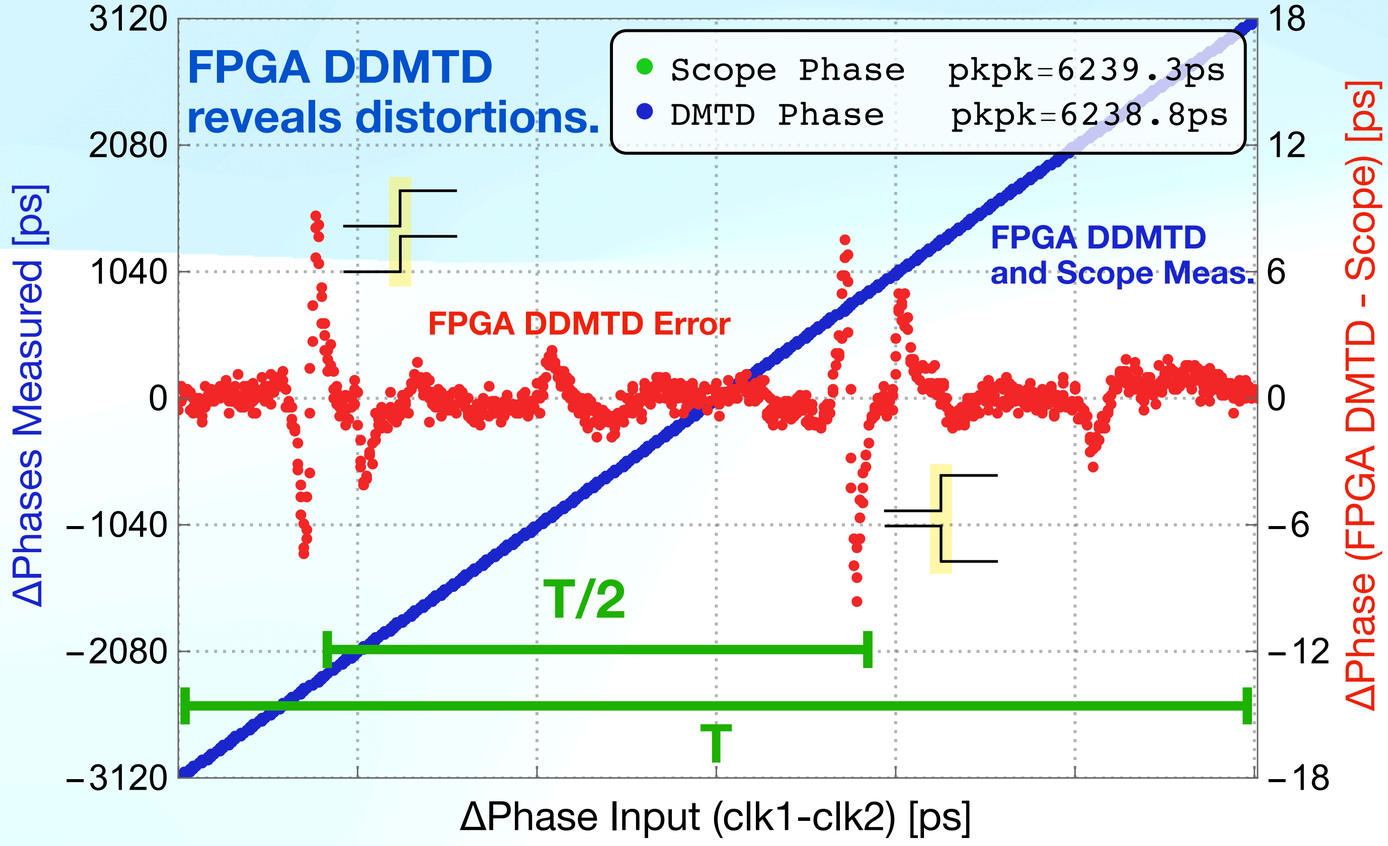
2. Temperature test:

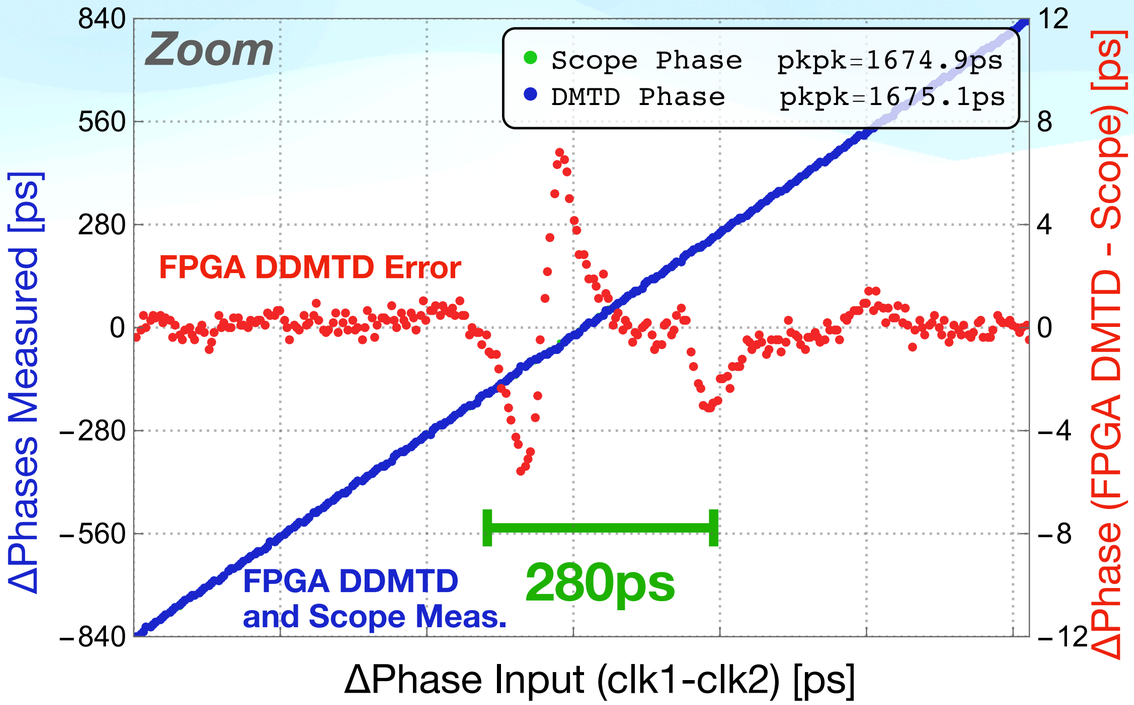
Compare the two DDMTDs measurements at a constant phase, varying temperature.



FPGA DDMTD Vs PCB DDMTD - Crosstalk @160MHz

Based on the routing, if one DDMTD input clock travels close to an aggressor clock of the same (or multiple) frequency and **the two clocks are in phase or in phase opposition**, **crosstalk** can cause a deterministic edge distortion.

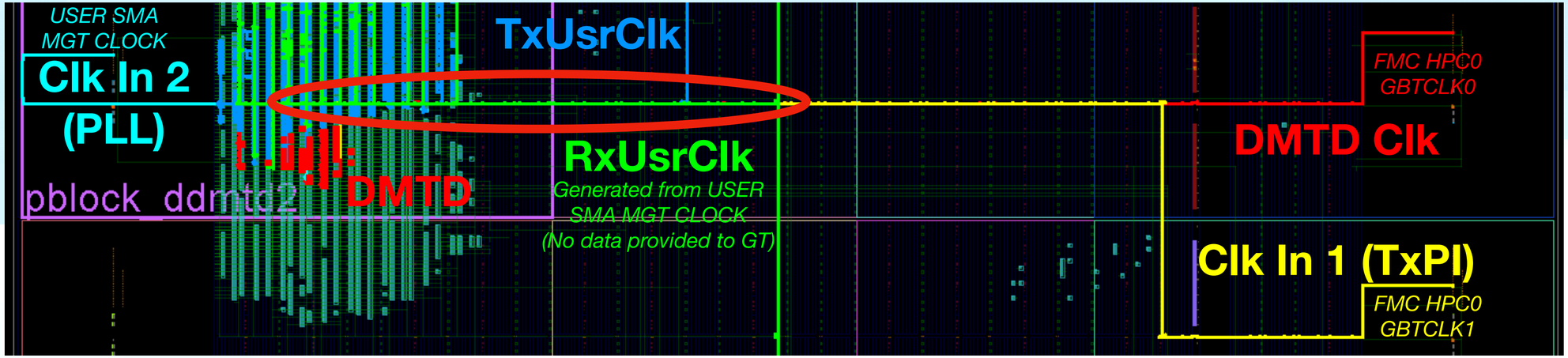


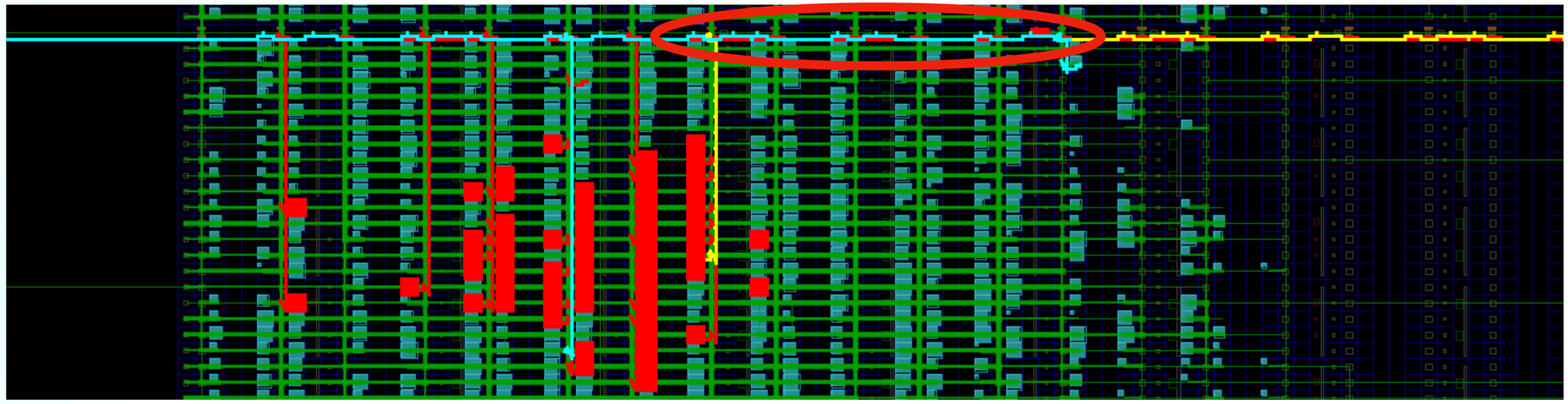


The phase measured by the PCB DDMTD does not reveal any distortions.

FPGA DDMTD Channels Routing - Crosstalk

Several linearity tests have been done changing the clock input ports and DDMTD placement. Whenever a clock is routed close to another, two phase distortions are observed with T/2 one from the other (on the clock edges).





FPGA DDMTD Channels Routing - Crosstalk

Possible solutions (tested):

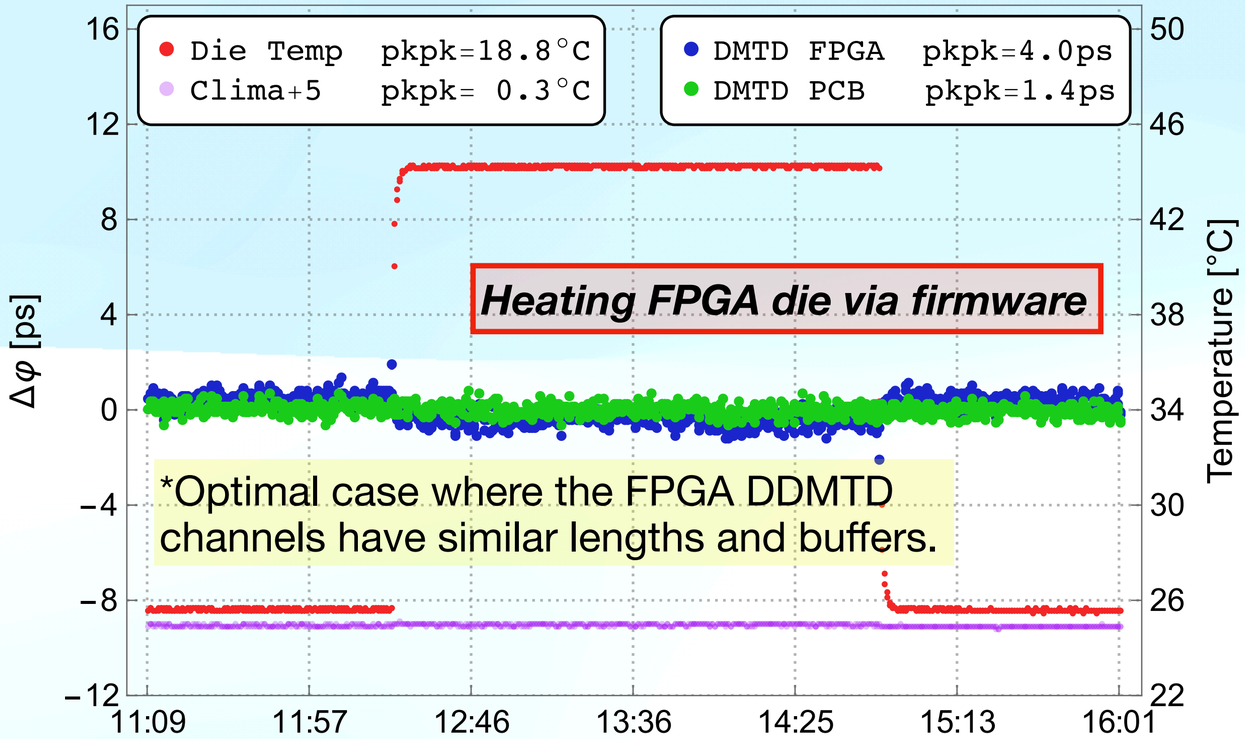
- Place the DDMTD in a PBlock aiming for a better routing, then check the implementation to see if the two inputs are routed far from other clocks.
- Place the two DDMTD sampler flip-flops on the input ports logic (IOB), to avoid further routing into the FPGA (not possible when using the GT Ref inputs).
- It is not guaranteed that for every implementation it is possible to obtain a routing which avoids non linearities in the FPGA.

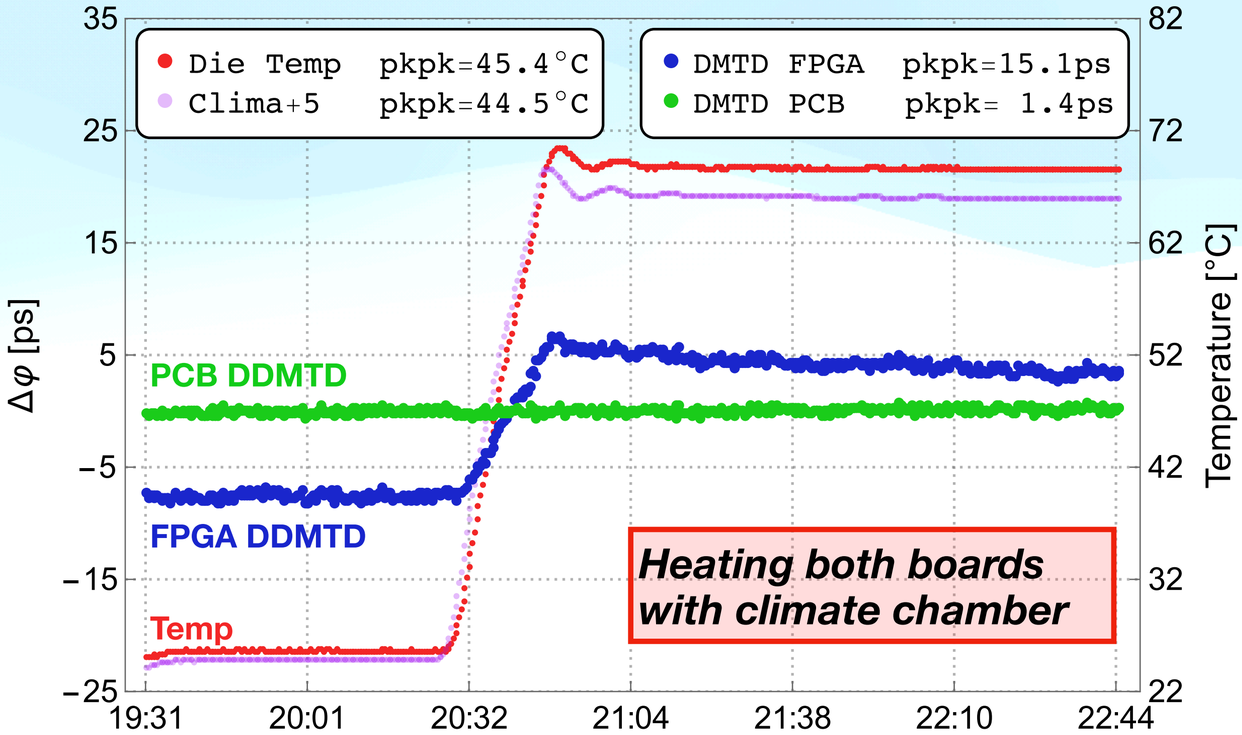
Routing clocks at a distance

FPGA DDMTD Vs PCB DDMTD - Temp Stability @160MHz

FPGA: 0 to 1 ps/degC Discrete: 0 ps/degC *[SMA Cable: 0.7 ps/(m degC)]*

*Depends on routing





The symmetric implementation of the PCB DDMTD makes it insensitive to temperature

Symmetrical routing

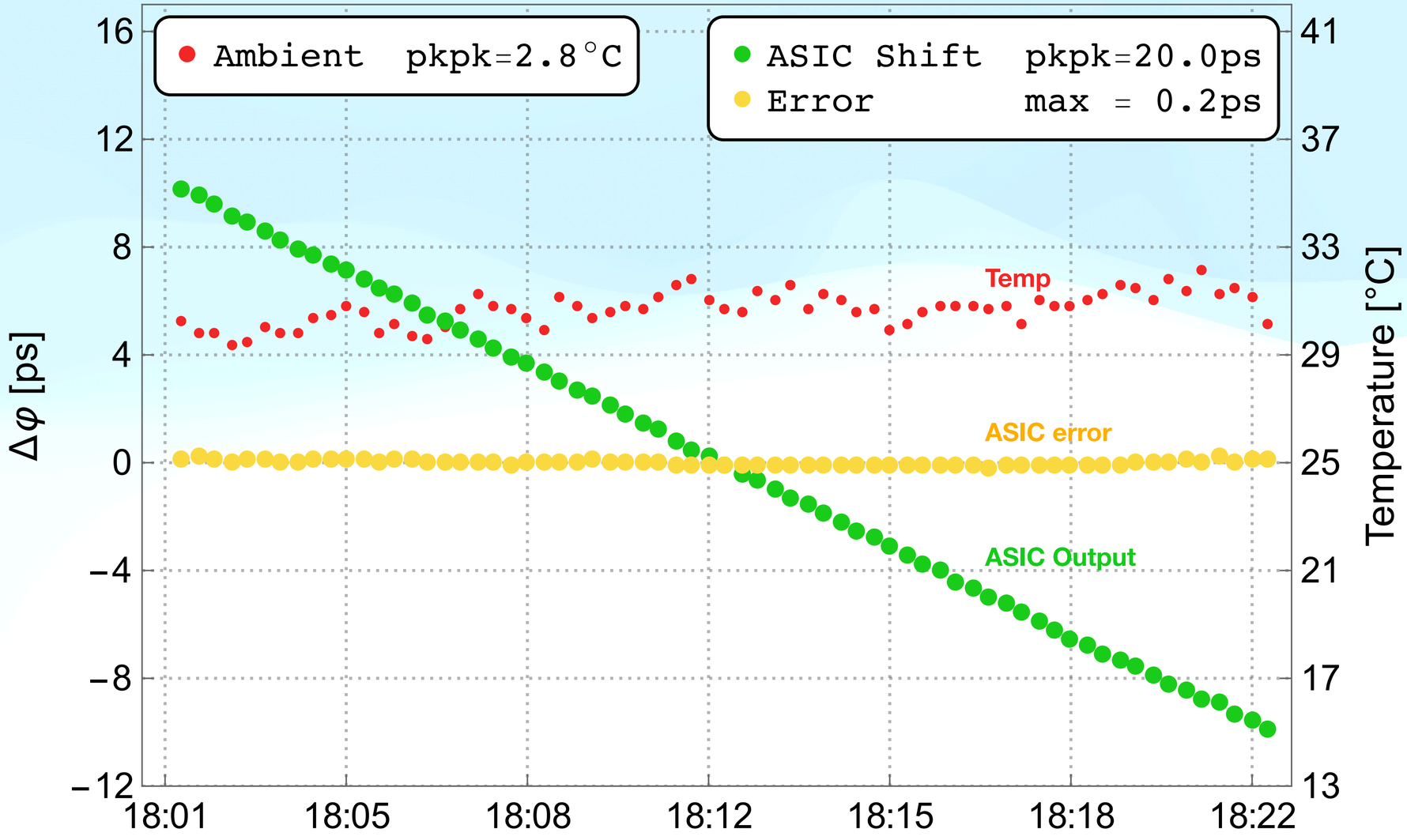
Phase Shifter ASIC Characterization @160MHz

Step of ~335fs

Range of 20ps

Stability of <0.1ps RMS

Test in climate chamber reported no temperature dependency



Phase Shifter is OK

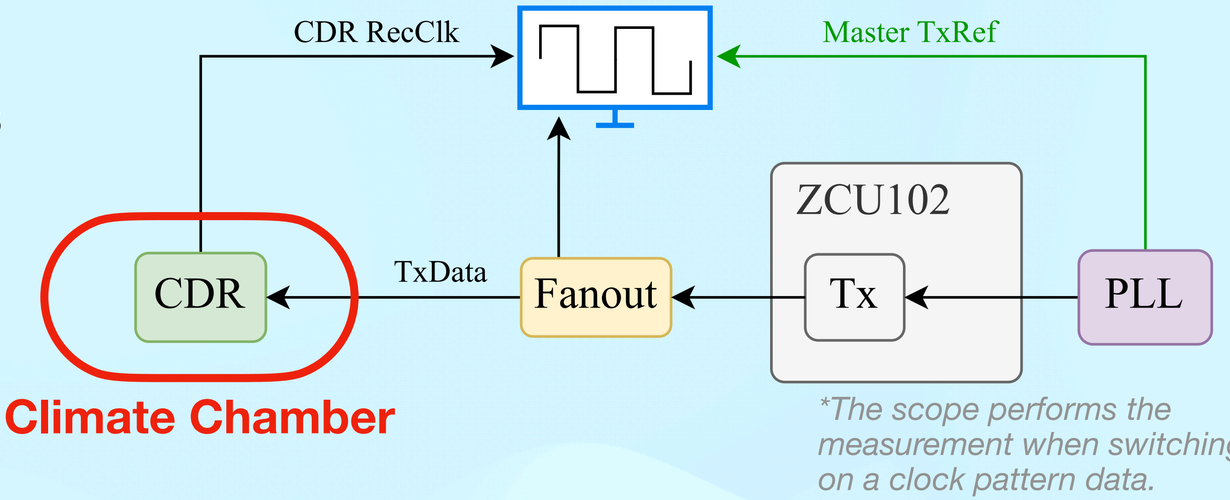
CDR Characterization @2.4Gbps

ADN2817

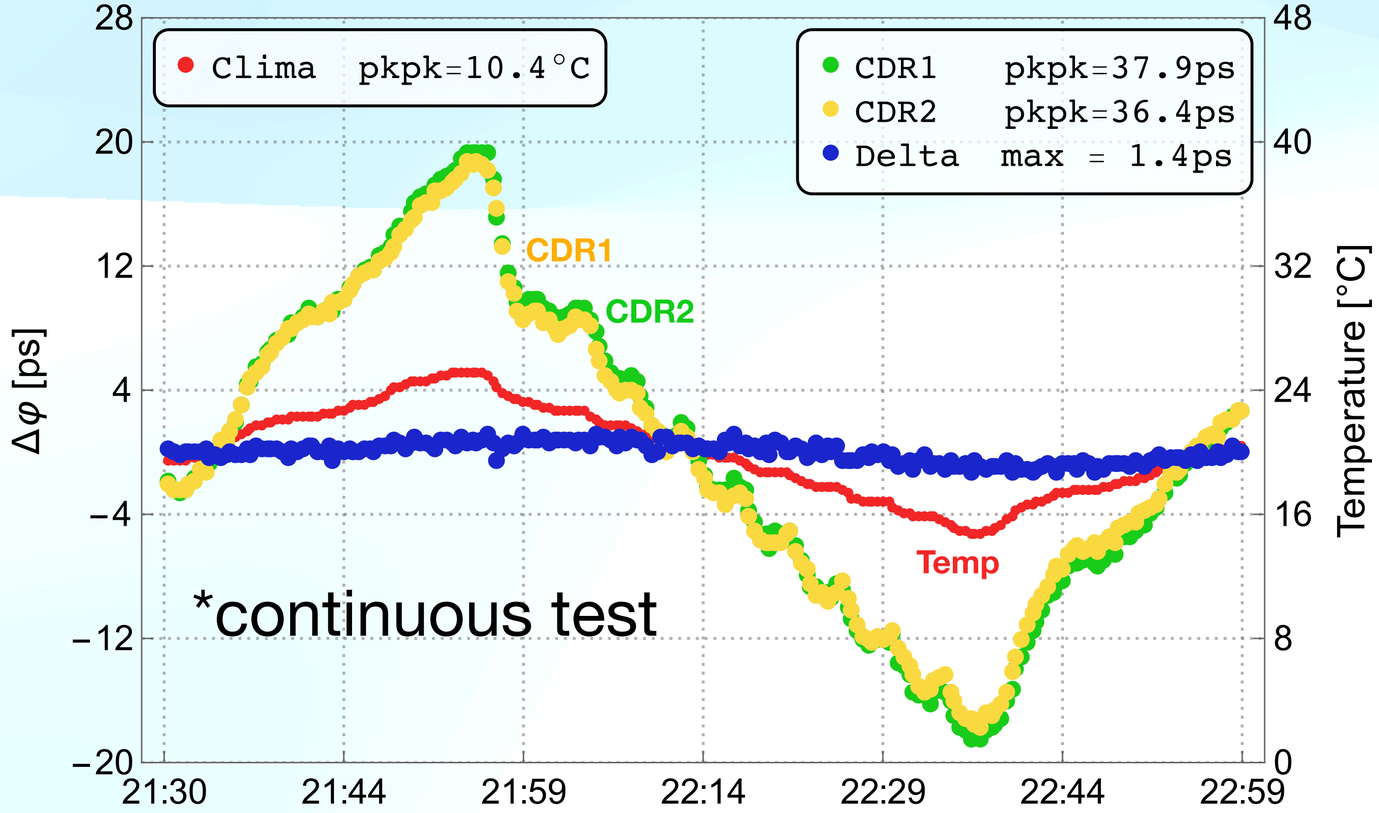
Temp stability: 3ps/degC

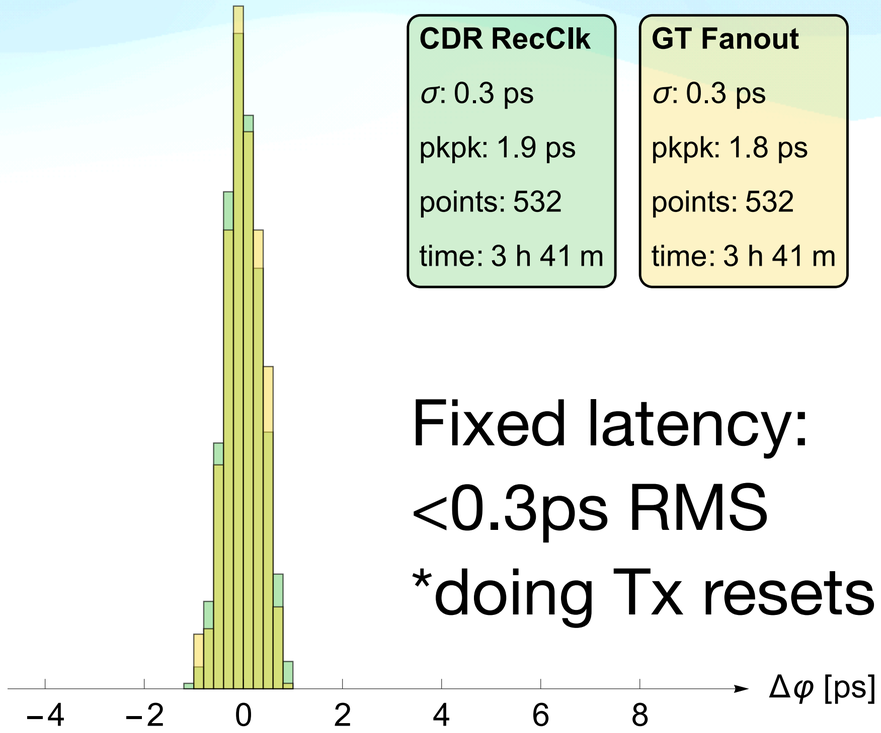
*corrected for SMA cable

Consistent between different devices



*The scope performs the measurement when switching on a clock pattern data.



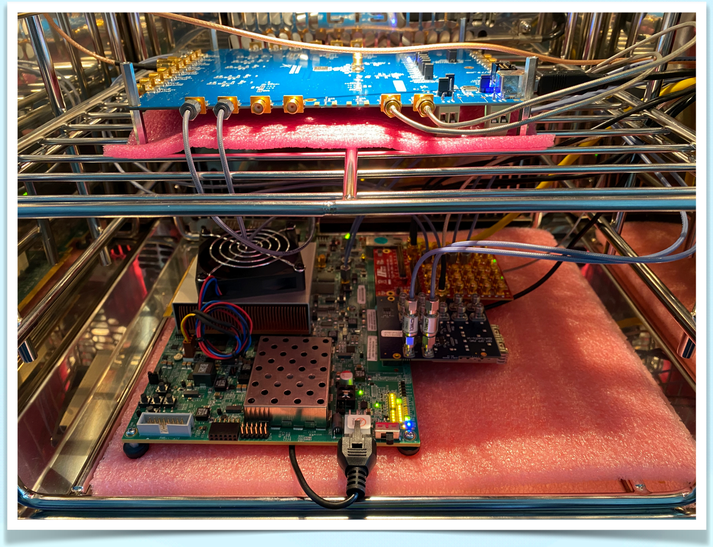


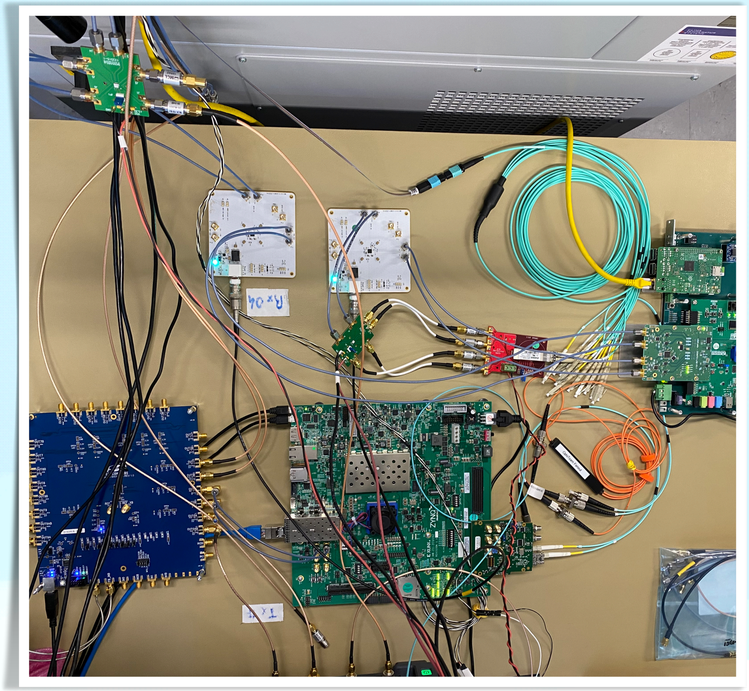
CDR RecClk	GT Fanout
σ: 0.3 ps	σ: 0.3 ps
pkpk: 1.9 ps	pkpk: 1.8 ps
points: 532	points: 532
time: 3 h 41 m	time: 3 h 41 m

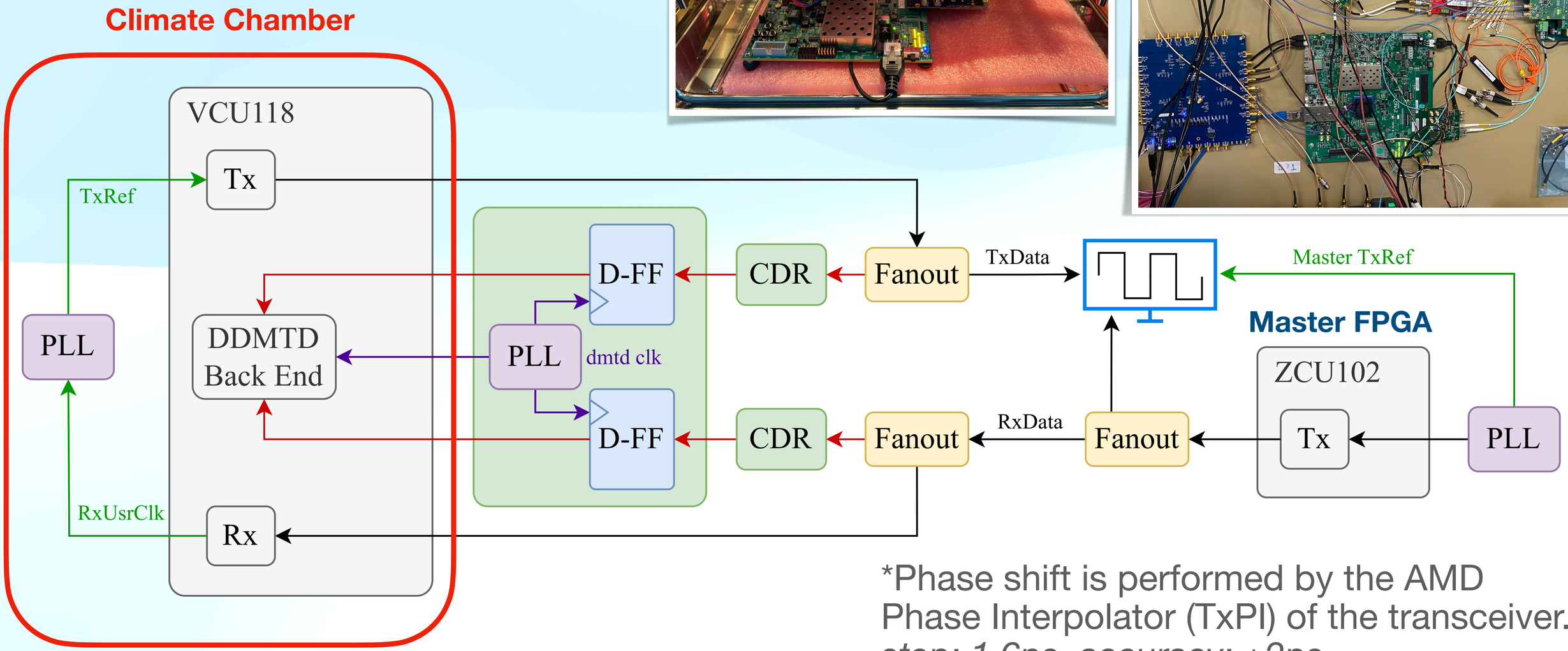
Fixed latency:
<0.3ps RMS
*doing Tx resets

CDRs are phase stable and equal

PCB Proof of Concept







*Phase shift is performed by the AMD Phase Interpolator (TxPI) of the transceiver.
step: 1.6ps, accuracy: ±2ps

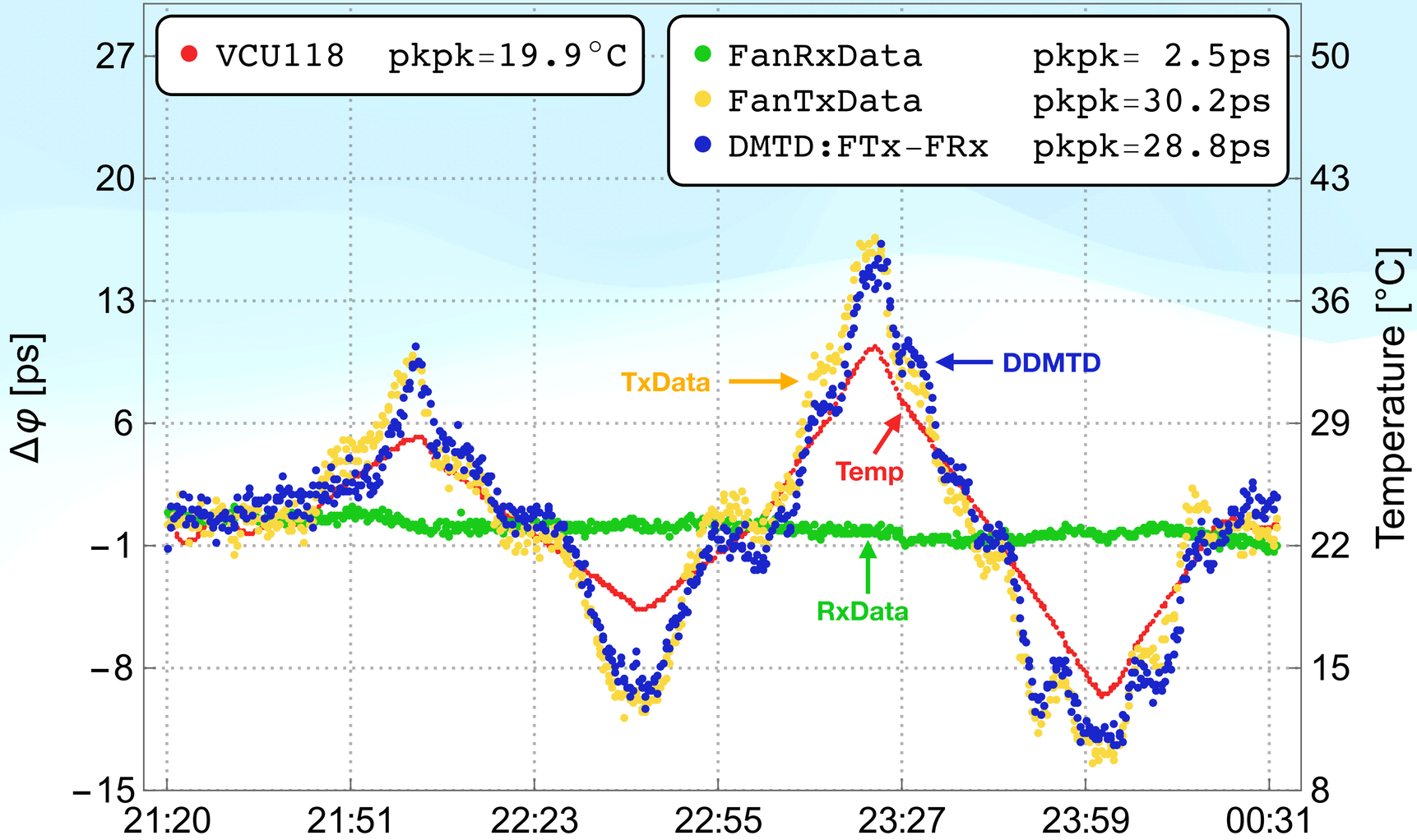
PCB Proof of Concept @2.4Gbps/60MHz

DDMTD PCB is measuring the phase between Rx and Tx recovered clocks from the two CDRs.

The DDMTD error is below 5ps.

TxData: 1.5ps/degC.

The scope performs the measurement when switching on a clock pattern data.

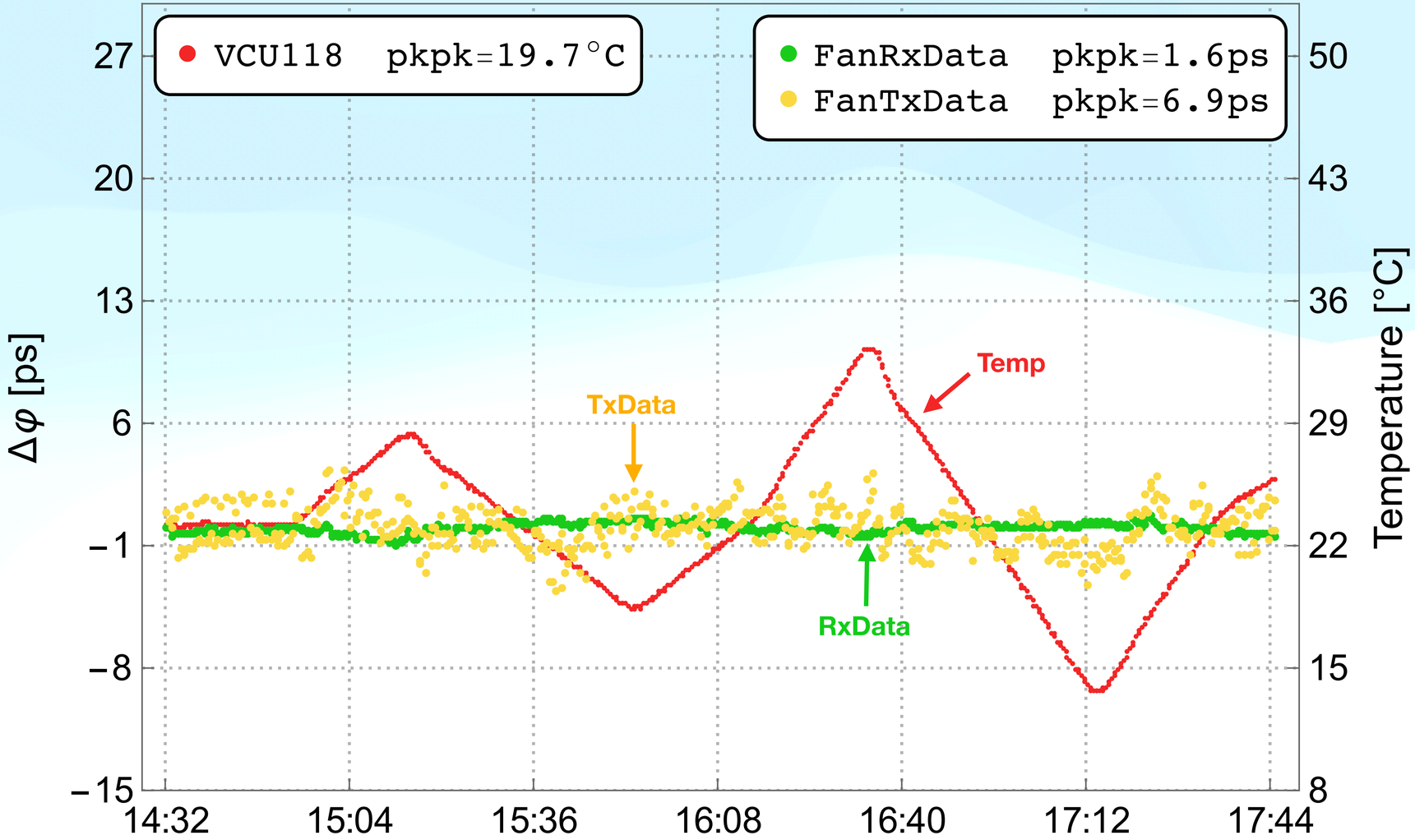


PCB Proof of Concept @2.4Gbps/60MHz

Now, the phase shifter uses the DDMTD measurement to achieve fixed latency on the VCU118.

The phase stability achieved on **TxData** is 1.1ps RMS.
With no temperature dependency.

TxData wander is due to TxPI resolution and accuracy, plus cable asymmetries.



Conclusions

A Mezzanine design for a FPGA-agnostic and phase stable timing link has been described.

The targeted components show promising performances for phase stability, proving to be suitable for the concept.

Symmetrical routing is required.

A proof of concept test has demonstrated the reliability of the phase drift tracking and compensation technique.

Next step: PCB design and production.