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# An FPGA-agnostic system for achieving picosecond-level phase determinism in timing distribution links for High Energy Physics Experiments

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Picosecond-level phase determinism in timing distribution systems is a requirement for future detectors in High Energy Physics. FPGA transceivers traditionally used to propagate timing do not meet by default this stringent requirement, and suffer from phase jumps at startup and temperature drifts. While ad-hoc solutions have been developed based on particular FPGA features to measure phase shifts and to apply phase corrections, they remain FPGA specific and therefore cannot be generalized to any type of timing link. This paper presents a study of discrete components for phase shifting and monitoring, allowing the implementation of a generic deterministic link.

## Summary (500 words)

In HEP Experiments, the detectors require to associate a precise timestamp to the measured events produced by the particles collisions. The high luminosity provided by the upcoming major upgrade of the HL-LHC will induce a high rate of collisions (up to 200 per bunch) - also called pile-up - which will be a challenge for future detectors; in particular, disentangling vertices with such a pile-up level will require distributing machine timing to the Front-End electronics with an extreme precision and stability of the order of a few picoseconds, a requirement which is not a priority in Commercial Off-the-shelf components like FPGAs used in traditional timing distribution chain.
In particular, FPGA transceivers have shown inconsistencies in terms of phase stability after resets or power cycles. Optical fibers and FPGA logic are also highly sensitive to temperature variations (of the order of 15 to 30 ps per degree C for a 100m fiber, and between 2 and 4ps per degree C for FPGA logic), leading to potentially substantial phase drifts even in the controlled environment of a counting room.
Several detailed studies have been carried out in the community in recent years to overcome these difficulties. Some have been presented at TWEPP in recent years, such as the TCLink for stabilizing the operation of transmitters in AMD/Xilinx FPGAs of the Ultrascale/Ultrascale+ family at ±1.5ps peak-to-peak, or compensating for phase variations due to temperature changes in optical fibers. Other techniques for constraining the receivers of these FPGAs have also been studied, with promising results of the order of ±5 to 10ps peak-to-peak per hop. All solutions are using internal FPGA features like transceiver phase interpolators for phase shifting, and Digital Dual Mixer Time Difference (DDMTD) logic for phase variation measurement.
Although showing promising performance, these solutions remain intrinsically linked to the architecture and specificities of FPGA families and their transceivers. To overcome this drawback, a study carried out as part of the CERN EP RnD and ECFA DRD7 programs, proposes to implement a generic solution to compensate for the instability of FPGAs, irrespective to their performance in terms of phase stability and temperature sensitivity.
This concept is based on a feedback loop encompassing the FPGA and its transceivers, and on discrete measurement and phase compensation components developed within the HEP community. This paper proposes to present the concept and building blocks of the generic solution and to describe the comparative perfor-

mances of components of a traditional solution based on FPGAs with those of such a generic implementation. In particular, stability of the discrete phase shifters and phase measurement circuits versus temperature and their immunity against cross-talk will be demonstrated.

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