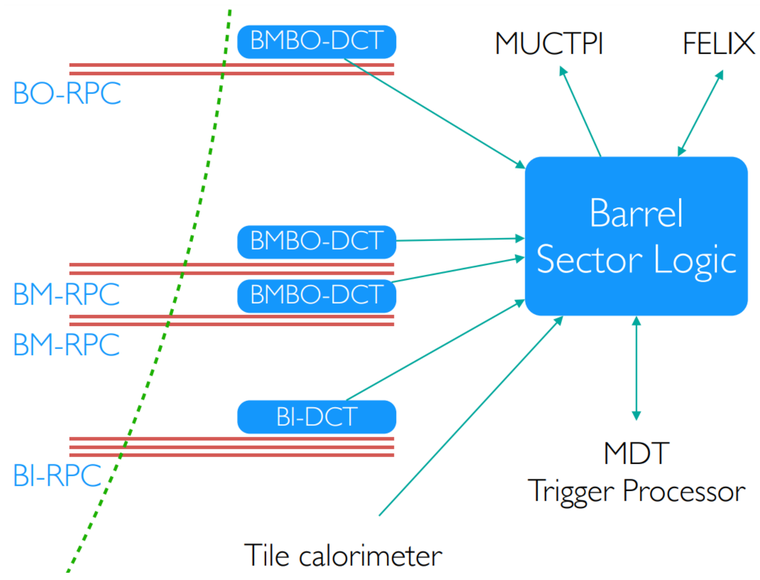
Low-latency hardware trigger for muons in the barrel region of the ATLAS experiment at the High-Luminosity LHC

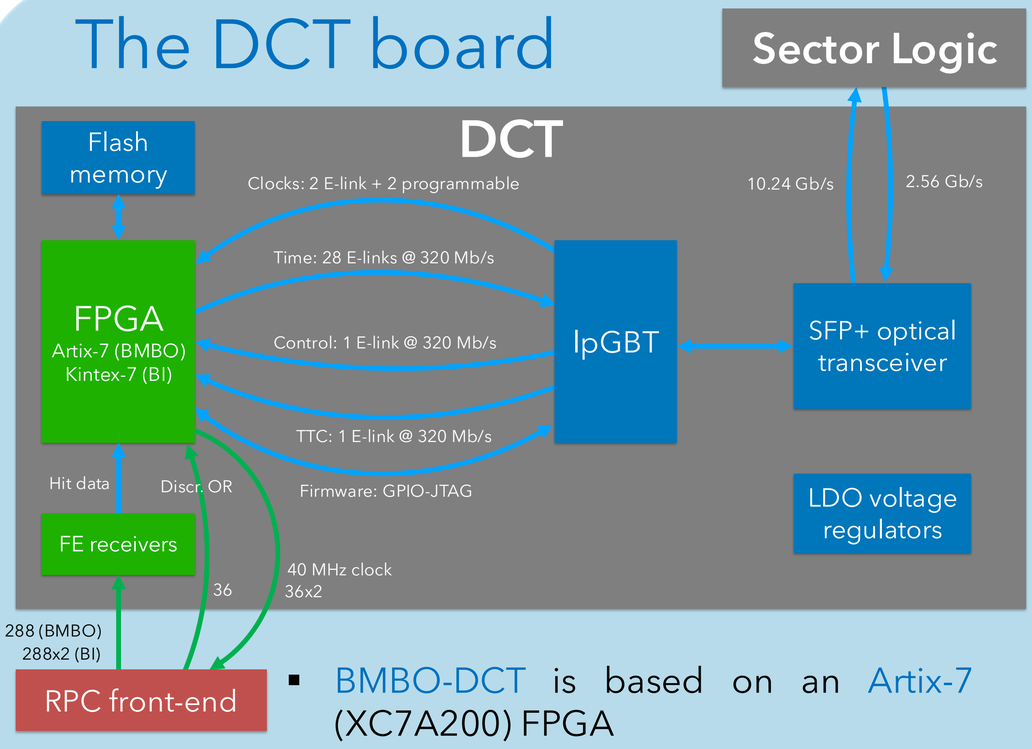
Topical Workshop on Electronics for Particle Physics (TWEPP)
30 Sep – 4 Oct 2024, Glasgow, UK

The L0 Muon barrel trigger system

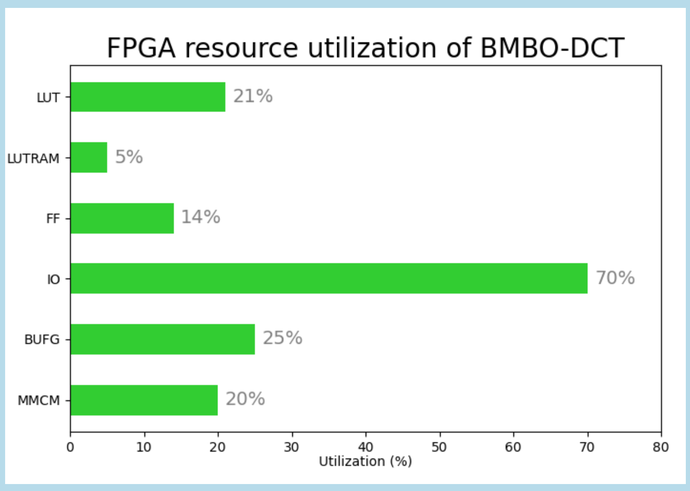
- L0 muon barrel trigger is performed by Resistive Plate Chambers (RPC): 3 legacy stations (2 BM, 1 BO) + 1 novel BI station
- Entire trigger and readout electronics will be replaced to cope with the higher luminosity ($5 \cdot 10^{34}\ \mathrm{cm^{-2}s^{-1}}$) and average pileup (140) of HL-LHC
- RPC data will be collected by 1546 on-detector DCT boards and sent to 36 off-detector Sector Logic (SL) boards, which will perform trigger and readout logic
- L0 RPC trigger candidates will require hit coincidence in at least 3 RPC stations or BI-BO hit coincidence: this looser coincidence with respect to the current system will allow to increase the trigger acceptance from 78% to 96%
- Trigger candidates are further processed by MDT trigger processors to reduce the trigger rate and to increase the geometrical resolution
- L0 trigger rate: 1 MHz. RPC SL candidate rate: 100 kHz, reduced to 30 kHz after MDT-TP processing. RPC SL trigger latency: 390 ns

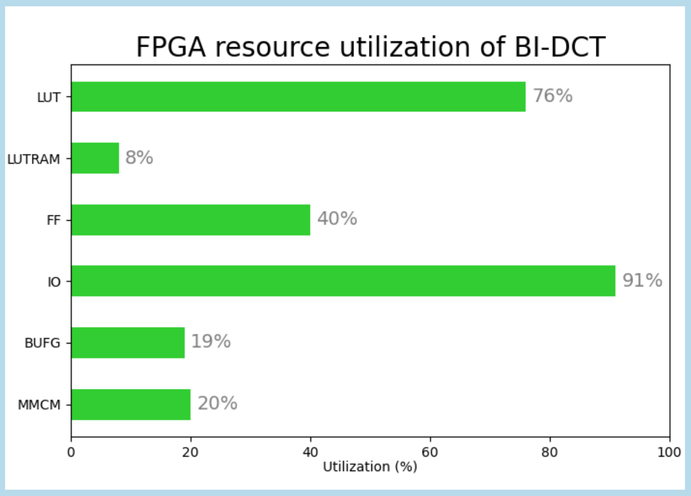


The DCT board

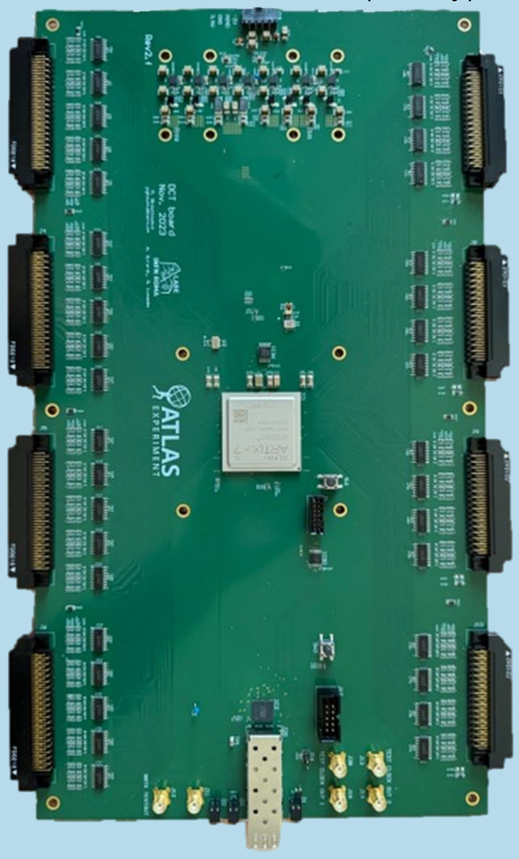


- BMBO-DCT is based on an Artix-7 (XC7A200) FPGA
- Analog pulses are sent from 288 front-end (FE) boards
- FPGA performs RPC hit digitisation with 1.2 Gb/s sampling (240 ps time resolution)
- lpGBT ASIC handles serial data transmission with SL
- BI-DCT design is based on the BMBO-DCT design but uses a Kintex-7 (XC7K325) FPGA
- Digital signals are sent from 288 FE boards with Manchester encoding
- Both firmwares are ready and simulated
- Maximum latency of BMBO-DCT firmware, measured to be 500 ns from simulation, is within requirements
- Second BMBO-DCT prototype delivered and tested
- First BI-DCT prototype design is almost completed, the delivery is expected by the end of 2024





Second BMBO-DCT board prototype

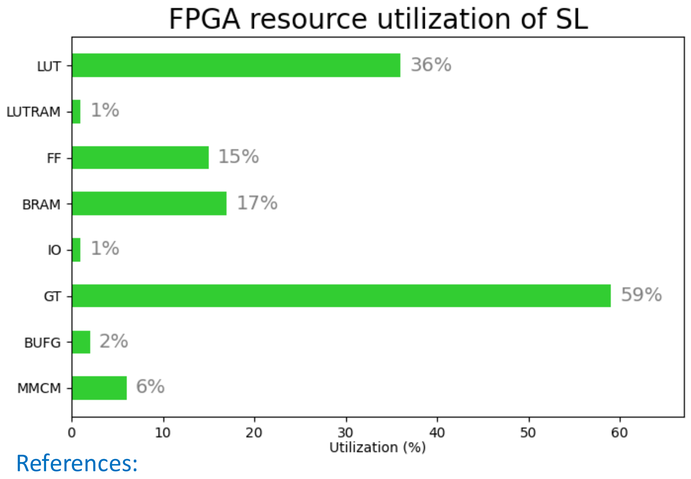


BMBO-DCT prototype tests

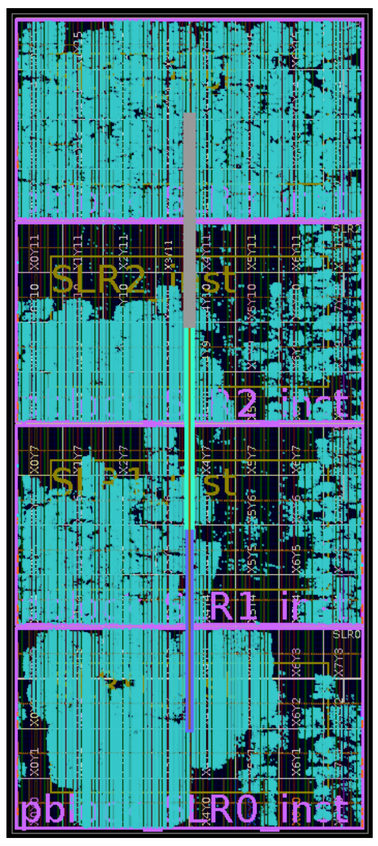
- All functionalities of second BMBO-DCT prototype have been tested and no issues were found:
  - All E-links tested with PRBS7 at 320 Mb/s data rate for a 120 hour long test, no errors found (bit error rate < $7.2 \cdot 10^{-15}$);
  - Each lpGBT clock tested using it as source clock for the DCT firmware, all clocks are stable;
  - lpGBT GPIO pins tested using an I2C slave in the FPGA;
  - FPGA and flash memory successfully configured;
  - SFP+ transceiver tested using an I2C master in the FPGA;
  - Each FE connector tested separately sending 10 ns pulses from an emulator board.

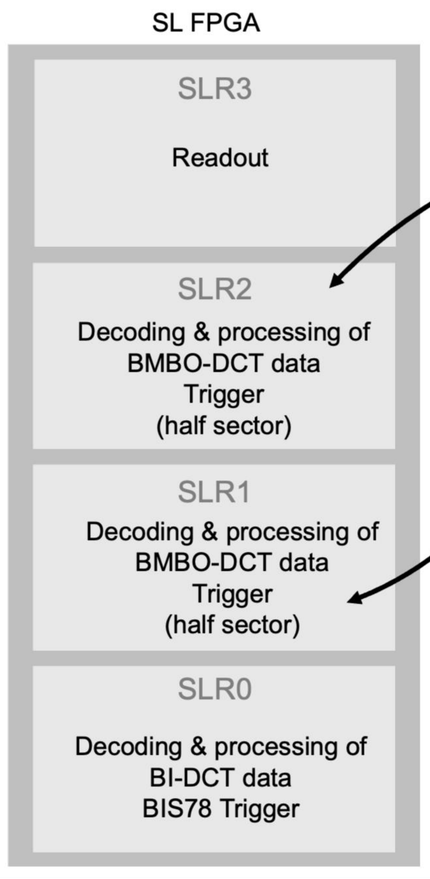
The Sector Logic board

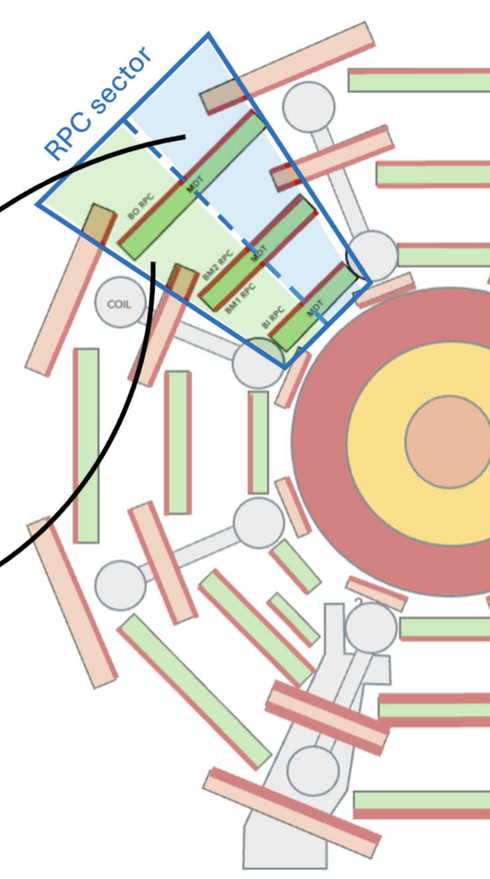
- SL board is based on Virtex Ultrascale+ (XCVU13P) FPGA
- A Zynq System-on-Chip (SoC) is used to interface with ATLAS servers
- Firmware ready and simulated
- SL FPGA is divided into 4 Super Logic Regions (SLR) and floorplanning and pipeline registers used to fulfill the strict timing constraints (logic based on 240 and 320 MHz clocks)



- First prototype extensively tested
- Communication test with BMBO-DCT prototype successfully performed
- AXI C2C protocol (for FPGA-SoC communication) and interfaces with ATCA crates tested
- Second prototype delivered and under test







References:
[1] ATLAS Collaboration. *TDR for the Phase-II Upgrade of the ATLAS Muon Spectrometer*. CERN-LHCC-2017-017.
[2] ATLAS Collaboration. TDR *for the Phase-II Upgrade of the ATLAS TDAQ System*. CERN-LHCC-2017-020.

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