Contribution ID: **48** Type: **Poster**

Low-latency hardware trigger for muons in the barrel region of the ATLAS experiment at the high-luminosity LHC

Thursday 3 October 2024 17:40 (20 minutes)

The High-Luminosity upgrade of the LHC (HL-LHC) will triple the proton-proton collision rate, posing challenging requirements for the ATLAS trigger and readout system. A low-latency, FPGA-based hardware trigger for muons in the barrel region will be implemented to identify candidates within 1.7 μs from collisions for further refinement by the Monitored-Drift-Tubes-Trigger-Processor. An additional layer of RPC detectors and the replacement of the trigger and readout electronics will keep high efficiency for both single-muon and multi-muon triggers, without any rate increase compared to the current one, despite the higher collision rate. Tests are progressing to be ready for HL-LHC operations.

Summary (500 words)

The High-Luminosity Large Hadron Collider (HL-LHC), scheduled to start operations in 2029, will exhibit over three times the instantaneous luminosity of LHC Run 3. To accommodate the higher proton-proton collision rate, an upgrade is necessary for the ATLAS trigger and readout system.
Specifically, this upgrade prioritizes the implementation of low latency hardware triggers for muons in the barrel region, ensuring rapid and efficient detection of relevant events within the increased data flow.
The current first-level hardware muon trigger system in the ATLAS barrel region utilises
on-detector ASIC boards implementing a coincidence-based algorithm across three concentric doublets of Resistive Plate Chambers (RPC). This setup selects muon candidates according to three predetermined transverse momentum thresholds.
To meet the requirements of the HL-LHC, significant upgrades are in progress to enhance the ATLAS Level-0 Barrel Muon Trigger System. These upgrades involve introducing a new inner layer of RPC detectors, the Barrel Inner (BI) station, featuring three gas gap RPC chambers.
Furthermore, the replacement of trigger and readout electronics is in preparation to ensure sustained performance, even under extreme particle rates and higher data throughput. For the barrel system, the primary electronic boards are based on two Xilinx Field Programmable Gate Array (FPGA) devices: the Data Collector and Transmitter (DCT) and the Sector Logic (SL) boards. The DCT boards sample RPC hit data and transmit them to the SL after zero suppression, aiming to reduce data throughput. The SL executes the trigger algorithm, forwarding up to four muon candidate coordinates and trigger threshold measurements to the Monitored Drift Tubes Trigger Processor (MDTTP) board. Only the muon candidates validated by the MDTTP are sent to the Central Trigger Processor, which decides if the event has to be registered. This integrated approach optimizes the muon selection process, effectively reducing the RPC trigger rate. Importantly, all the aforementioned processes occur with low latency to meet the stringent L0 latency requirement set by the ATLAS TDAQ system. Most of the firmware has already been developed, tested and proved to respect the latency requirements in simulation. Additionally, tests are currently underway for both the DCT and the SL prototypes to include hardware and firmware validation.

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Session Classification: Thursday posters session

Track Classification: Trigger and Timing Distribution