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Testing of the Prototype CMS Global Level-1 Trigger for Phase-2

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The Global Trigger will be the final stage of the new Level-1 trigger for Phase-2 operation of CMS. Based on high-precision inputs from the muon-, calorimeter-, track- and particle flow triggers, it will evaluate a menu of O(1000) cut-based and machine-learning-based algorithms in a system of up to thirteen Serenity processing boards equipped with AMD Ultrascale+ FPGAs and interconnected with 25 Gb/s optical links. We report on tests of a firmware prototype, integration tests with the upstream systems and the ongoing integration of a prototype into a slice test connected to the running experiment.

Summary (500 words)

For Phase-2 of the LHC, starting in 2029, CMS will undergo major upgrades to its detectors and readout electronics. A completely new Level-1 trigger system will ensure that the excellent physics performance of CMS is maintained or improved under the challenging pile-up conditions in Phase-2. The new trigger system, based on generic ATCA processing boards hosting Xilinx Ultrascale Plus FPGAs and interconnected with links at 25 Gb/s, will exploit high granularity information from the calorimeters, muon systems and a track finder, reconstructing tracks from the silicon strip tracker at the bunch crossing rate. The trigger system will contain algorithms such as particle flow that previously only have been employed in software at the higher trigger levels. The final stage of the Level-1 trigger, the Global Trigger (GT), will receive high-precision trigger objects from the muon-, calorimeter-, track- and particle flow triggers. It will evaluate a menu of O(1000) cut-based and machine-learning-based trigger algorithms in order to determine the Level-1 trigger accept decision. Up to twelve generic processing boards will each receive a copy of all inputs from the upstream systems, allowing algorithms to be freely assigned to any processing board. A 13th generic processing board, the Final-OR board, will handle pre-scaling and monitoring of the algorithms, assignment of the trigger type, merging of the algorithm decisions and transmission of the trigger decision to the Trigger Control and Distribution system. The target board for all thirteen processing boards is the Serenity board, equipped with a single VU13P FPGA. Upstream systems use either the Serenity board or one of two other flavors of generic ATCA processing boards. Interfaces to all upstream systems have been defined and prototype firmware has been developed for both the Algorithm and Final-OR boards to handle all basic algorithms and their pre-scaling and monitoring (as reported at the two previous TWEPP conferences). The focus currently lies on validating the prototype designs by performing integration tests. We report on two-board and multi-board integration tests that have been performed between the boards in the GT system and with upstream boards. In addition to these tests, a prototype GT board is currently being integrated with the Drift Tube slice test, a test setup connected to the running experiment that tests a full vertical slice of Phase-2 electronics from on-chamber electronics in the muon drift tube system up to the Global Muon Trigger. The GT prototype, a special version that merges algorithm and final-OR functionality into one board, is expected to receive muon candidates found in two instrumented sectors of the CMS barrel and to send its trigger output to the 40 MHz L1 Scouting system that will record it at the 40 MHz bunch crossing rate. With this test setup we are aiming to compare the trigger rates and efficiencies of a full slice of Phase-2 electronics to its Phase-1 counterpart and to gain operational experience with the Phase-2 hardware, firmware and software. We will report on the state of the system.

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