Design and implementation of the timing and synchronization system for JUNO-TAO detector

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Introduction to JUNO-TAO

JUNO (Jiangmen Underground Neutrino Observatory), a multiple purpose neutrino experiment

- Neutrino mass hierarchy
- Precision measurement of 3 oscillation parameters
- Supernova neutrino
- Geo-neutrino
- Solar neutrino
- Proton decay
- …

$3\%/\sqrt{E}$ energy resolution

20k ton LS

Online in 2025

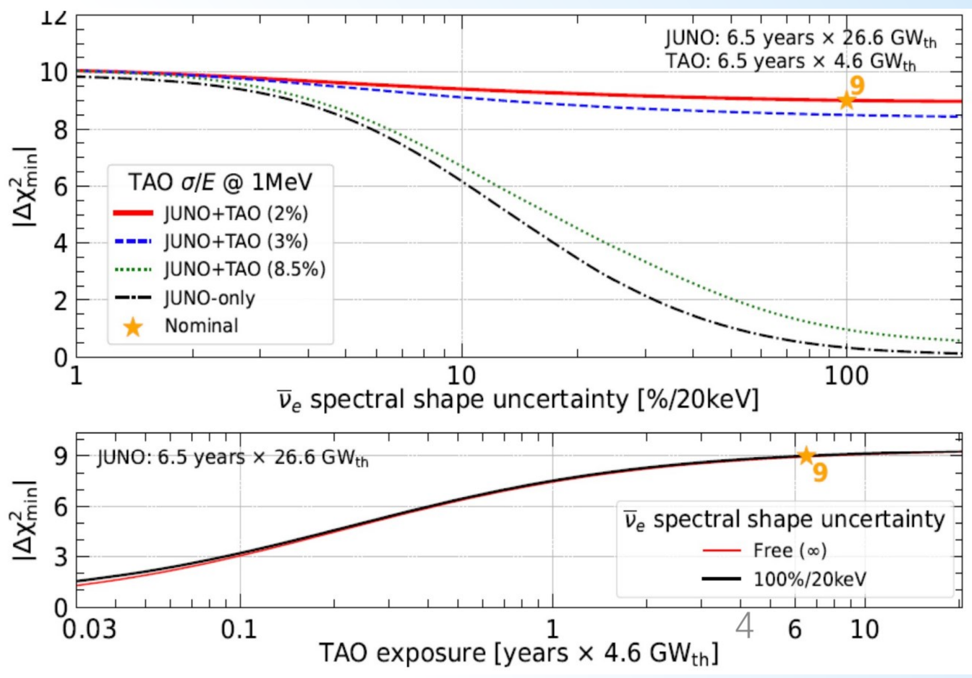
TAO (Taishan Antineutrino Observatory), a satellite experiment of JUNO

- Measure reactor neutrino w/ sub-percent E resolution
- Short-baseline reactor antineutrino experiment
- Location: 44 m from Taishan NPP core (4.6 GW)

Online at the beginning of 2025

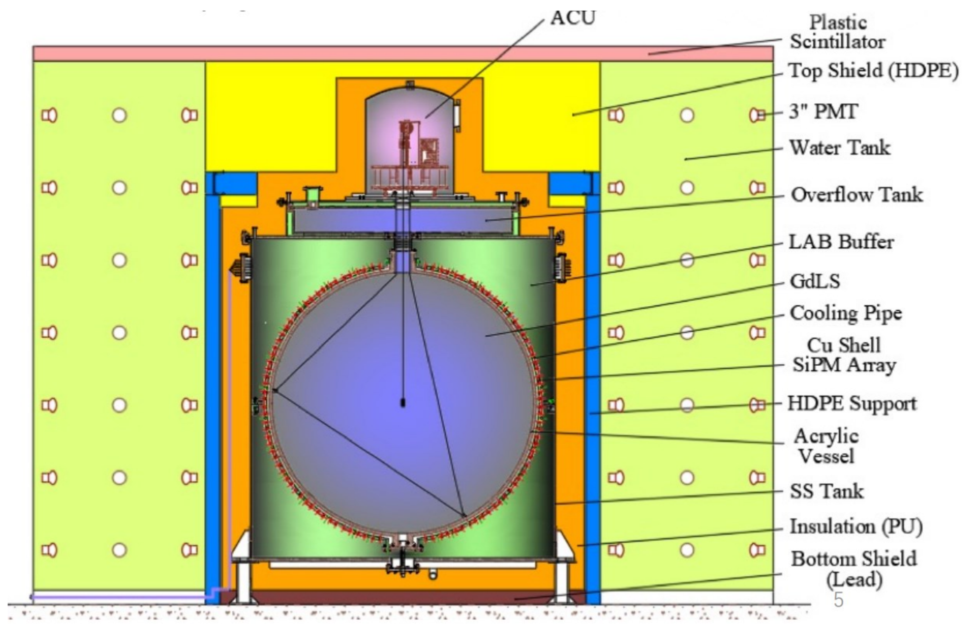
TAO Motivation

1. Provide reference spectrum for JUNO
   - TAO can help to remove the model dependence by measuring fine structures in neutrino energy spectrum
   - The energy resolution of TAO must equal or better than $3\%/\sqrt{E}$ (now $<2\%/\sqrt{E}$).
   - Reactor spectral shape precision better than 1% in 2-5 MeV
2. Provide a benchmark spectrum for nuclear database
3. Measuring isotopic neutrino spectrum
4. Reactor monitoring
5. Sterile neutrino



TAO Detector

- -9.6 m underground
- ~ 10 m² SiPM coverage (95%)
- 1.8 m diameter, 2.8 ton GdLS (1 ton for fiducial volume cut)
- Operate at -50°C
- 2000 IBD/day (1000 w/ FV)
- 4500 p.e/MeV

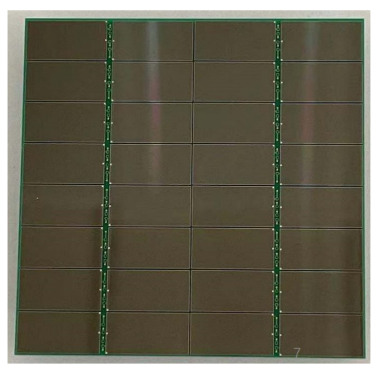


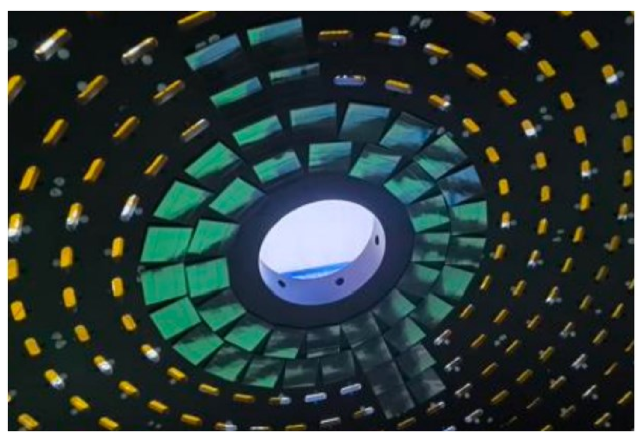
Inner → Outside

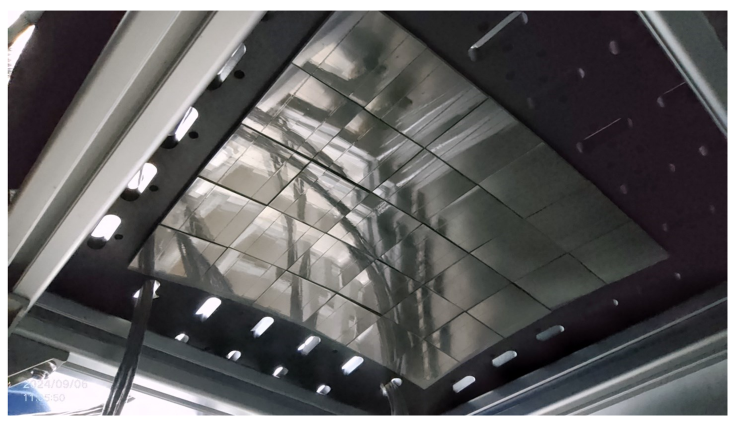
Gd-LS ⇨ acrylic vessel ⇨ SiPM & support ⇨ LAB buffer ⇨ cryogenic vessel ⇨ water & HDPE shield ⇨ muon veto

SiPM (Silicon photomultiplier)

- Tile 50.8 x 50.8 mm², 4024 tiles from HPK
- ~ 8000 channels, charge resolution per channel ⩽ 15%
- Supported & cooled by copper shell
- Work at -50°C, dark noise 100k➔100 Hz/mm²
- All QA finished



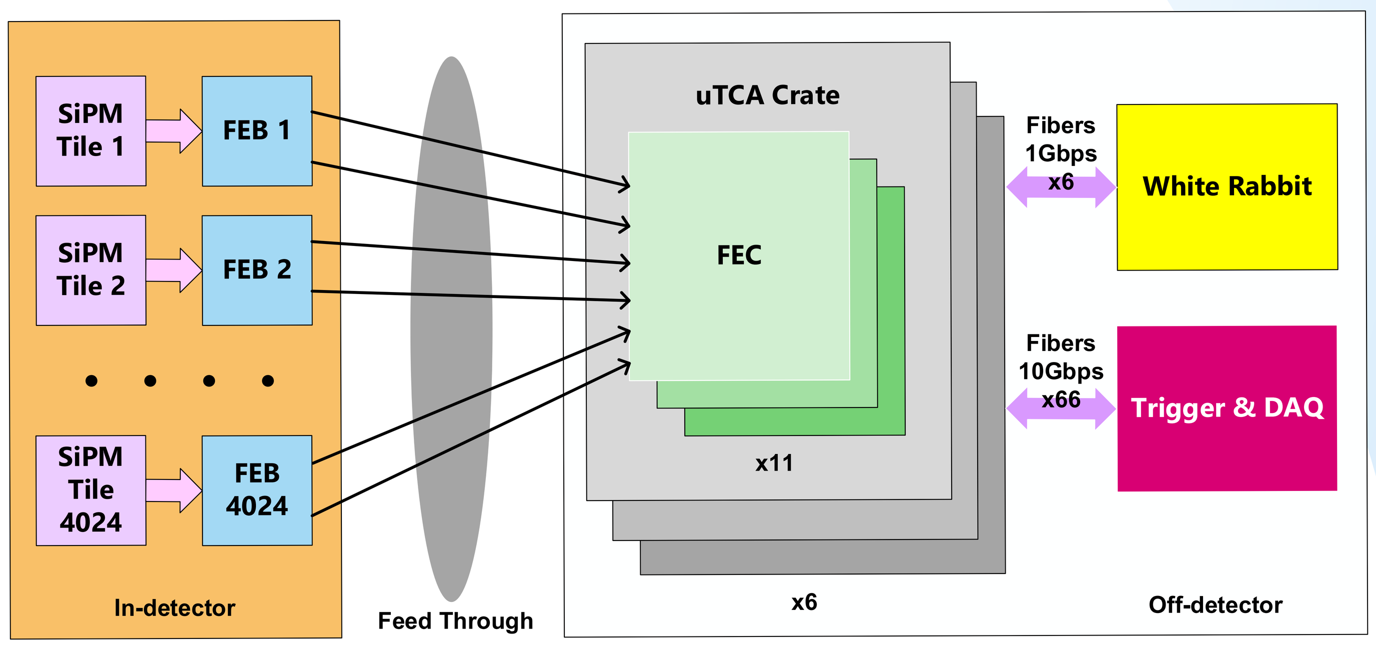




Electronics & TDAQ

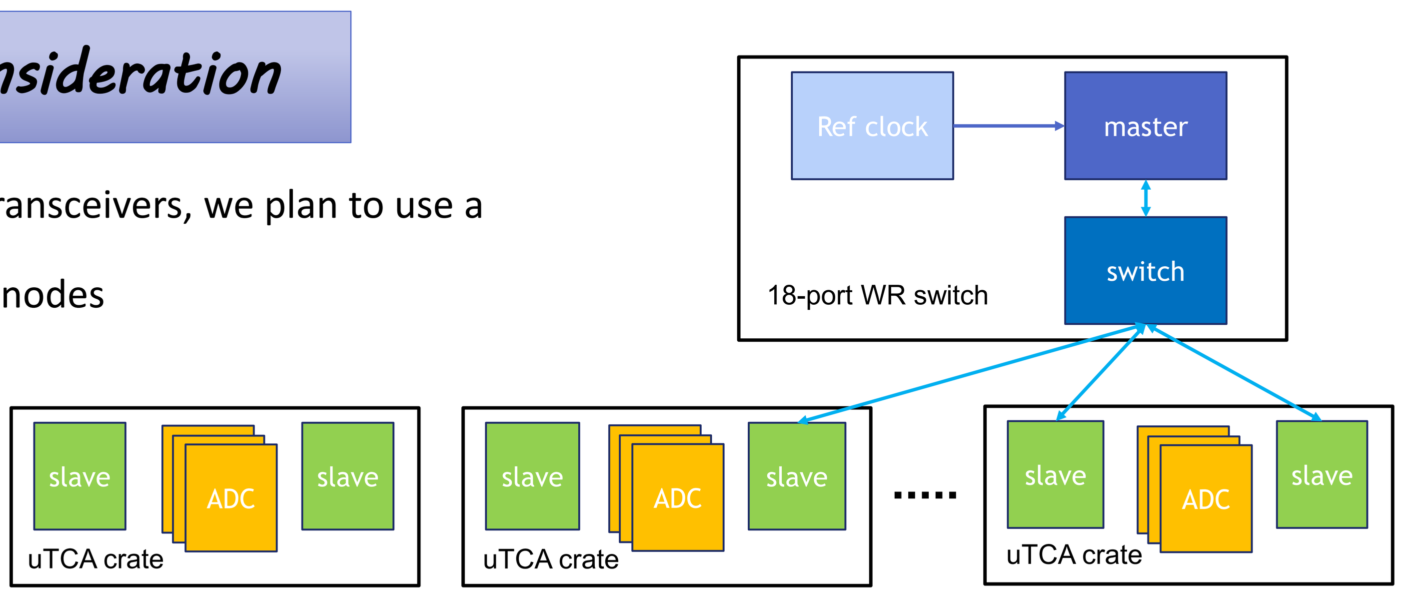
- Electronics of central detector (CD)
  - FEB based on discrete components
  - FEC in MicroTCA crate
    - Waveform digitized by ADC (14-bit@250MHz or 16-bit@125MHz)
    - FPGA calculates Q/T, sent to TDAQ
  - WR for clock synchronization

The White Rabbit Project



Clock Redundancy Consideration

- Due to the life limit of fiber optic transceivers, we plan to use a redundant WR clock
- Each uTCA crate has two WR slave nodes
- Clock source selection
  - WR node report the loss of lock
  - DCS get the report, and configure the hardware to switch to the redundant node



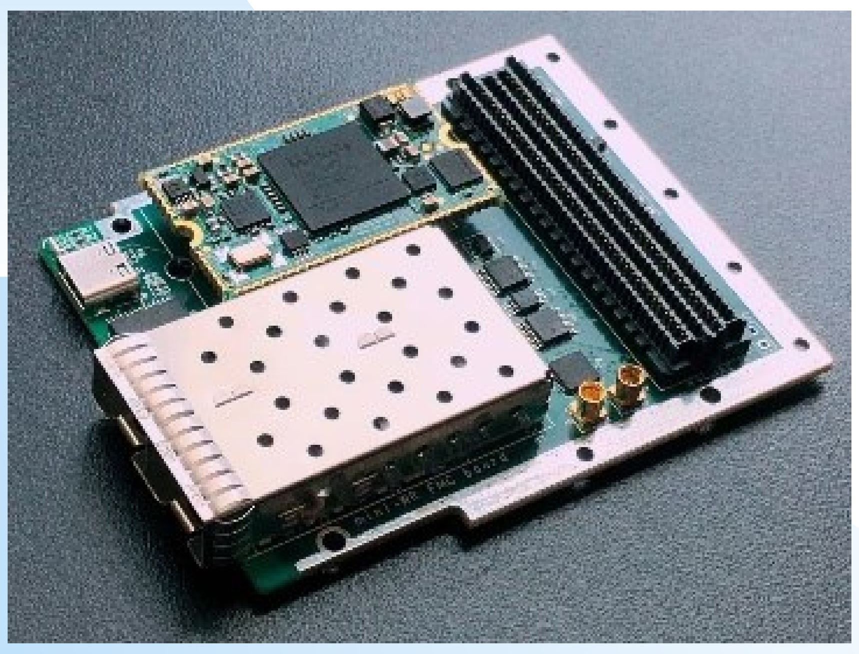
Clock Distribution in MicroTCA

Two clock allocation schemes inside the crate

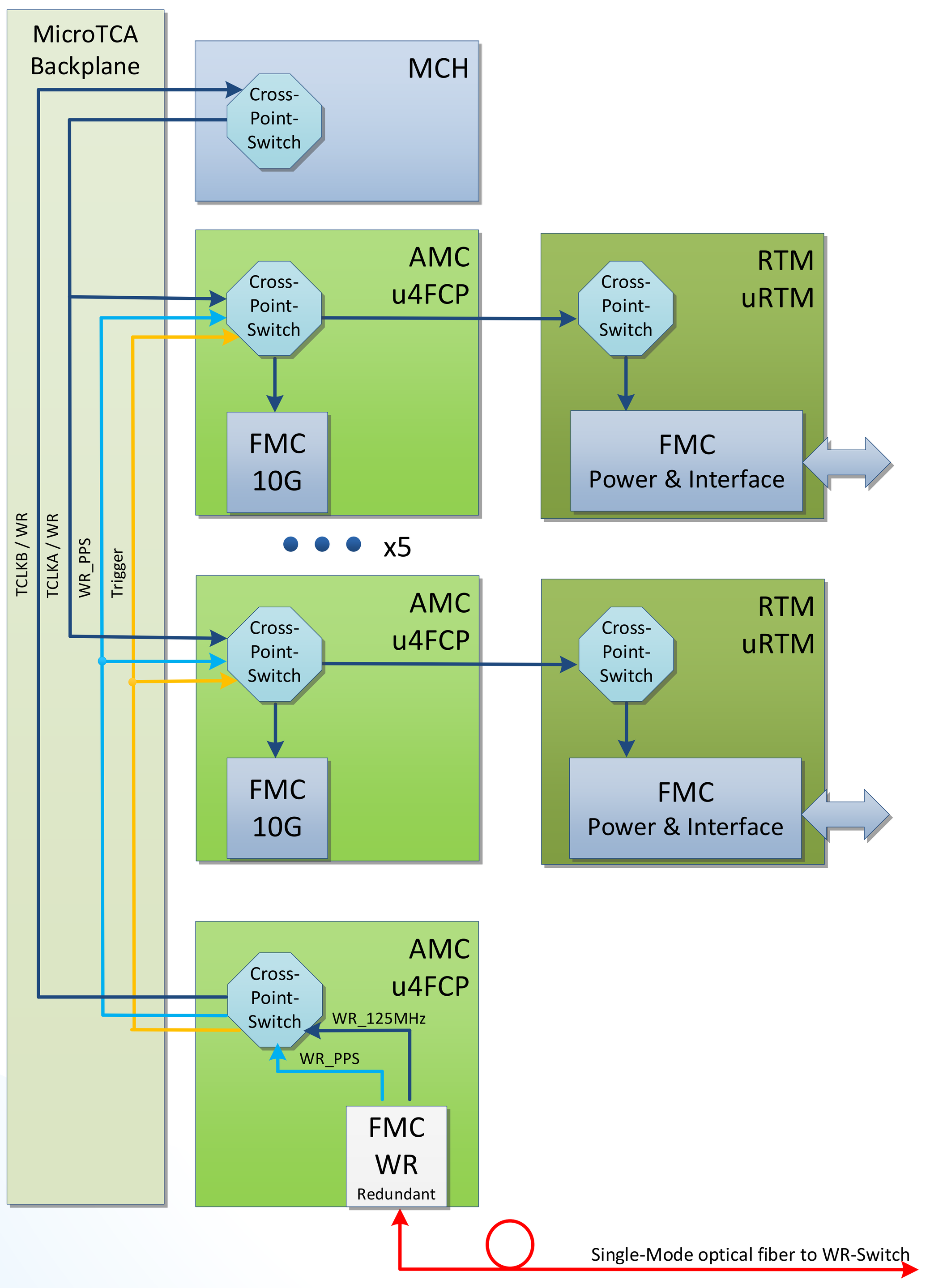
- Port 17
  - Native R9 crate with WR Support
  - MLVDS multi-drop connection

or

- TCLK
  - TCLKB (slot12)-> MCH (NAT-MCH-PHYS80) -> TCLKA (slot1-11)

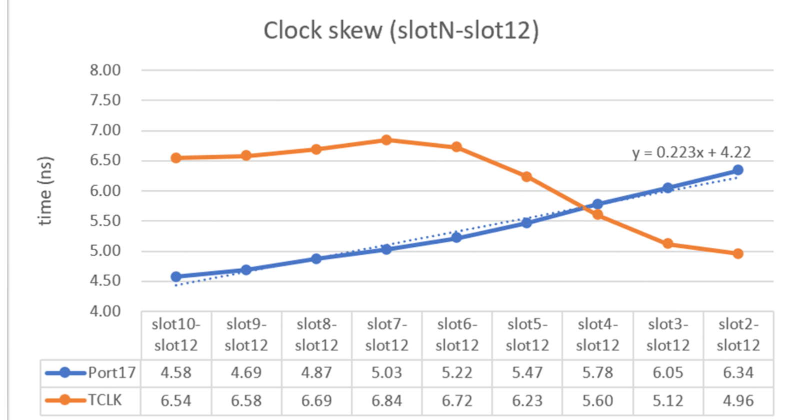


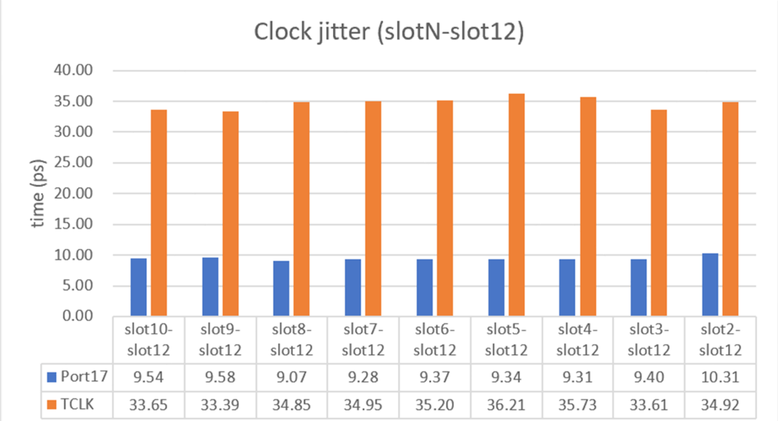
Mini-WR FMC for System-level clock synchronization



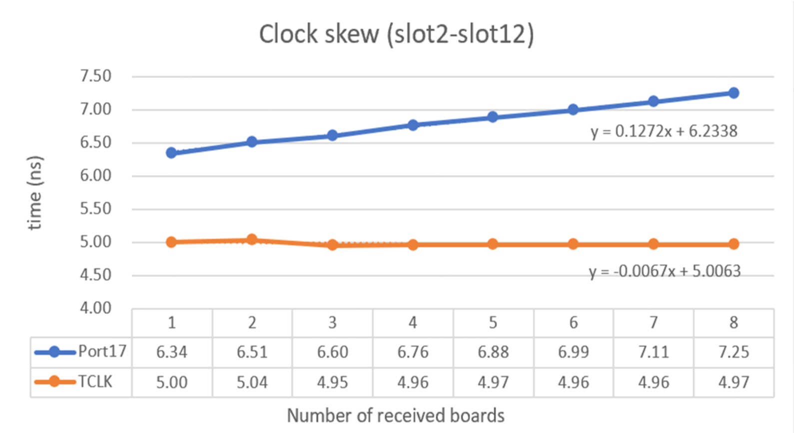
Test results

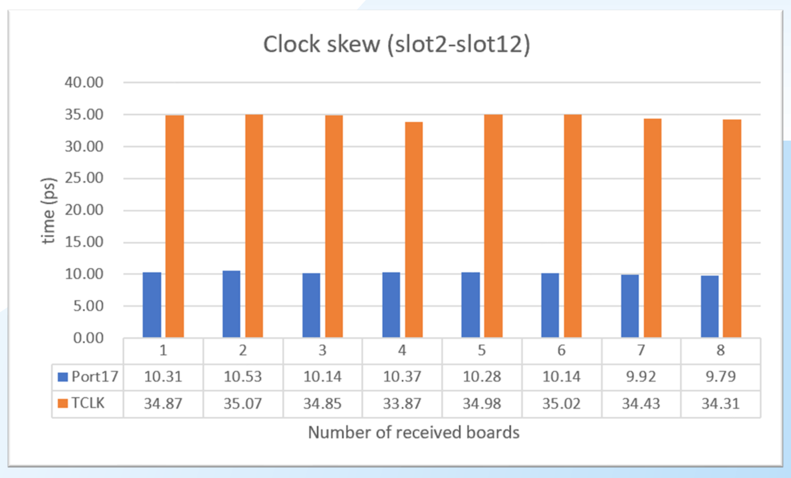
- AMC with mini-WR fixed in slot 12, move AMC receiver





- Receiver is fixed at slot 2, add more adjacent AMC boards





- TCLK scheme has deterministic skew, but more jitter
- Port17 scheme has smaller jitter, but the skew is related to the location and receiver quantity