Contribution ID: **60** Type: **Poster**

Design and implementation of the timing and synchronization system for JUNO-TAO detector

The Taishan Antineutrino Observatory (TAO) aims to measure the energy spectrum of reactor antineutrinos, providing a reference spectrum for the JUNO and offering benchmark references for the nuclear databases.
The JUNO-TAO experiment uses 4024 SiPM tiles with 8048 ADC channels to ensure the proposed energy resolution(<1.5% @ 1 MeV), spatial resolution(around 1 cm), and timing performances(around 1 ns).
This paper presents an implementation of timing and synchronization system with the White Rabbit(WR) distributed synchronous timing technology.
The R&D effort carried out to study the timing and synchronization and the other components, supported by laboratory test results, will also be presented.

Summary (500 words)

The White Rabbit (WR) distributed synchronous timing technology enables multi-node sub-nanosecond clock distribution, meeting the system's clock synchronization accuracy requirements. To ensure the consistency of each channel's events and the accuracy of ADC sampling, a high-precision timing and synchronization system is crucial for the TAO experiment.

We designed and implemented a timing and synchronization system for the TAO readout electronics, verifying the feasibility of the chassis-level clock distribution method and comparing the jitter and skew performance of two clock distribution schemes through the MicroTCA backboard. Additionally, we developed firmware for the Module Management Controller (MMC) based on FreeRTOS, enabling the management and monitoring of the status of readout electronics boards and the clock modules on the boards.

The paper also conducts clock performance tests on the timing and synchronization system to verify that the system meets the requirements of the TAO experiment. The research primarily focuses on the readout electronics architecture and timing synchronization requirements of TAO. Specific work includes:

1. Design and deployment of the White Rabbit (WR) network for TAO, configuration of master and slave nodes, establishment of WR synchronization links, and parameter calibration compensation for hardware delays to achieve ps-level clock deviation.
2. Design and implementation of clock modules on the boards, optimizing and transmitting the synchronized clocks. It designs a clock-compatible circuit so that the Advanced Mezzanine Cards (AMC) can serve as both clock sending and receiving boards, and two feasible clock distribution schemes based on the backplane bus are also implemented and compared on these boards.
3. Testing and verification of the implemented TAO timing synchronization system, including test results from 1:1 detector prototype with photon measurements.

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Track Classification: Trigger and Timing Distribution