TITLE:

Ensuring Clock Phase Repeatability by Preventing Loss of the 40.078 MHz Clock in Time-Critical Detectors: A Non-disruptive Clock Switching Approach

ABSTRACT: [up to 100 words]

At LHC phase 2, the CMS detector electronics need a precise clock to discriminate piled-up events. The backend electronics of the barrel electromagnetic calorimeter (ECAL) supplies the high-precision clock to the frontend. However, after a reset in the deserializer, the resulting phase of the recovered clock is not accurately repetitive. Therefore we have studied a case where the system seamlessly switches on-the-fly to a local clock so it keeps running when the link that delivers the clock to the backend, unlocks. This approach prevents the loss of the backend links towards the on-detector electronics ensuring clock phase repeatability.

SUMMARY: [up to 500 words]

In order to achieve the required physics performance [1], the CMS ECAL Barrel (EB), as well as other time critical subsystems at LHC Phase 2, needs to support the distribution of a high-precision clock. Although the current electronics can meet this requirement, the repeatability of the data-recovered-clock phase, after a SERDES reset, may vary up to 15 ps peak-to-peak between each stage in the system. Since the system consists of several stages in series, the total skew between channels, after a reconfiguration, could accumulate to multiple of 15 ps. This can in principle be calibrated with online physics data analysis at the beginning of each acquisition run however it introduces dead time. In addition the system is forced to be reconfigured at the start of a new run because the high speed link, from which they recover the “LHC machine” clock, is getting unlocked.

Therefore, we are proposing a non-disruptive clock switch technique that prevents the loss of the 40.078 MHz clock. The key point of the proposed method is that it avoids upsetting the rest of the system while the TClink [2] which drives the clock to the backend is being unlocked. Instead, the system switches on-the-fly to a local clock until the LHC clock becomes stable. We present the robustness of this scheme by constantly switching between two decoupled clock sources. For that we used two setups : a) The Advanced Processor Final (APxF) board together with the Advanced Timing Hub (ATH) card in order to demonstrate the impact of the scheme on several high speed links. b) The Barrel Calorimeter Processor V1 (BCP-V1) [3] together with the DAQ and Timing Hub P1 (DTH-P1) [4] and a slice of the phase-2 CMS ECAL Barrel Front-End electronics [5,6] (Figure 1) to demonstrate the stability of the future ECAL using the proposed scheme.

In general a random clock switch can cause a glitch which upsets the logic of the FPGA and its high speed links but in our approach we do switch the input of the jitter cleaner [7] which drives the FPGA. We are evaluating whether or not this switch causes an impact to the system or if the PLL of the jitter cleaner is able to filter the glitch. In particular we are presenting : a) The switching of the clock at several points of the system to understand how flexible this scheme can be, b) the behavior of the jitter cleaner at the moment switches (Figure 2), c) how close in frequency the two clocks must be in order to achieve the desired behavior, d) the impact on the system while emulating the rump-up of the LHC clock frequency, e) the bit error rate (BER) on several optical links while we are constantly switching the source of their reference clock (figure 3), and finally f) the impact on the logic of the FPGA as we clock-switch by testing an algorithm.

REFERENCES :

[1] Section 1.3, last paragraph, https://cds.cern.ch/record/2283187/files/CMS-TDR-015.pdf
[2] https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10029896
[3] https://iopscience.iop.org/article/10.1088/1748-0221/17/08/C08005/meta
[4] https://doi.org/10.22323/1.343.0129
[5] https://www.osti.gov/biblio/1831999
[6] https://inspirehep.net/literature/1749984
[7] https://www.skyworksinc.com/en/Products/Timing/High-Performance-Jitter-Attenuators/Si5395A

ABBREVIATIONS:

CMS	Compact Muon Solenoid
ECAL	Electromagnetic CALorimeter
EB	ECAL Barrel
CERN	Conseil Européen pour la Recherche Nucléaire
SERDES	SERialiser / DESerializer
DTH	Daq and Timing Hub
BCP	Barrel Calorimeter Processor
LHC	Large hadron Collider
PLL	Phase-Locked Loop
FPGA	Field Programmable Gate Array

FIGURES AND MEDIA :

Jitter cleaner output behavior when its switches its inout clock
https://cernbox.cern.ch/index.php/s/dlW5ciaJFiuoHRu

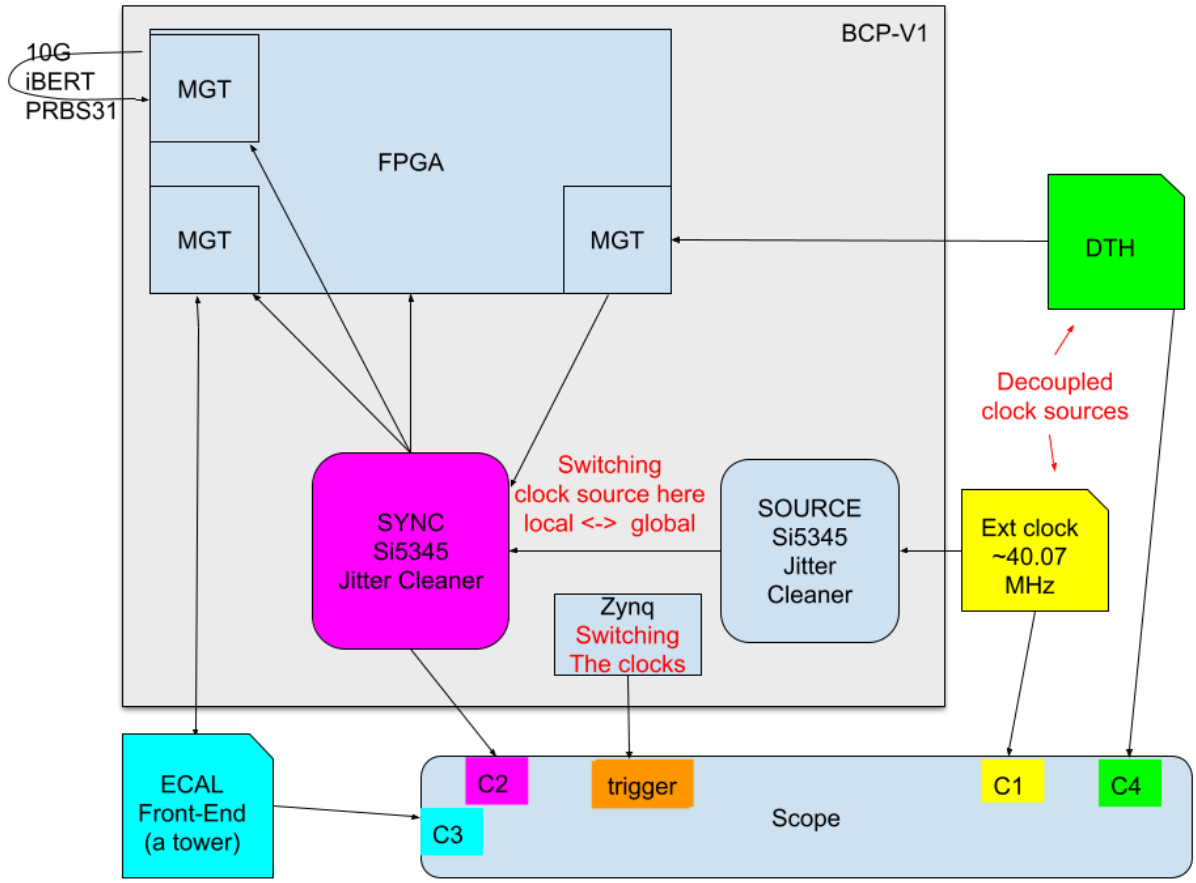


Figure 1 : Test setup

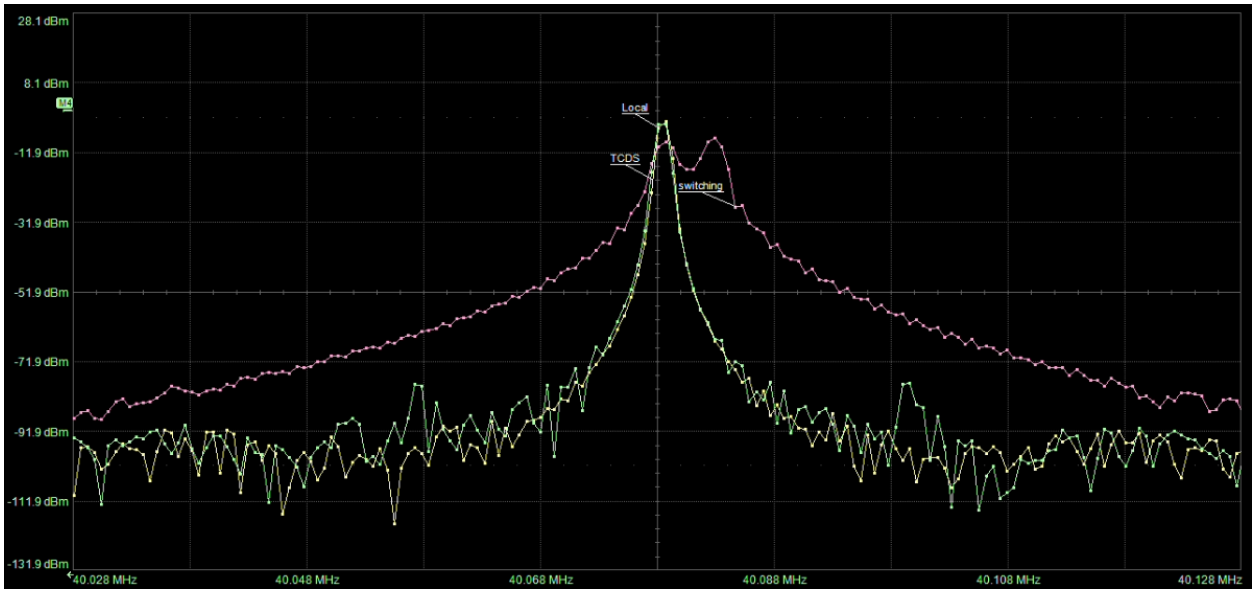
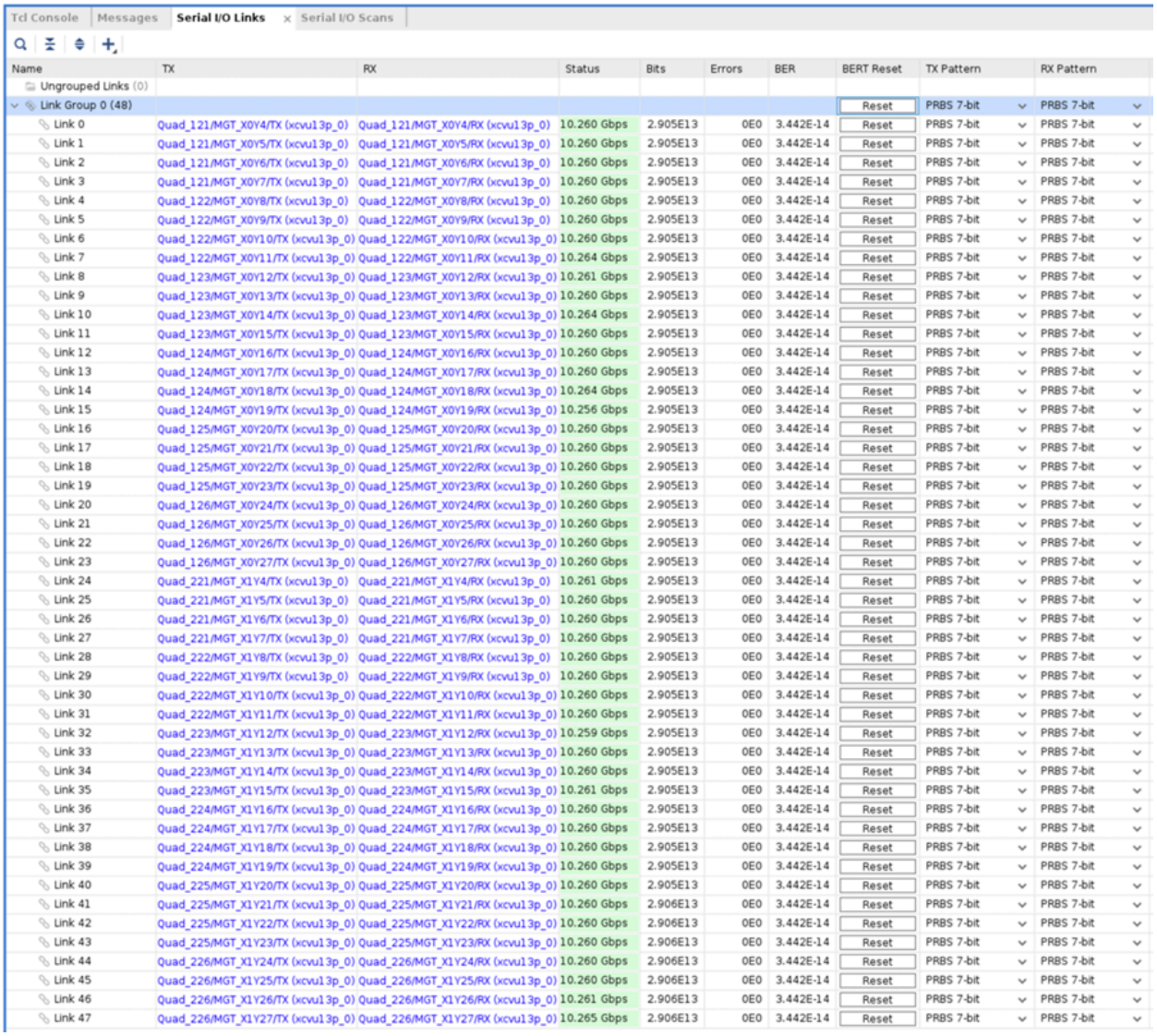


Figure 2 : FFT at the moment the jitter clean switches clocks (TCDS <-> local)



Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (48)							Reset	PRBS 7-bit	PRBS 7-bit
Link 0	Quad_121/MGT_X0Y4/TX (xcvu13p_0)	Quad_121/MGT_X0Y4/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 1	Quad_121/MGT_X0Y5/TX (xcvu13p_0)	Quad_121/MGT_X0Y5/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 2	Quad_121/MGT_X0Y6/TX (xcvu13p_0)	Quad_121/MGT_X0Y6/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 3	Quad_121/MGT_X0Y7/TX (xcvu13p_0)	Quad_121/MGT_X0Y7/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 4	Quad_122/MGT_X0Y8/TX (xcvu13p_0)	Quad_122/MGT_X0Y8/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 5	Quad_122/MGT_X0Y9/TX (xcvu13p_0)	Quad_122/MGT_X0Y9/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 6	Quad_122/MGT_X0Y10/TX (xcvu13p_0)	Quad_122/MGT_X0Y10/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 7	Quad_122/MGT_X0Y11/TX (xcvu13p_0)	Quad_122/MGT_X0Y11/RX (xcvu13p_0)	10.264 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 8	Quad_123/MGT_X0Y12/TX (xcvu13p_0)	Quad_123/MGT_X0Y12/RX (xcvu13p_0)	10.261 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 9	Quad_123/MGT_X0Y13/TX (xcvu13p_0)	Quad_123/MGT_X0Y13/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 10	Quad_123/MGT_X0Y14/TX (xcvu13p_0)	Quad_123/MGT_X0Y14/RX (xcvu13p_0)	10.264 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 11	Quad_123/MGT_X0Y15/TX (xcvu13p_0)	Quad_123/MGT_X0Y15/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 12	Quad_124/MGT_X0Y16/TX (xcvu13p_0)	Quad_124/MGT_X0Y16/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 13	Quad_124/MGT_X0Y17/TX (xcvu13p_0)	Quad_124/MGT_X0Y17/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 14	Quad_124/MGT_X0Y18/TX (xcvu13p_0)	Quad_124/MGT_X0Y18/RX (xcvu13p_0)	10.264 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 15	Quad_124/MGT_X0Y19/TX (xcvu13p_0)	Quad_124/MGT_X0Y19/RX (xcvu13p_0)	10.256 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 16	Quad_125/MGT_X0Y20/TX (xcvu13p_0)	Quad_125/MGT_X0Y20/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 17	Quad_125/MGT_X0Y21/TX (xcvu13p_0)	Quad_125/MGT_X0Y21/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 18	Quad_125/MGT_X0Y22/TX (xcvu13p_0)	Quad_125/MGT_X0Y22/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 19	Quad_125/MGT_X0Y23/TX (xcvu13p_0)	Quad_125/MGT_X0Y23/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 20	Quad_126/MGT_X0Y24/TX (xcvu13p_0)	Quad_126/MGT_X0Y24/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 21	Quad_126/MGT_X0Y25/TX (xcvu13p_0)	Quad_126/MGT_X0Y25/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 22	Quad_126/MGT_X0Y26/TX (xcvu13p_0)	Quad_126/MGT_X0Y26/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 23	Quad_126/MGT_X0Y27/TX (xcvu13p_0)	Quad_126/MGT_X0Y27/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 24	Quad_221/MGT_X1Y4/TX (xcvu13p_0)	Quad_221/MGT_X1Y4/RX (xcvu13p_0)	10.261 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 25	Quad_221/MGT_X1Y5/TX (xcvu13p_0)	Quad_221/MGT_X1Y5/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 26	Quad_221/MGT_X1Y6/TX (xcvu13p_0)	Quad_221/MGT_X1Y6/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 27	Quad_221/MGT_X1Y7/TX (xcvu13p_0)	Quad_221/MGT_X1Y7/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 28	Quad_222/MGT_X1Y8/TX (xcvu13p_0)	Quad_222/MGT_X1Y8/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 29	Quad_222/MGT_X1Y9/TX (xcvu13p_0)	Quad_222/MGT_X1Y9/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 30	Quad_222/MGT_X1Y10/TX (xcvu13p_0)	Quad_222/MGT_X1Y10/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 31	Quad_222/MGT_X1Y11/TX (xcvu13p_0)	Quad_222/MGT_X1Y11/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 32	Quad_223/MGT_X1Y12/TX (xcvu13p_0)	Quad_223/MGT_X1Y12/RX (xcvu13p_0)	10.259 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 33	Quad_223/MGT_X1Y13/TX (xcvu13p_0)	Quad_223/MGT_X1Y13/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 34	Quad_223/MGT_X1Y14/TX (xcvu13p_0)	Quad_223/MGT_X1Y14/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 35	Quad_223/MGT_X1Y15/TX (xcvu13p_0)	Quad_223/MGT_X1Y15/RX (xcvu13p_0)	10.261 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 36	Quad_224/MGT_X1Y16/TX (xcvu13p_0)	Quad_224/MGT_X1Y16/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 37	Quad_224/MGT_X1Y17/TX (xcvu13p_0)	Quad_224/MGT_X1Y17/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 38	Quad_224/MGT_X1Y18/TX (xcvu13p_0)	Quad_224/MGT_X1Y18/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 39	Quad_224/MGT_X1Y19/TX (xcvu13p_0)	Quad_224/MGT_X1Y19/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 40	Quad_225/MGT_X1Y20/TX (xcvu13p_0)	Quad_225/MGT_X1Y20/RX (xcvu13p_0)	10.260 Gbps	2.905E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 41	Quad_225/MGT_X1Y21/TX (xcvu13p_0)	Quad_225/MGT_X1Y21/RX (xcvu13p_0)	10.260 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 42	Quad_225/MGT_X1Y22/TX (xcvu13p_0)	Quad_225/MGT_X1Y22/RX (xcvu13p_0)	10.260 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 43	Quad_225/MGT_X1Y23/TX (xcvu13p_0)	Quad_225/MGT_X1Y23/RX (xcvu13p_0)	10.260 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 44	Quad_226/MGT_X1Y24/TX (xcvu13p_0)	Quad_226/MGT_X1Y24/RX (xcvu13p_0)	10.260 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 45	Quad_226/MGT_X1Y25/TX (xcvu13p_0)	Quad_226/MGT_X1Y25/RX (xcvu13p_0)	10.260 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 46	Quad_226/MGT_X1Y26/TX (xcvu13p_0)	Quad_226/MGT_X1Y26/RX (xcvu13p_0)	10.261 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 47	Quad_226/MGT_X1Y27/TX (xcvu13p_0)	Quad_226/MGT_X1Y27/RX (xcvu13p_0)	10.265 Gbps	2.906E13	0E0	3.442E-14	Reset	PRBS 7-bit	PRBS 7-bit

Figure 3 : APxF link BERs while switching LHC to local clocks