Ensuring Clock Phase Repeatability by Preventing Loss of the 40.078 MHz Clock in Time-Critical Detectors: **A Non-disruptive Clock Switching Approach**

- The APx consortium for the CMS collaboration -

N.Loukas[1], L.Moreno[2], T.Anderson[3], G.Cucciati[1], S.Goadhouse[3], T.Gorski[4], A.Svetek[4]

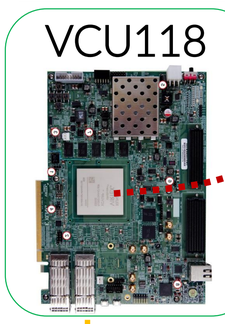
[1] University of Notre Dame [2] Princeton University
[3] University of Virginia [4] University of Wisconsin-Madison

Present Conditions

As measured, an up to 15 ps clock phase jump leads to a multiple of 15 ps accuracy error which **needs to be calibrated**. In principle, this can be done through Physics analysis. However, in case of for example the CMS-ECAL Upgrade for HL-LHC, this process must be applied to ~62k channels every time the system is in configure. This procedure would inevitably **introduce a dead-time**.

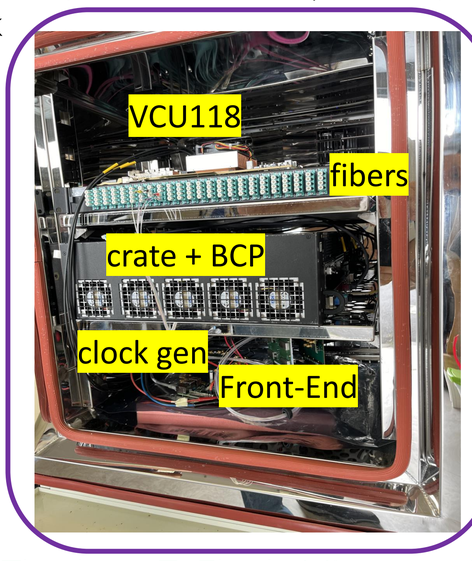
Experimental Setup

VCU118



Master
Distributes the LHC clock

Climatic Chamber
(Stable 0.1C temperature)



Master (VCU118) → BCPv1 → lpGBT → LiTeDTU

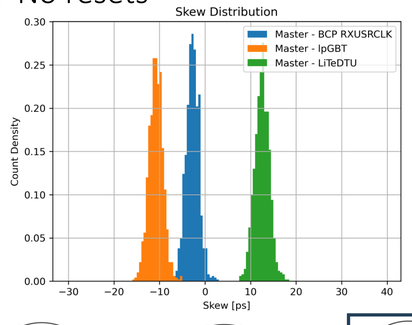
BCP-V1

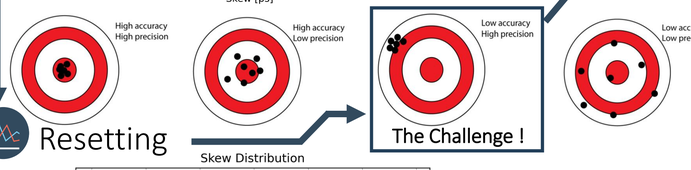
Slave
Recovers the LHC Clock

Thanks to Z. Eberle Minnesota Univ. student for taking measurements from the climatic chamber

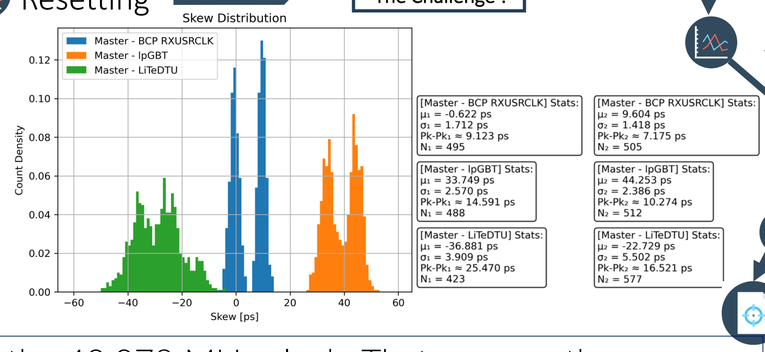
Recover clock measurements at different stages

No resets

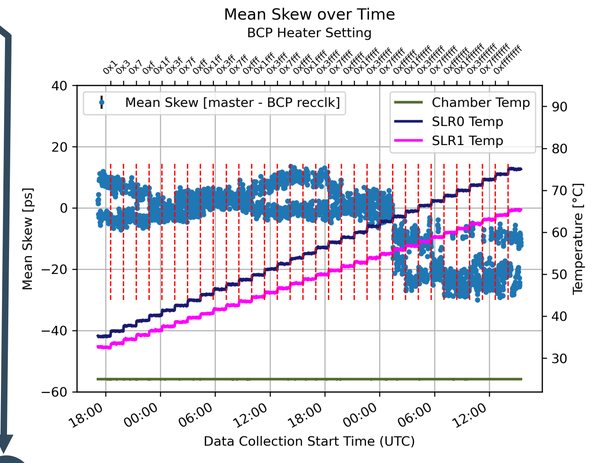




Resetting

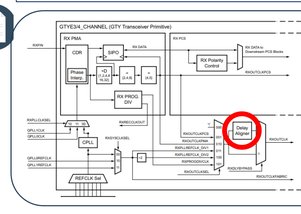


Resetting Slave FPGA every new measurement
Heating up the FPGA every 10th measurement



Accuracy depends on Temperature !

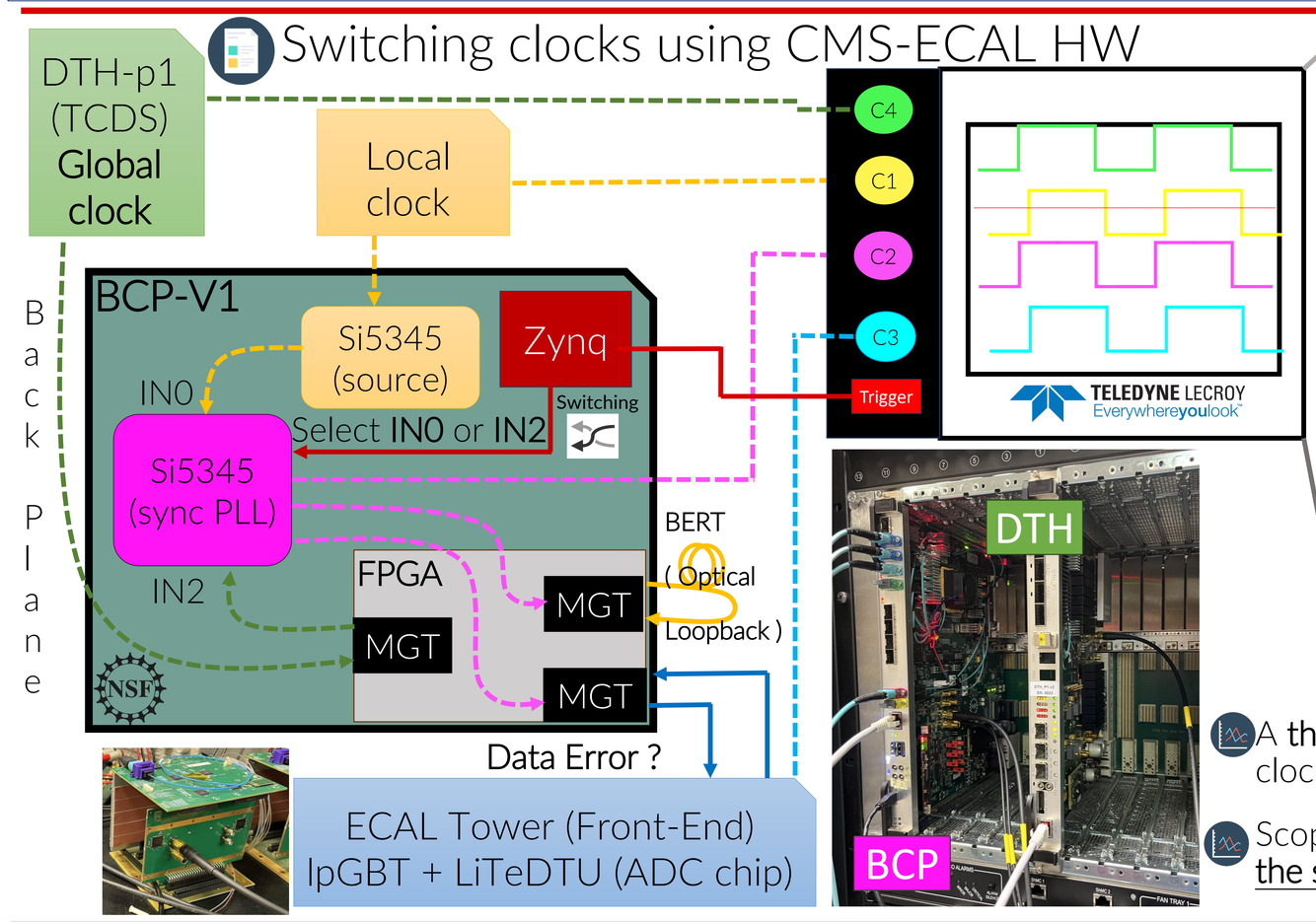
"Post-reset, FPGA temperature may cause up to **a 15 picosecond** deviation in the new clock phase

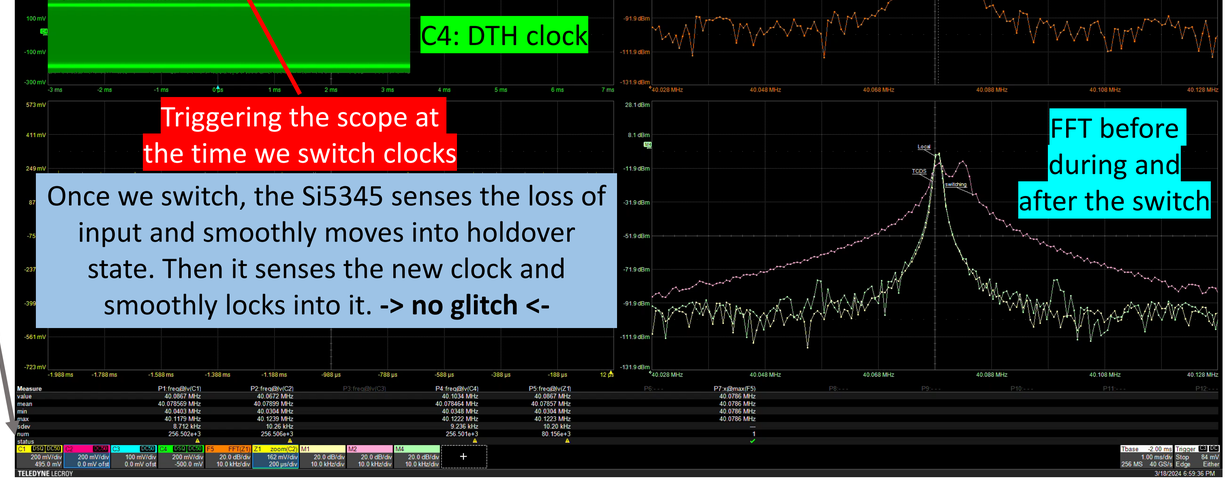


Deviation which is caused by a necessary feature of the AMD's FPGA receivers, the **Delay Aligner** (PVT circuit)

We are proposing a **non-disruptive clock switch technique that prevents the loss** of the 40.078 MHz clock. That ensures the accuracy of the clock distribution remains unchanged between data takings → Less often calibration → Less time lost during data taking.

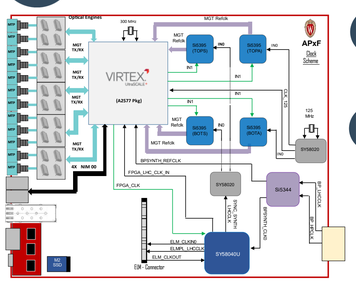
Switching clocks using CMS-ECAL HW

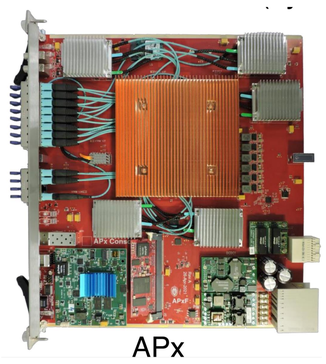




- A **thousand switches** between local and global clock were executed as the FPGA was running
- Scope is showing how the Si5345 is handling the switch (FFT analysis gives a third peak)
- Scope is showing C2, C3 (Front-End) switching between C1 & C4
- FE->BCP & BCP->BCP shows zero transmission errors (10^-16)

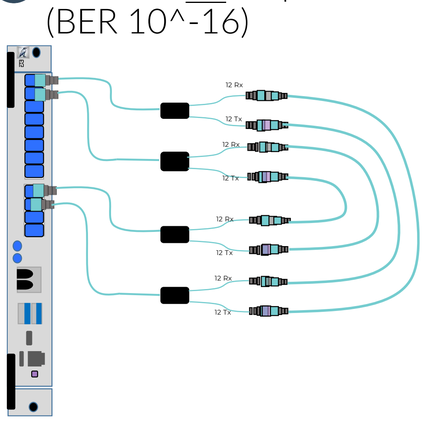
Using the APxF card (Similar PLL (si5395))





APx

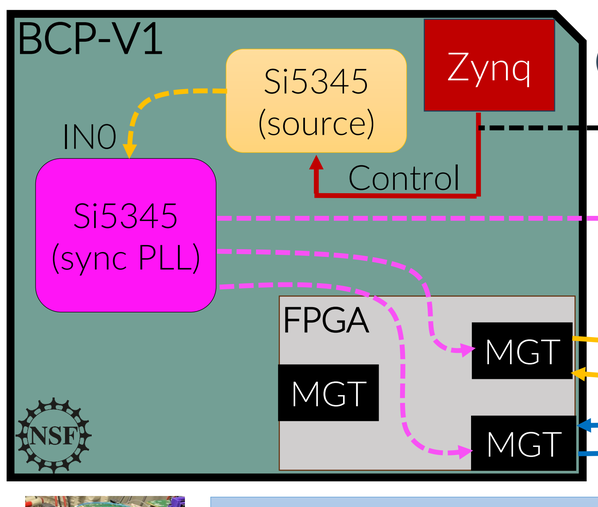
- Continuously switching between **backplane** and **local clocks** every 10 seconds
- BERT on 48 loopback links → no error (BER 10^-16)

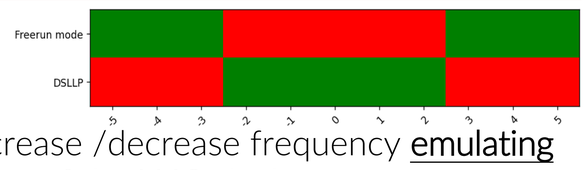


48 error free links BER 10^-16

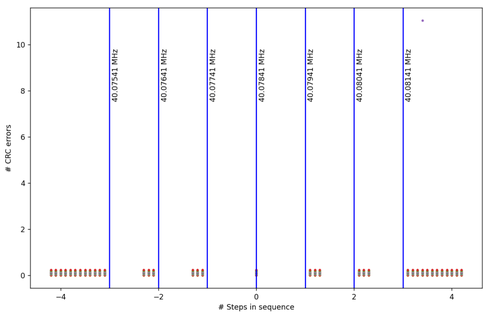
Lane Rate = 10.26047 Gbps
ClkRef = 320.64MHz

Ramping Up/Down clock frequency





- Dynamically increase /decrease frequency emulating ramping up/down of the LHC clock



- ± 1kHz steps from the central frequency
- When the PLL deviates no more than ± 2KHz from its configured frequency, the PLL remains locked and ECAL Front-End channels (up to 7 channels per optical link) run error free.

Conclusions:

- ✓ The distribution of the clock using FPGAs gives a precision within specs, but the accuracy varies with temperature.
- ✓ To overcome the need for continuous timing calibrations (introduction of dead time) caused by the loss of high-speed links, we propose keeping them running by sustaining transceivers reference clock using **A Non-disruptive Clock Switching Approach**.
- ✓ We demonstrated an on-the-fly multiple clock switches test at the input of system's PLL resulting no data error on transceivers.
- ✓ We stressed the system by rising the input frequency at the input of system's PLL and saw that we got zero errors from the Front-End.

References:

[1] The Phase-2 Upgrade of the CMS Barrel Calorimeters – Technical Design Report.
[2] The CMS Barrel Calorimeter Processor demonstrator (BCPv1) board evaluation – JINST (TWEPP2021)
[3] TCLink: A Fully Integrated Open Core for Timing Compensation in FPGA-Based High-Speed Links - IEEE
[4] The APx Board for the CMS Phase 2 L1 Calorimeter trigger: Testing and Performance
[5] CMS ECAL Upgrade Front End card: design and prototype test results - PoS (TWEPP2018)
[6] First measurements with the CMS DAQ and Timing Hub prototype-I

nikitas.loukas@cern.ch , lperezmo@cern.ch