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Ensuring Clock Phase Repeatability by Preventing Loss of the 40.078 MHz Clock in Time-Critical Detectors: A Non-disruptive Clock Switching Approach

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At LHC phase 2, the CMS detector electronics need a precise clock to discriminate piled-up events. The backend electronics of the barrel electromagnetic calorimeter (ECAL) supplies the high-precision clock to the frontend. However, after a reset in the deserializer, the resulting phase of the recovered clock is not accurately repetitive. Therefore we have studied a case where the system seamlessly switches on-the-fly to a local clock so it keeps running when the link that delivers the clock to the backend, unlocks. This approach prevents the loss of the backend links towards the on-detector electronics ensuring clock phase repeatability.

Summary (500 words)

In order to achieve the required physics performance [1], the CMS ECAL Barrel (EB), as well as other time critical subsystems at LHC Phase 2, needs to support the distribution of a high-precision clock. Although the current electronics can meet this requirement, the repeatability of the data-recovered-clock phase, after a SERDES reset, may vary up to 15 ps peak-to-peak between each stage in the system. Since the system consists of several stages in series, the total skew between channels, after a reconfiguration, could accumulate to multiple of 15 ps. This can in principle be calibrated with online physics data analysis at the beginning of each acquisition run however it introduces dead time. In addition the system is forced to be reconfigured at the start of a new run because the high speed link, from which they recover the "LHC machine"clock, is getting unlocked.

Therefore, we are proposing a non-disruptive clock switch technique that prevents the loss of the 40.078 MHz clock. The key point of the proposed method is that it avoids upsetting the rest of the system while the TClink [2] which drives the clock to the backend is being unlocked. Instead, the system switches on-the-fly to a local clock until the LHC clock becomes stable. We present the robustness of this scheme by constantly switching between two decoupled clock sources. For that we used two setups : a) The Advanced Processor Final (APxF) board together with the Advanced Timing Hub (ATH) card in order to demonstrate the impact of the scheme on several high speed links. b) The Barrel Calorimeter Processor V1 (BCP-V1) [3] together with the DAQ and Timing Hub P1 (DTH-P1) [4] and a slice of the phase-2 CMS ECAL Barrel Front-End electronics [5,6] (Figure 1) to demonstrate the stability of the future ECAL using the proposed scheme.

In general a random clock switch can cause a glitch which upsets the logic of the FPGA and its high speed links but in our approach we do switch the input of the jitter cleaner [7] which drives the FPGA. We are evaluating whether or not this switch causes an impact to the system or if the PLL of the jitter cleaner is able to filter the glitch. In particular we are presenting : a) The switching of the clock at several points of the system to understand how flexible this scheme can be, b) the behavior of the jitter cleaner at the moment switches (Figure 2), c) how close in frequency the two clocks must be in order to achieve the desired behavior, d) the impact on the system while emulating the rump-up of the LHC clock frequency, e) the bit error rate (BER) on several optical links while we are constantly switching the source of their reference clock (figure 3), and finally f) the impact on the logic of the FPGA as we clock-switch by testing an algorithm.

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