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CompactPCI-Serial Hardware Toolbox - Advancements towards Cost Effectiveness

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At PSI the future standard hardware platform based on CompactPCI-Serial is already widely spread for developments in several applications and is under discussion for use on all our accelerators.
With the focus on cost optimization smaller sub-racks are now part of the toolbox as well as rear boards with a subtle set of interfaces.
Based on the requirements of a Fill-Pattern Monitor for SLS 2.0 there is a near-term development of a CPCI-S front board on the way. Its generic design approach regarding board management and configuration interfaces shall enable easy-access for further application-specific developments.

Summary (500 words)

After the decision for CompactPCI-Serial standard as the future electronics hardware platform at PSI in the last few years a basic set of components has been developed and supplemented from COTS to cover already by now major functionality of the accelerators data acquisition and control systems.
To increase the acceptance from system responsible persons it is an important requirement to reduce the cost per sub-rack system with base functionality including power supply, communication interfaces, local processing capability and so on. The cost of our original empty crate is roughly CHF 4000 whereas our goal is to have a complete system for the same price including all relevant electronics necessary for a basic application.
The difficulty of this work was to find the best balance between hardware design flexibility and standardization. Similar considerations need to be taken during system design of most particle accelerators. In terms of reliability and maintainability our system design approach needs to lead into the direction of standardization and design reuse. The initially higher development effort will be paid off soon.
Beside the cost reduction by crate type variation and some subtle interface combinations per module nevertheless the sustainability of the platform will be dependent as well on the adaptability for application specific electronics.
Based on the requirements of a Fill-Pattern Monitor for SLS 2.0 the development status of such an application specific electronics is shown for the first time. Since the required electronics was not available as COTS the design is implemented as CPCI-S front card. The design approach bases on a generic board template which covers all necessary board management functionality and configuration interfaces. This design approach is intended to improve product quality and to minimize development efforts regarding hardware design as well as regarding optimized firmware adaptability.

Author: Mr GLOOR, Mathias (Paul Scherrer Institut)

Co-authors: Mr KALANTARI, Babak (Paul Scherrer Institut); Mr LINGUA, Jonas (Paul Scherrer Institut); Mr RIZZI, Mattia (Paul Scherrer Institut); Mr DITTER, Robin (Paul Scherrer Institut)

Presenter: Mr GLOOR, Mathias (Paul Scherrer Institut)

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