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Prototype of SiC beam monitor for the COMET experiment at J-PARC

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We developed a prototype of muon beam monitor for the COMET experiment. The detector consists of SiC PN-diodes and dedicated readout electronics. By tailing the 256 sensors in a matrix, the beam parameters extracted from this monitor are utilized for the essential background estimation. The electronics is designed in 65 nm CMOS, including 16 channels analog processor, ADC, PLL, and CML drivers. We demonstrated the functionality of the ASIC with a designed peaking time and voltage gain. We also tested the electronics at cryogenic temperature and confirmed stable behaviors down to -100 degree Celsius.

Summary (500 words)

We report on the muon beam monitor based on silicon carbide (SiC) sensors for the COMET (Coherent Muon to Electron Transition) experiment at J-PARC (Japan Proton Accelerator Research Complex). The experiment aims to search for neutrinoless muon-to-electron conversion processes in the field of the nucleus. The muon-beams are generated from the decay of pions, which are generated by the primary proton beam collisions with the pion-production target. The pions are then collected by the solenoidal field and transported to the main detector stage during the decay to muons. Muon-energetic electrons from muon decay are emitted from the muon-stopping target and detected by a cylindrical drift chamber (CDC).

The SiC muon beam monitor will be installed in a vacuum chamber and located in front of the muon-stopping target and the CDC. Since the radiation damage caused by continuous passing of the hig intensity muon beams, corresponding to 5 x 1013 neutron equivalent fluence, requires higher tolerance than standard n-type silicon sensors, SiC is an optimal option for the monitor. This monitor plays a key role in tracking the beam intensity and spatial stability of the secondary muon-beams, and is also used for the particle identification of the background. For this purpose, we are currently developing a prototype detector by arraying 256 PN diodes in a matrix form, combined with the dedicated front-end ASIC in 65nm CMOS technology.

The readout ASIC consists of 8 channels, in each channel contains a CSA, CRRC, and ADC for sampling the continuous waveforms from sensors. The internal clocks are generated in the on-chip PLL, and the serialized data are sent out via CML driver with pre-emphasis. In the lab. testing, we confirmed the basic functions, e.g., analog output with designed peaking time and gain, sampling ADC outputs, and clear eye diagram with 20 m wires. We also performed low-temperature test with liquid Nitrogen, to operate the ASIC in a pseudo-realistic condition. Although the PLL is not functioning below -120 degree Celsius, the sampling ADC outputs are working down to -100 degree, which is in a sufficiently low operating condition.

As for the SiC sensors, we fabricated the device with a reverse bias tolerance of over 3 kV in the prototyping facilities for power devices at Advanced Industrial Science and Technology in Japan. The thickness of the epitaxial layer is 52 um and a reverse bias of 1.2 kV is required from full depletion. To implement the sensors on the board, we designed a 100um thick flex capton board for to reduce the material budget. The prototype monitor is currently planned to be tested with muon pulse beam at J-PARC in June 2024. In this presentation, we will also discuss this test result and future prospect.

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