TWEPP-24

Topical Workshop on Electronics for Particle Physics

Glasgow, United Kingdom, 30 September – 4 October 2024

A. Kluge

Local and scientific committee

Local organisation

R. Bates (University of Glasgow, UK)
A. Blue (University of Glasgow, UK)
D. Maneuski (University of Glasgow, UK)
S. Naik (University of Glasgow, UK)
K. Walkingshaw Pass (University of Glasgow, UK)

Scientific organisation

A. Kluge (CERN, CH, Chair)
J. Alme (UIB, NO)
S. Baron (CERN, CH)
R. Bates (University of Glasgow, UK)
A. Boccardi (CERN, CH)
H. Chen (BNL, US)
S. Danzeca (CERN, CH)
C. Fernandez Bedoya (CIEMAT, ES)
M. French (RAL, UK)
D. Gascon (UB, ES)
P. Gui (SMU, US)
M. Hansen (CERN, CH)
C. G. Hu (IPHC-IN2P3, FR)
G. Lehmann Miotto (CERN, CH)
D. Maneuski (University of Glasgow, UK)
A. Ricci (CERN, CH, Secretary)
A. Rivetti (INFN, IT)
W. Snoeys (CERN, CH)
F. Vasey (CERN, CH)
K. Wyllie (CERN, CH)

Agenda

- TWEPP24 web page
  - https://indico.cern.ch/e/twepp2024
- Presentations start at 9:00
  - Invited/plenary presentations in
    - Grosvenor Suite Theatre
  - Parallel sessions in
    - Grosvenor Suite Theatre
    - Botanic Suite
- Poster sessions
  - 1.10 Tue & 3.10 Thu 16:40 – 18:00
- FPGA & Link user group
  - 2.10 Wed 17:15 – 18:30
- Micro electronics user group
  - 2.10 Wed 17:15 – 18:30
- Tutorial
  - 4.10 Fri 14:00
- Reception
  - 30.9 Mon 18:30
- Social activities
  - 1.10 Tue 14:00
- Conference Dinner
  - 2.10 Wed 19:00

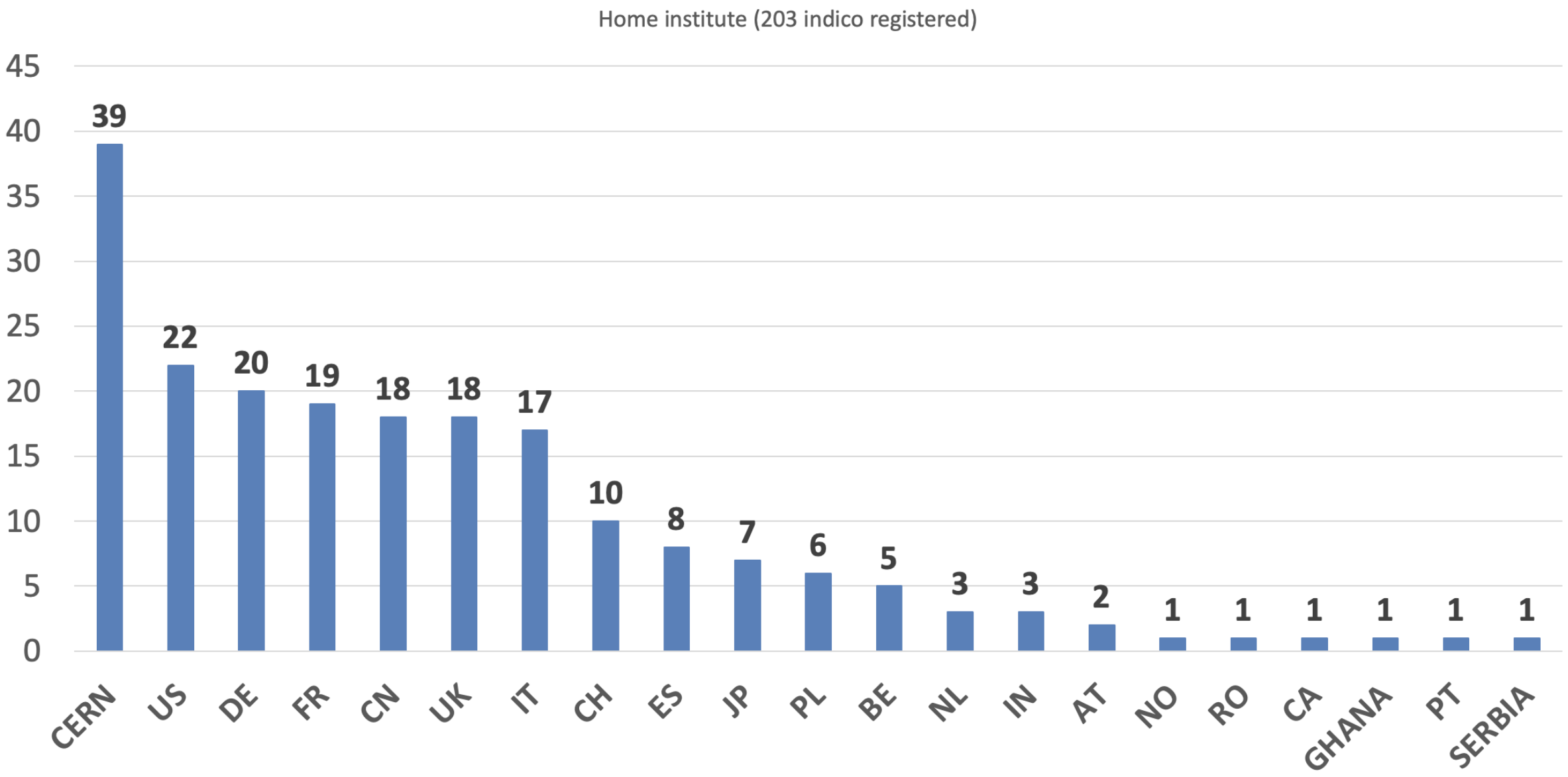
Presentations

- 72 oral presentations
  - 2 parallel sessions
- 87 poster presentations
- 5 invited plenary talks

- 213 registered attendees (indico)
  - 182 submitted abstracts, including 6 withdrawn & 18 rejected

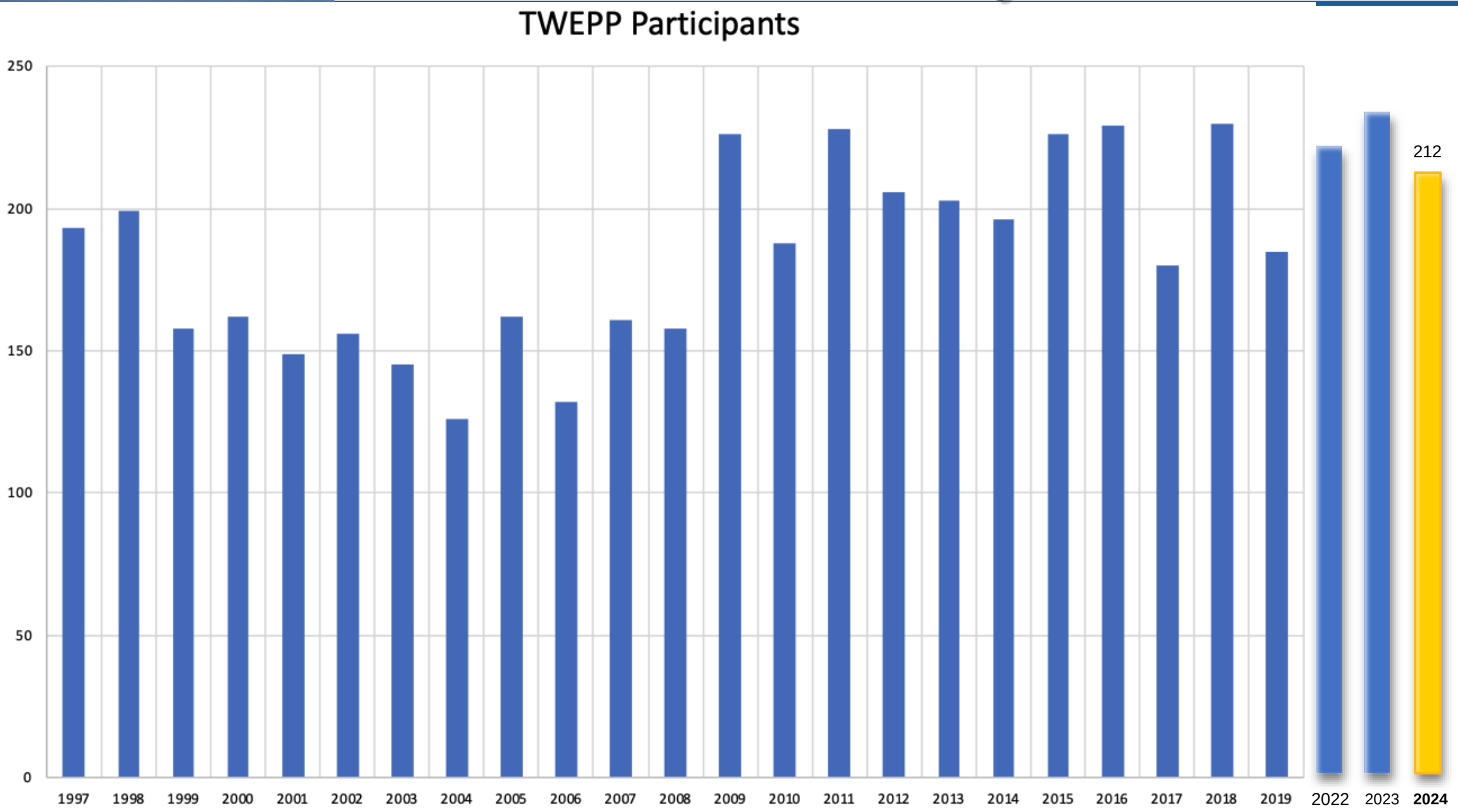
TWEPP 2024 participants

Participant Home institute



Participant travel departure

TWEPP attendance over years



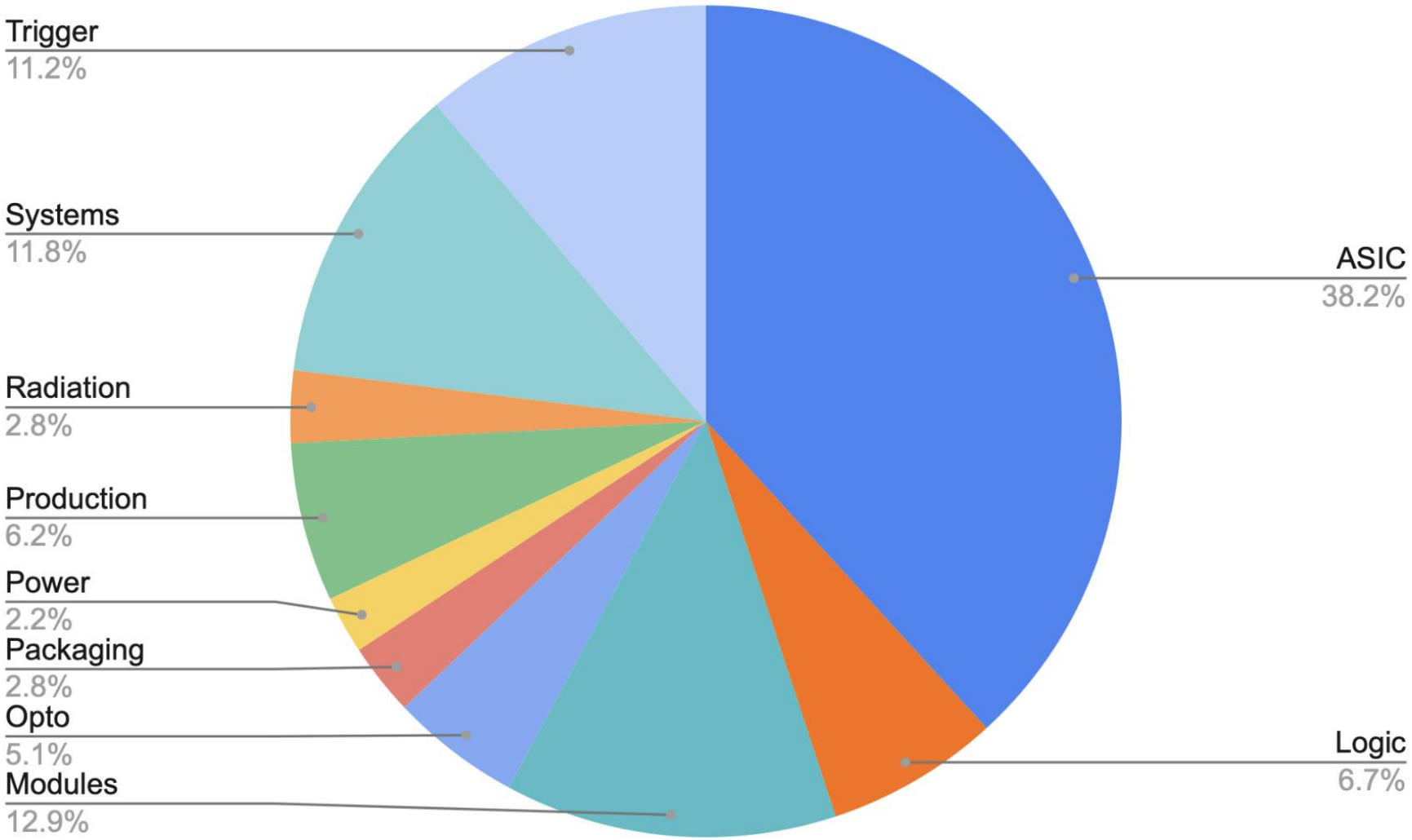
Tracks

TWEPP tracks

- **ASIC** (ASIC)
- **Optoelectronics & Links** (Links/Opto)
- **Packaging & Interconnects** (Packaging)
- **Power, Grounding & Shielding** (Power)
- **Production, Testing & Reliability** (Production)
- **Radiation-Tolerant Components & Systems** (Radiation)
- **Programmable Logic, Design & Verification Tools & Methods** (Logic)
  - FPGA, System-on-chip, Design Tools, Verification methods, Logic, Algorithms
- **PCB, module & component design** (Modules)
- **System design, description & operation** (System)
  - Design, architecture, planning, installation, integration, commissioning & operation experience of systems
- **Trigger & Timing Distribution** (Timing & Trigger)

Abstracts 2024

- **182 abstracts submitted**



TWEPP 2024 schedule

Schedule 2024: Mon/Tue

		Monday 30.9	Tuesday, 1.10											
Start (tue-fri)	Endn (tue-fri)	Salle 1	Salle 1								Salle 2			
		Title and speaker	Chair 1	Chair 2	Track	#	ID	Title	Chair 1	Chair 2	Track	#	ID	Title
9:00	9:16		D. Gascon	M. French	ASIC	1	12	ECON-D and ECON-T: Design and Production Testing	S. Baron	A. Boccarc	Trigger	1	28	High-Precision Timing Distribution for the ATLAS Phase-II Central Trigger Upgrade
9:20	9:36		D. Gascon	M. French	ASIC	2	97	An Integer-N Frequency Synthesizer for Flexible On-Chip Clock Generation	S. Baron	A. Boccarc	Trigger	2	85	An FPGA-agnostic system for achieving picosecond-level phase determinism in timing distribution links for High Energy Physics Experiments
9:40	9:56		D. Gascon	M. French	ASIC	3	108	Functional Verification for Endcap Concentrator ASICs in the High-Granularity Calorimeter Upgrade of CMS	S. Baron	A. Boccarc	Trigger	3	82	Phase Stability Compliancy Testing of a White Rabbit Based Solution for the LHC RF and Timing Distribution Backbone Upgrade
10:00	10:30	Registration	Break											
10:30	11:15		K. Wyllie		Invited	1		Quantum Technology for Sensing and Timing Applicat	speaker	Douglas Paul/Glasgow				
11:20	11:36		M. French	D. Gascon	ASIC	4	134	SOCRATES: a Radiation-Tolerant SoC Generator Framework	A. Boccarc	S. Baron	Trigger	4	75	System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC
11:40	11:56		M. French	D. Gascon	ASIC	5	156	Event-Driven Readout Development: Testing of the EDWARD65P1 Chip with Integrated Event Generators	A. Boccarc	S. Baron	Trigger	5	80	New Small Wheel Trigger Processor Electronics
12:00	12:16		M. French	D. Gascon	ASIC	6	86	Design update and characterization of sub-10ps TDC ASIC in 28nm for future 4D trackers.	A. Boccarc	S. Baron	Trigger	6	137	Triggering on muon showers in the Barrel Muon Trigger of the CMS experiment for the HL-LHC upgrades
12:20	14:00		Break											
14:00	14:16	14:00 - 14:20 Introduction - Alexander Kluge	D. Gascon	P. Gui	ASIC	7	29	FAST3 asic: front-end electronic with ps resolution, designed for thin LGADs read-out	S. Baron	C. Bedoya	Trigger	7	49	Firmware implementation of Phase-2 Overlap Muon Track Finder algorithm for CMS Level-1 trigger
14:20	14:36	14:20 - 14:50	D. Gascon	P. Gui	ASIC	8	59	The testing and performance of the ETROC2 for CMS MTD Endcap Timing Layer (ETL) upgrade	S. Baron	C. Bedoya	Trigger	8	113	FPGA implementation of the HL-LHC CMS Drift Tubes Level-1 Trigger Algorithm
14:40	14:56	14:50 - 15:20	D. Gascon	P. Gui	ASIC	9	140	First results on the Ignite-0 test ASIC in CMOS 28-nm technology	S. Baron	C. Bedoya	Trigger	9	95	Design and deployment of a fast neural network for measuring the properties of muons originating from displaced vertices in the CMS Endcap Muon Track Finder
15:00	15:30	15:20 - 15:40 Break	Break											
15:30	15:46	15:40 - 16:25	A. Kluge		Invited	2		Accelerator technologies, specifications and challeng	speaker	E. Gschwendtner				
15:50	16:06	16:25 - 17:10												
16:20	16:36	17:10 - 17:35	D. Gascon	P. Gui	ASIC	10	158	Design of 28nm readout ASIC prototype for 3D-integrated LGAD sensors	S. Baron	C. Bedoya	Trigger	9	157	The APx Board for the CMS Phase 2 L1 Calorimeter trigger: Testing and Performance
16:40	16:56	17:35 - 17:45 Practical Information	Poster											
17:00	18:00		Poster											
		Reception 18:30	Social activity 1830											

Schedule 2024: Wed

Wednesday, 2.10

Salle 1						Salle 2					
Chair 1	Chair 2	Track	#	ID	Title	Chair 1	Chair 2	Track	#	ID	Title
A. Rivetti	C. G. Hu	ASIC	11	120	Development of the MOSAIX chip for the ALICE ITS3 upgrade	M. Hansen	H. Chen	Power	1	34	Next generation fully integrated DCDC converters for HEP applications in 28nm technology
A. Rivetti	C. G. Hu	ASIC	12	20	Yield Characterisation and Failure Analysis of the Monolithic Stitched Sensor MOSS for ALICE ITS3	M. Hansen	H. Chen	Power	2	81	Radiation and magnetic field qualification of LVPS – a unified 12 VDC power source for the CMS detector.
A. Rivetti	C. G. Hu	ASIC	13	56	Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3	M. Hansen	H. Chen	Power	8	15	Optimized Rad-Hard DC/DC Converters for HEP Applications
					Break						
F. Vasey		Invited	3	0	years of CERN, how has particle physics electronic	speaker	Geoffrey Hall				
P. Gui	M. French	ASIC	14	44	Investigation of non-idealities of pulsing circuitry in the ALICE ITS3 MOSS monolithic sensor	C. Bedoya	G. Lehmanr	Radiation	1	3	CMS ECAL on-detector readout electronics radiation tests
P. Gui	M. French	ASIC	15	172	Design and characterization of the monolithic ASIC for the pre-shower upgrade of the FASER experiment	C. Bedoya	G. Lehmanr	Radiation	2	21	Rad-Hard Readout System for Timepix3 Hybrid Pixel Detectors
P. Gui	M. French	ASIC	16	169	RD50-MPW4: A thin backside-biased High Voltage CMOS pixel chip for high radiation tolerance	C. Bedoya	G. Lehmanr	Radiation	3	148	RadMon: a versatile, integrated radiation monitoring system for accelerators and experiments electronics at CERN
					Break						
J. Alme	K. Wyllie	Modules	1	152	Design, Construction, and Testing of the APOLLO ATCA Blades for Use at the HL-LHC	A. Boccardi	C. Bedoya	Logic	1	26	Development of methodology and implementation of SoC-based compact single-board validation system for the ATLAS Phase-II level-0 muon trigger system
J. Alme	K. Wyllie	Modules	2	6	Phase-2 CMS DAQ -- Growing from prototype boards to demonstrator systems	A. Boccardi	C. Bedoya	Logic	2	45	A Low-Cost, Low-Power Media Converter Solution for Next-Generation Detector Readout Systems
J. Alme	K. Wyllie	Modules	3	165	Technical challenges designing a prototype common readout board for LHCb future upgrades	A. Boccardi	C. Bedoya	Logic	3	121	Mitigating Multiple Single-Event Upsets During Deep Neural Network Inference using Fault-Aware Training
					Break						
K. Wyllie	J. Alme	Modules	4	149	Development of readout electronics for a high-speed event-driven neutron imaging detector based on Timepix4	C. Bedoya	A. Boccardi	Logic	4	132	Applications of PixESL framework on pixel detectors for High Energy Physics experiments
K. Wyllie	J. Alme	Modules	5	142	Design, test and performance of a PicoTDC based board	C. Bedoya	A. Boccardi	Logic	5	145	Improvements for the implementation of RDMA on FPGA devices
					Usergroup1&2&3&4						
					Usergroup1&2&3&4						
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Conference Dinner 19:00

Schedule 2024: Thu

Thursday, 3.10

Salle 1						Salle 2					
Chair 1	Chair 2	Track	#	ID	Title	Chair 1	Chair 2	Track	#	ID	Title
C. G. Hu	A. Rivetti	ASIC	17	64	HKROC: an integrated readout chip designed to facilitate the readout of a large number of photomultiplier tubes for the next generation of neutrino experiments	A. Kluge	G. Lehmanr	Systems	1	22	HGCAL SiPM-on-Tile Full-Stack Integration with the Serenity-S Phase-2 DAQ Hardware
C. G. Hu	A. Rivetti	ASIC	18	66	Implementation and performance of ALTIROC3 readout ASIC for ATLAS HGTD timing detector	A. Kluge	G. Lehmanr	Systems	2	2	Bandwidth induced bias on Time Of Arrival (ToA) uncertainty and optimal operating poin definition for fast timing silicon technologies
C. G. Hu	A. Rivetti	ASIC	19	73	Cleopatra : A 12-Channel Recycling Integrator ASIC for the Readout of Hydrogenated Amorphous Silicon Detectors in Radiotherapy Dosimetry	A. Kluge	G. Lehmanr	Systems	3	5	Performance of the CMS GE1/1 system at LHC Run-3 and prospects of the future ME0 system
						Break					
A. Rivetti		Invited	4		ng electronic boundaries with 3D integration and advanced	speaker	Parceval Coudrain (CEA/LETI)				
A. Rivetti	C. G. Hu	ASIC	20	83	UKRI-MPW1: an HV-CMOS pixel sensor for high radiation tolerance	G. Lehmanr	H. Chen	Systems	4	53	DAMIC-M electronics system, status and firs results.
A. Rivetti	C. G. Hu	ASIC	21	144	The Energy Measurement ASIC for the Upgrade II in the LHCb Calorimeter Detector	G. Lehmanr	H. Chen	Systems	5	115	Electrical measurement and read-out performance of a realistic, full-scale system bench of CMS Inner Tracker Barrel for HL-LHC
A. Rivetti	C. G. Hu	ASIC	22	50	A Wide-Temperature-Range SAR ADC in Open-Source CMOS Technology	G. Lehmanr	H. Chen	Systems	6	112	The services chain for the upgrade of the Inner Tracker Pixel detector of the ATLAS experiment – full services from pixel modules to optical readout for the Outer Barrel sub-system
					Break						
F. Vasey	S. Baron	Opto	1	17	Silicon photonic components on the COTTONTAIL chip	G. Lehmanr	J. Alme	Systems	7	147	Readout Electronics for Neutron Detectors a CSNS and CSNS-II: Challenges, Solutions, and Progress
F. Vasey	S. Baron	Opto	2	63	Silicon Photonics Circuits for the optical readout of CERN detectors	G. Lehmanr	J. Alme	Systems	8	161	Advancing Space Telescope Capabilities: SiPM-based UV-Light Detection for Ultra High Energy Cosmic Rays
F. Vasey	S. Baron	Opto	3	153	Ionizing Radiation Damage in Silicon Photonic Ring Modulators and Silicon-Germanium Electro-Absorption Modulators	G. Lehmanr	J. Alme	Systems	9	177	Readout Electronics for dN/dx Measurement of the Drift Chamber for CEPC R&D
					Break						
F. Vasey		Invited	5		the development of cryogenic CMOS electronics for	speaker	Manuel Rolo (INFN)				
F. Vasey	S. Baron	Opto	4	183	CWDM-based radiation-tolerant high-speed optical links	A. Kluge	J. Alme	Systems	10	38	Prototype of SiC beam monitor for the COMET experiment at J-PARC
					Poster						
					Poster						
					Hunterian Museum and Art Gallery 18:30 & comittee dinner 20:30						

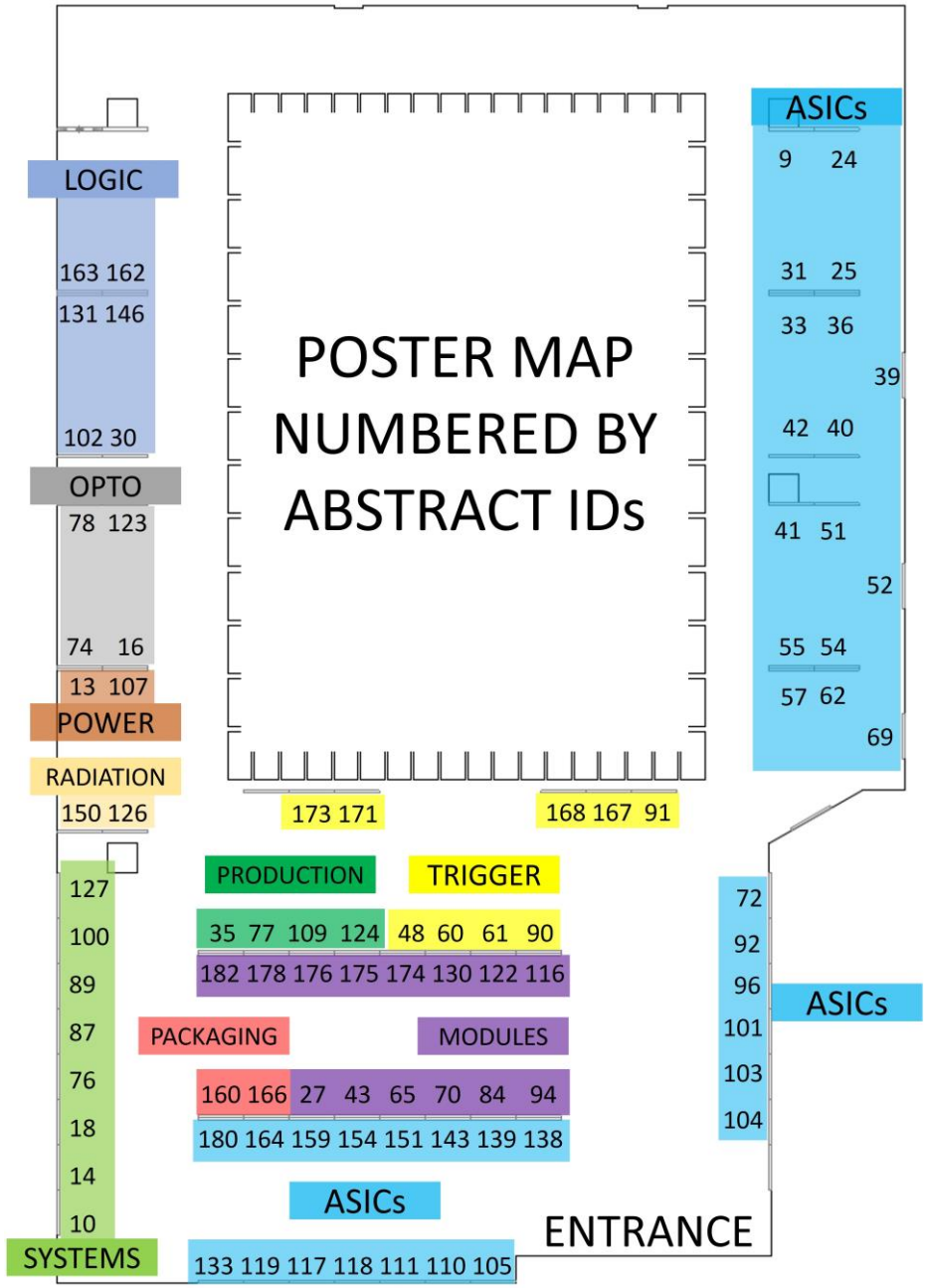
Schedule 2024: Fri

Friday, 4.10

Salle 1						Salle 2					
Chair 1	Chair 2	Track	#	ID	Title	Chair 1	Chair 2	Track	#	ID	Title
K. Wyllie	M. Hansen	Packaging	1	46	3D Integration of Pixel Readout Chips using Through-Silicon-Vias	H. Chen	F. Vasey	Production	1	71	Performance tests and hardware qualification of the FEBs for the novel Super-Fine Grained Detector of T2K Phase II
K. Wyllie	M. Hansen	Packaging	2	135	Development of a novel low-mass module flex PCB using nano-wire-based flip-chip interconnection	H. Chen	F. Vasey	Production	2	32	Hybrids pre-production results for the CMS Outer Tracker Phase-2 Upgrade
K. Wyllie	M. Hansen	Packaging	3	141	Design, Production and Testing of ATLAS ITk Strip Bus Tapes	H. Chen	F. Vasey	Production	3	58	Insights gained from test system preparation for the hybrids production for the CMS Outer Tracker Phase-2 Upgrade.
Break											
10:30-10:50	10:50-11:10										
J. Alme	K. Wyllie	Modules	6	79	Design and Implementation of a Compact Analog Constant Fraction Discriminator for High-Resolution Timing in Gamma-Ray Spectroscopy	F. Vasey	H. Chen	Production	4	93	Characterization of Pre-Production Petals for the ATLAS Inner Tracker Strip Detector
J. Alme	K. Wyllie	Modules	7	125	KALYPSO LGAD - A MHz repetition rate line camera based on trench isolated low gain avalanche detector	F. Vasey	H. Chen	Production	5	68	Production of flex circuits for the ATLAS ITk Pixel Outer Barrel
Closing											
Break											
Tutorial											

Poster sessions

Poster sessions



Invited plenary talks

TWEPP 2024

- 5 invited talks each 45’
  - **In the 70 years of CERN, how has particle physics electronics evolved?**
    - Geoffrey Hall (Imperial College)
  - **Accelerator technologies, specifications and challenges**
    - Edda Gschwendtner (CERN)
  - **Quantum Technology for Sensing and Timing Applications**
    - Douglas Paul (Glasgow)
  - **Redefining electronic boundaries with 3D integration and advanced packaging**
    - Parceval Coudrain (CEA/LETI)
  - **An outlook to the development of cryogenic CMOS electronics for particle physics**
    - Manuel Rolo (INFN Torino)

Tutorial

Tutorial

- Cadence
  - **Signal integrity optimisation**
    - via simulation of the integrated circuit, PCB, connector, cable and system level
      - Electrical thermal co-simulation at PCB/IC package leve
      - Optimisation of EMC at PCB/IC package level
      - Design of robust power supply network at PCB/IC package level
      - Simulation of DDR routing at PCB/IC package level
      - Simulation of High-Speed serial link routing at PCB/IC package level
      - Analysis of a complete system – PCB/package/connector/cable
  - https://indico.cern.ch/event/1381495/page/32655-tutorial
  - **If you are interested but have not registered, please contact twepp@cern.ch**

Schedule App

TWEPP24 app

- **Mobile app → access to TWEPP schedule**

Type '**Conference4me**' in
Play Store/iTunes App Store/Windows Phone Store
or scan the code below

Oral Presentation award

Oral presentation awards

- Oral presentation award
- Friday, October 4, 11:10
- Referees
  - TWEPP scientific committee

Proceedings

Proceedings

- **JINST - https://jinst.sissa.it/jinst/**
  - **submission using JINST web based infra structure**
  - **organized as non-open access, no cost for author**
    - JINST offers open access, cost would need to be covered by author/institute/experiment
    - or author institute has agreement with JINST
  - **each paper assigned to 2 referees**
    - from TWEPP scientific committee
- **Length**
  - **number of pages must not exceed 5 pages**
    - **(excluding the title & abstract page & references)** for both oral and poster contributions
- **Deadline November 3, 2024, 23:59 CET→ no extension**
- **Instruction to authors**
  - **TWEPP web page**
    - https://indico.cern.ch/event/1255624/page/28781-proceedings-instruction-for-authors
  - **review will be strict**
    - 2 rounds of review
      - do not waste 1 round with insufficient formatting, structure, writing style or length

Proceeding recommendations

- Describe specifications and implementation challenges arising from these specifications
- Use quantitative (numbers) statements, comparisons and performance figures
  - and do not give statements that a given parameter needs to be high or low
- Limit introduction to relevant information to work you describe in the paper
  - Repetition of standards phrases about the LHC luminosity upgrade might only be useful if information is set in direct context to your work
- Describe work/challenge/complexity so that it can be understood by a scientist outside your field of competence
  - in contrast to writing an experiment collaboration note
- Describe why your work is worth being presented at a scientific/technical workshop
- Describe challenges/difficulties during implementation and how they were solved or why not
- Check quality of formatting, language, style and length

Upload your presentation & poster

TWEPP-24

Topical Workshop on Electronics for Particle Physics

Glasgow, United Kingdom, 30 September – 4 October 2024

Deadline for abstracts: 30 April 2024

The workshop covers all aspects of electronic systems, components and instrumentation for particle and astro-particle physics such as: electronics for particle detection, triggering, data-acquisition systems, accelerator and beam instrumentation.

Operational experience in electronic systems and R&D in electronics for LHC, High Luminosity LHC, FAIR, neutrino facilities and other present or future accelerator projects are the major focus of the workshop.

For information
https://indico.cern.ch/e/twepp2024
https://www.ppe.gla.ac.uk/twepp24

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F. Vasey (CERN, CH)
K. Wyllie (CERN, CH)

University of Glasgow

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