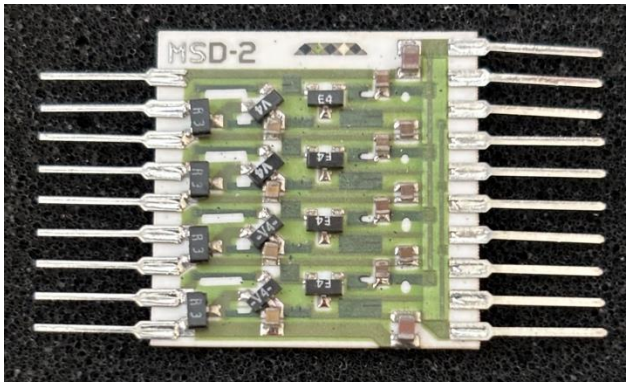
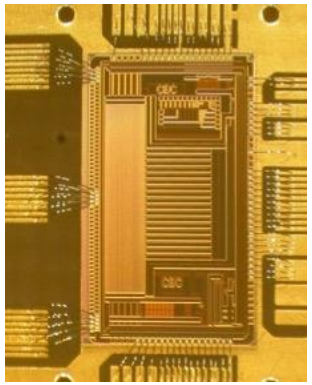




Electronics for particle physics – how it has evolved in the 70 years of CERN

October 2024

Geoff Hall

Imperial College London

Overview

- I was invited to give a talk on 70 years of CERN electronics – but why?
  - I am not an historian, or an electronics engineer, but just old (enough?)
- Nevertheless, the subject was tempting.
  - I have tried to select some relevant material BUT
  - No claim to be a rigorous historical account with all contributors properly cited
    - this is potentially a huge subject impossible to do full justice to
  - I include some material I am familiar with and omit others
    - especially e.g. power supplies, specialist accelerator systems, computing, …
- Declaration of interest
  - Now, many years of involvement in this area, mainly for the CMS experiment
    - But I am not an electronic designer or even, any longer, a hands-on user
    - despite that I seem to have dipped my toes in a lot of (hot, sometimes) water
    - Heavily involved in LEB, LERC, LECC, TWEPP for many years…

Expect some opinions – which you may not share

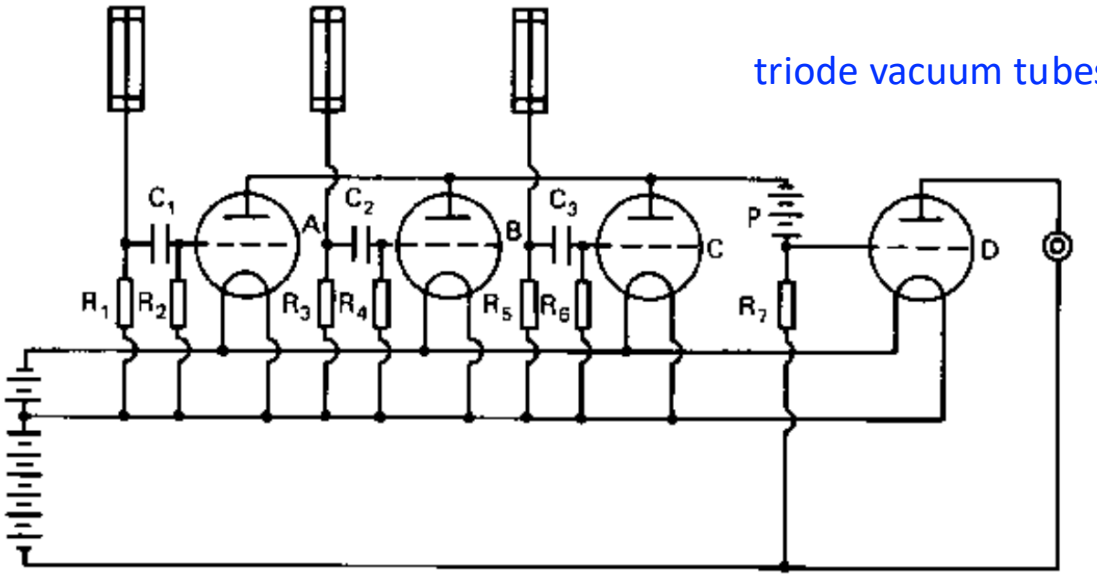
Some of my history

- I started school in 1954
  - Sadly, no electronics courses offered
- Physics degrees 1968-1974
  - Y2 UG bipolar electronics using partial differential equations – v. obscure!
- SLAC: triggered rapid-cycling bubble chamber 1975-1982
  - the charm era, but only our final experiment observed charm ~1981
    - γp –> charm : < 100 events from ~2M triggered photos
    - triggered on tracks using NOVA mini-computer, algorithm in assembler code (2ms)
    - various hardware projects, including Cerenkov counters with PM readout
- NA14': first UK project to use silicon detectors, started ~1981: γp –> charm
  - I finally began to learn some electronics!
  - Our first silicon microstrips manufactured by Micron Semiconductor
    - initially very primitive, based on MOS process devised by J Kemmer, read out by MSD2 (Jarron/Goyot)
  - UK contribution to NA14' cancelled before telescope operated! (but experiment continued)
    - supposedly insufficient publications by previous members in one of regular UK funding crises
  - I became involved with many silicon detector projects, leading to SSC & LHC preparations
    - along the way drift photodiodes immersed in LXe, Laben amplifiers & GH shaping amps – actually worked!
    - radiation damage studies, initially of silicon, then FE electronics – RD20 DRDC project (1991), then CMS APV

Me, celebrating CERN inauguration

Pre-CERN

- When did electronics developments begin, and for what purpose?
  - Rossi (1930): coincidence circuit, triggering using Geiger counters and valves
    - Quickly adopted, e.g. Blackett & Occhialini (1932) triggered cloud chamber in a magnetic field to observe the positron (but scooped by Anderson to publish)
- Rossi, B "Method of Registering Multiple Simultaneous Impulses of Several Geiger Counters", Nature 1930, 125: 636.



triode vacuum tubes

"The consequent variation of the anode current was detected acoustically by a telephone."

Rossi's coincidence circuit, the first fast electronic coincidence circuit of the parallel type, became essential in cosmic-ray research. It allowed the simultaneous registration of electrical pulses from any number of Geiger-Mü ller counters and had a resolving time of 10 -3 second, an order of magnitude faster than Walther Bothe's

Rossi the pioneer – a couple of examples

- Invention of the electronic trigger

tool for cosmic-ray experiments when used in coincidence arrangements. The coincidence technique,** first used by Hans Geiger and Walther Bothe in 1924 to verify that Compton scattering produces a recoil electron simultaneously with the scattered γ-ray, achieved its full potentialities only in connection with the invention of electronic circuits at the beginning of 1930s. From then on, in conjunction with the invention of new sophisticated detectors,

** Bothe and Geiger defined a coincidence using electrometers recorded on fast photographic film - when both counters showed a signal within a 1 ms interval

Rotblat (1940) measured resolving times of 6 μs – 1 ms with Rossi's circuit

- Time to Amplitude Converter

In the fall of 1940 Hans Bethe obtained for Rossi an appointment as associate professor at Cornell University. With his student, Norris Nereson, Rossi made a precise measurement of the decay curve of the mesotron at rest, the first such measurement of a fundamental particle. Their setup employed a combination of coincidence and anticoincidence circuits that signaled when a mesotron stopped in a block of graphite, and an *electronic chronometer* to measure the time interval between the stop signal and the pulse produced by the electron ejected in decay of the mesotron. Because of its potential military value, publication of the chronometer, now called a time-to-amplitude converter or TAC, was withheld until after the war.[21] Figure 6 shows the final result of

Other developments

Wynn-Williams (1931) *A Thyratron "scale of two" automatic counter*. Proc. Roy. Soc A 136, 312

allows to record numbers of events with "mechanical counting meter" (octal)

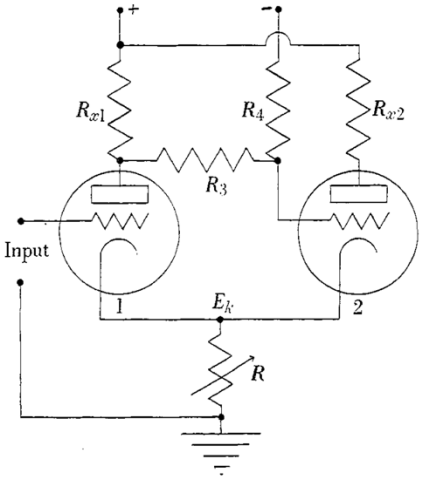


Fig. 1. Thermionic trigger circuit

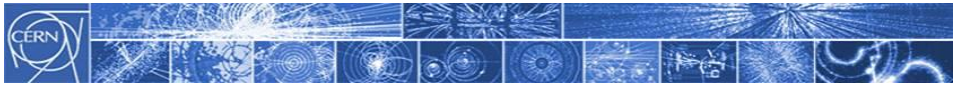
Schmitt (1937) *A thermionic trigger* J. Sci. Instrum. 15 24

Threshold crossing circuit using valves -> 1-bit A-D conversion

A STABLE NINETY-NINE CHANNEL PULSE AMPLITUDE ANALYSER FOR SLOW COUNTING

By D. H. WILKINSON

Received 18 October 1949



Nuclear and particle physics experiments need most advanced technologies for progress

In 1948 Wilkinson introduced signal digitization for nuclear spectrometry

D.H. Wilkinson Proc.Cambridge Phil.Soc.46(1950) 508

Emilio Gatti improved it further (1949)

using 2 telephone registers

99 channel digitizer

E. Gatti Nuovo Cimento 7(1950) 655-673

ONE ADC !!

F.Anghinolfi and E. Heijne IEEE-Sol.St.Circ Mag.4-3(2012) 24 history of ADC

iPHONE >30 ADCs

& CERN PH Department 12 November 2013

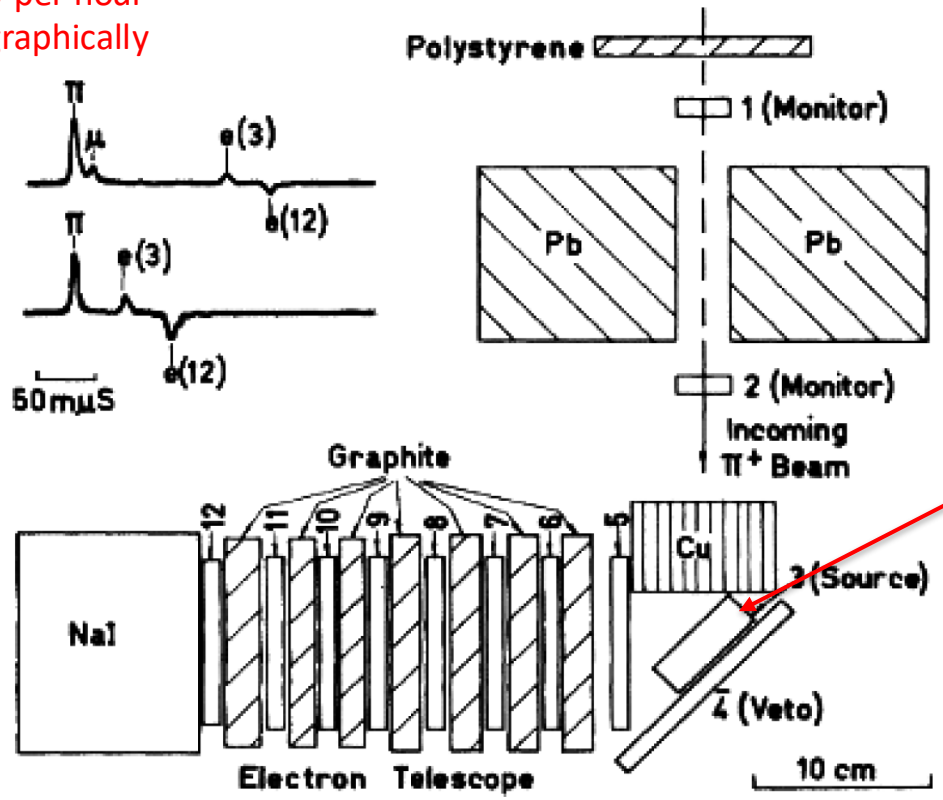
from E. Heijne EPS Workshop 2013

Early CERN

- Fidecaro et al. Discovery of $\pi \rightarrow e\nu$ decay 1958

events recorded on fast oscilloscope – few per hour – seemingly photographically

need to distinguish from $\pi \rightarrow \mu \rightarrow e$



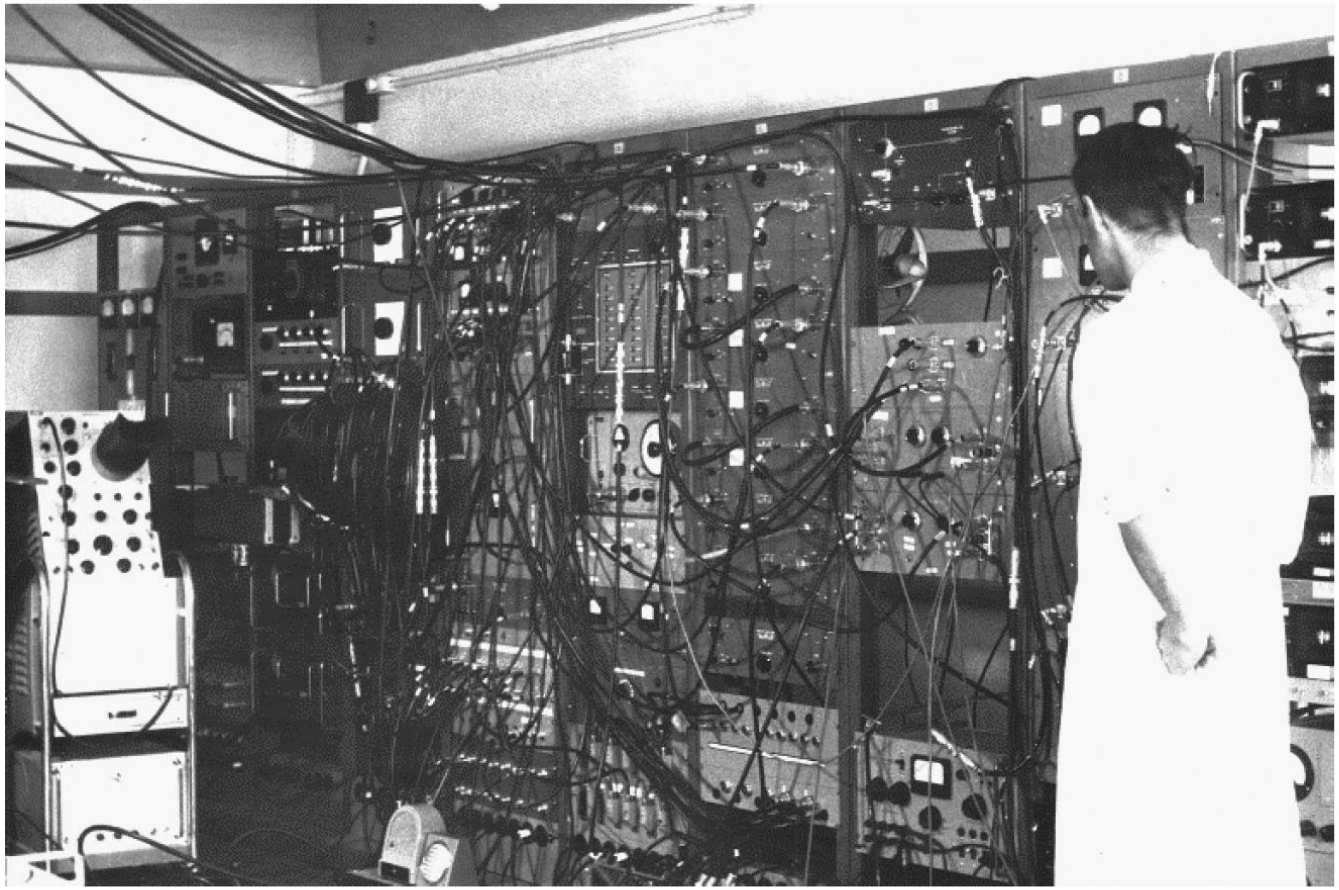
π^+ stopped in active target – plastic scintillator + PM – opened ~150 ns gate for oscilloscope

"positron detection efficiency… Monte Carlo program … at CERN when the first *electronic computer* [my emphasis] (British-made Ferranti-Mercury…) was installed"

Fig. 3. Layout of the SC experiment[29] together with typical $\pi^+ \rightarrow \mu^+ \rightarrow e^+$ and $\pi^+ \rightarrow e^+$ signals, as recorded on a fast oscilloscope (the time scale unit, "milli-micro-second" (mμs) is called "nanosecond" (ns) today). Counter 3 is the active target where incident π^+ mesons stop. The NaI counter information was not used in the final analysis.

electronics?

$\pi \rightarrow e\nu$ experiment electronics



Some scope for standardisation?

Fig. 6. The main electronic racks in the counting room of the SC experiment.[29]

BTW

- If you want to build your own circuits from circa 1959
  - components are easily available, it seems…

E88CC

EL34 :

The EL34 is a thermionic vacuum t

2. Description of the Simulator

We have built a fast pulse generator which produces groups of pulses at regular intervals and may be used to test coincidence circuits, discriminators, and scalers under pulsed conditions. In particular, we were interested in our coincidence circuit[1]) directly (minimum pulse height required about 2 V).

The simulator is used to test a circuit by verifying with an oscilloscope that the pulses in a bunch are all properly transmitted through the circuit and appear at all points of the circuit

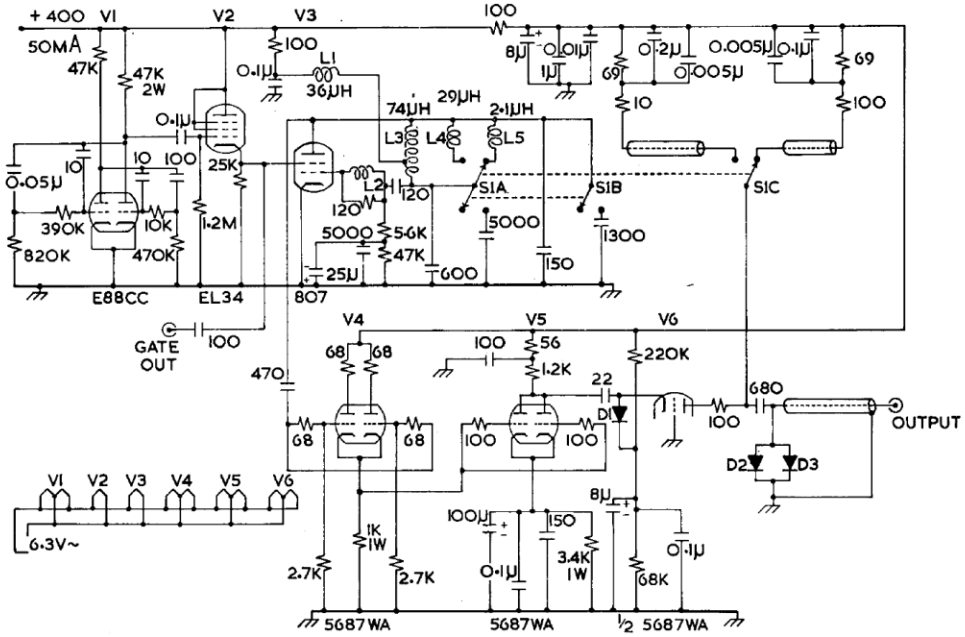


Fig. 2. Circuit diagram. Cables are 125 ohms. Capacities in the resonant circuits are mica, all others up to 0.2 μF are ceramic. Those marked + — are electrolytic. All resistances are carbon, rated $\frac{1}{2}$ W or less unless otherwise marked. Resistances given in ohms, capacities in pF unless otherwise marked. Diodes: D_1, CG1E (BTH). D_2 and D_3, HD 2130 (Hughes).

A SYNCHRO-CYCLOTRON PULSE SIMULATOR FOR TESTING ELECTRONIC CIRCUITS

T. FAZZINI, G. FIDECARO and H. PAUL†

CERN, *Geneva*

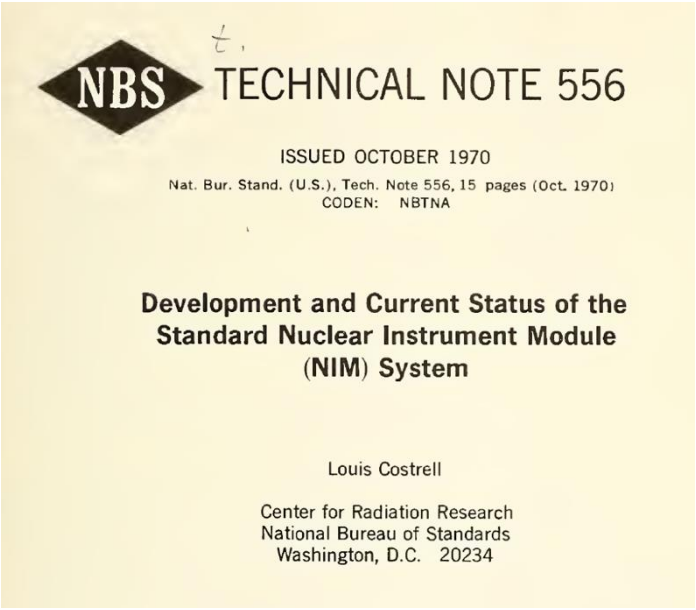
NIM (Nuclear Instrumentation Module) era

By the 1950's it was realized that most all nuclear instrumentation utilized several, common, basic building blocks with only a single or couple of application specific items for each different measurement scheme or system.

The idea came to a number of people that the basic building blocks could be provided in portable, removable modules common to a single cage or rack which would itself have a built in power supply to supply 4 commonly used DC and the standard line AC voltages on a bussed together group of standard amp plugs. The cage and attached power supply would itself fit into a standard 19" rack for laboratory use. The standardized modules could then just slide into the rack on rails and the rear mounted power plugs couple into the modules. The modules could then be linked up in logical order via front or back BNC jacks and cables to make any instrument desired. Neat, huh?

The credit for publishing the first paper to standardize this system goes to Lou Costgrell of the old Atomic Energy Commission who authored the document "Standard Nuclear Instrument Modules" TID-20893.

ORTEC (Oak Ridge Technical Enterprise Corp) offered 17 NIM Modules in their first catalog in 1966. Tennelec (Tennessee Electronics) was also an early supplier of NIM modules. (Bought out by Oxford and then Canberra. Most of the NIM makers are or were clustered in a cozy fashion on the door step of the major national AEC laboratories, which were their prime customers.



NBS TECHNICAL NOTE 556

ISSUED OCTOBER 1970

Nat. Bur. Stand. (U.S.), Tech. Note 556, 15 pages (Oct. 1970)
CODEN: NBTNA

Development and Current Status of the Standard Nuclear Instrument Module (NIM) System

Louis Costrell

Center for Radiation Research
National Bureau of Standards
Washington, D.C. 20234

NIM and miniaturisation

10. References

1. Report of National Academy of Sciences National Research Council Advisory Panel 231.00 to Radiation Physics Division of Nat. Bur. Stand., Jan. 26, 1968.

2. U. S. AEC Report TID-20893 (Rev. 3), Standard Nuclear Instrument Modules, Dec. 1969, U. S. Government Printing Office, Washington, D. C. 20402. (Earlier issues are dated July 1964, January 1966 and January 1968).

3. American National Standard Nomenclature and Dimensions for Panel Mounting Racks, Panels, and Associated Equipment, ANSI C83.9-1968, American National Standards Institute, 1430 Broadway, New York, New York 10018.

4. International Electrotechnical Commission Publication 297, First Edition, 1969, Dimensions of Panels and Racks for Nuclear Electronic Instruments, International Electrotechnical Commission, 1 rue de Varembe, Geneva, Switzerland.

5. J. Bardeen and W. H. Brattain, "Transistor, A. Semi-Conductor Triode," Physical Review, 74, No. 2, 230 (July 15, 1948).

6. United Kingdom Atomic Energy Authority Specification and Guide to the 2000 Series Unitized Equipment, AESS(R)11048, January 1962, U.K. Atomic Energy Research Establishment, Harwell, Berks, England.

7. CERN 19-inch Chassis Systems, B. Sagnell, CERN Report 62-29, 8 October 1962, European Organization for Nuclear Research, Geneva, Switzerland.

8. ESONE System of Nuclear Electronics, European Atomic Energy Community - EURATOM Report EUR 1831e dated 1964, Office Central De Vente Des Publications, Des Communautes Europeennes, 2, place de Metz, Luxembourg.

9. U. S. AEC Report TID-20893, Standard Nuclear Instrument Modules, July 1964, U. S. Government Printing Office, Washington, D. C. 20402 (Superseded by TID-20893 (Rev. 3), December 1969)

10. CAMAC, A Modular Instrumentation System for Data Handling, Description and Specification, EURATOM Report EUR 4100e dated March 1969, Office Central De Vente Des Publications, Des Communautes Europeennes, 2, place de Metz, Luxembourg.

"Though transistors are extremely small compared to vacuum tubes and consume far less power, transistorized instruments that emerged in the 1950 's were nonetheless constructed in a manner quite similar to that of their vacuum tube predecessors. Thus the ***instruments utilized 19-inch front panels*** *and contained their own dc power supplies operated from the ac line. It rapidly became apparent that such construction was quite uneconomical and inefficient, that* ***a number of transistorized instruments in modular form could be accommodated in the space occupied by a single 19-inch panel****, and that a single dc power supply…"*

Popular too…

It is difficult to recall any other instrumentation system in any field that has received even a reasonable fraction of the broad acceptance and utilization received by the NIM system. It is apparent that the system must provide considerable benefits to command such a following.

As seen in 1980

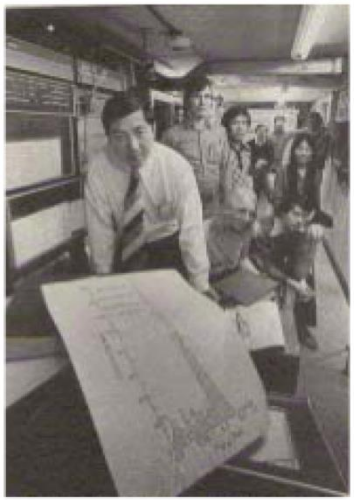
Table 8. Recent landmarks in electronics for particle physics.

Item	Approximate year of introduction	Characteristics and comments
NIM electronics (Nuclear Instrumentation Modules)	1967	Signal processing with standardised modular instruments; modularity allows repeated use for different experimental configurations; standardisations permit interchangeability, external serviceability and international industrial support
CAMAC	~1970	Extends the NIM concept to computer-oriented modular data acquisition systems; TTL-oriented signal levels; MHz signal transfer; subsequently becomes widely used in industry for process control
Custom-integrated circuits	1971	First attempts to have MWPC electronics in medium-scale integration. Concept becomes viable for experiments with $\gtrsim 10^5$ identical circuits per customer
CAMAC-compatible ADC	1972	Packaging density of ADC has increased by several hundred during period 1970–1979. Price decreased approximately by same factor
Low-noise charge-sensitive preamplifiers	1974	State-of-the-art analogue instrumentation techniques successfully adapted to high-energy physics; basis for instrumentation of ion- and low-gas-gain proportional chamber.
Programmable pre-processors	~1977	Logic decisions, too complex for conventional logic modular instrumentation, conferred to specially built programmable processor; speed of computation versus ease of programmation controversy
CAMAC replacement	~1978	Start of discussions: new system ('Fast Bus') oriented towards high-speed data transfer for 'fast' processing, based on ECL technology.
CCD, flash encoders	1978	Charge-coupled devices or flash encoders permit 'continuous' (up to 100 MHz sampling rate at present) digitisation of detector signals; allows track chamber construction with ~1 mm^3 granularity for information read-out

"Particle detectors" C W Fabjan and H G Fischer 1980 Rep. Prog. Phys. 43 1003

- Report dominated by gaseous detectors, but also Cerenkov, TR and hadronic and EM calorimetry. Electronics is discussed under detector systems.
- What happened next?

In fact, it had already happened!



Physics Motivation
November Revolution

J/ψ

11 November 1974

- *from Chris Damerell talk (Snowmass 2001)*

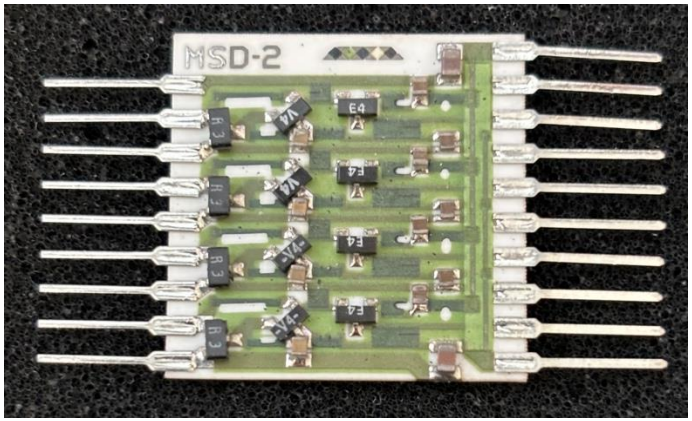
- Gaillard, Lee and Rosner RMP **47** (1975) 277 *Search For Charm*
  'The tracks of charmed particles will be too short to see in bubble chambers, but should definitely be of the order of tens or hundreds of microns: easily detectable in emulsion'.
- Charpak, EPS Conference in Palermo June 1975
  'Drift chambers are the easiest to build, most accurate, cheapest and most convenient detector for localising particles. Whoever is familiar with their operation would be strongly reluctant to use other devices in the planning of a new experiment'.
- ACCMOR collaboration in CERN struggled to see charm hadroproduction (single *e* trigger)
- Succeeded over next 10 years to develop silicon microstrip and pixel detectors (CCDs) as powerful tools for charm physics.

CJSD/Snowmass/July 2001/no3

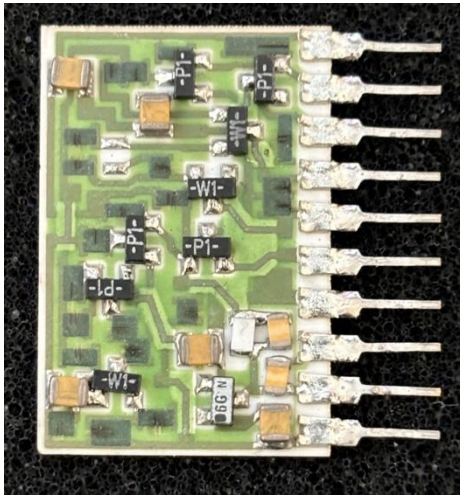
The driving force behind many electronics developments since the mid-1980s. Would it have happened anyway?

1980s custom integrated circuits

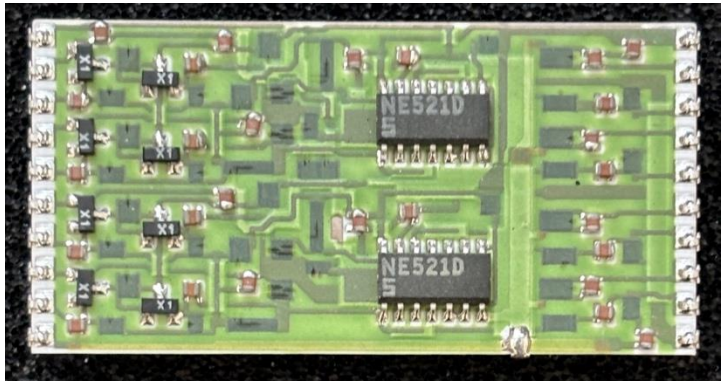
- Hybrid thick film ceramic circuits
  - from LABEN (1958-2004) *LABoratori Elettronici e Nucleari*
    - merged into Alcatel Alenia Space



Quad bipolar preamplifier

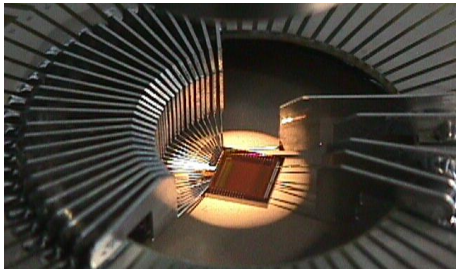


Single channel
JFET-bipolar
preamplifier



Quad bipolar-IC comparator
shaper discriminator

The ASIC era

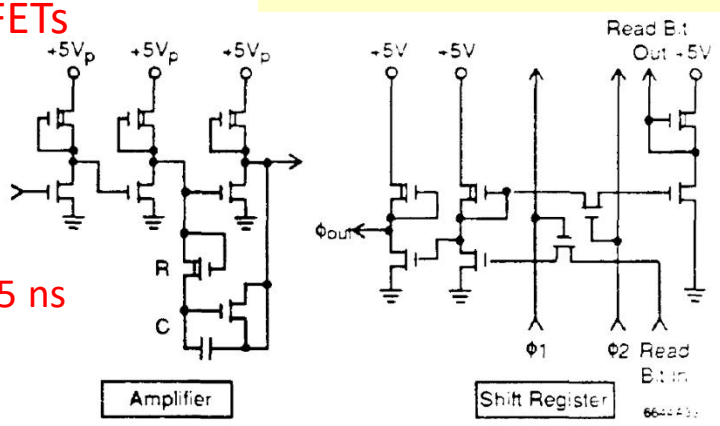


- Application Specific Integrated Circuit
  - customised electronic circuit for a well-defined requirement
  - generally manufactured in **CMOS**
    - a lot of people joined in from around 1990
- Pros of ASICs
  - **can be optimised** for demanding requirements: size, power, functions, performance,…
  - **miniature** – large numbers of channels
  - very **dependable manufacturing quality with low unit cost** on large scale
  - **radiation hardness** now understood, and can be excellent in commercial processes
- Cons of ASICs
  - **Big development investment** required in both time and cost
  - **Unchangeable** once complete, unless a lot of flexibility built-in (adds complexity)
  - **Substantial design and evaluation** requiring specialist skills (industry pays well!)
- In short, well matched – and essential! - to the later LHC era
  - once the technologies had been mastered

A very brief history

- 1984 - first HEP ASIC: Microplex at SLAC (California!) Mark-II silicon vertex detector
  - NMOS only : 128 channel - amplifier, Sample-Hold, DCS processing, multiplexing.
    - 34 mm^2 , 5µm university lab process, **14 mW/ch**. **Pioneers** learned from first principles!
- Late 1980s: MX3, MX7, CAMEX64 - LEP silicon vertex detectors
  - Commercial CMOS, initially ~3µm and later 1.5µm => 1-2 mW/channel
    - Amplifiers: integrators with switched capacitor filters. Switching noise injected during the amplifier reset subtracted due to its very reproducible behaviour. $t_{rise} \approx 400$ ns, $t_{int} \approx 1.8$ µs
- 1988: SVX ASIC for CDF (& L3) – memory & sparsification
  - amplifier, comparator, multiplexer, nearest neighbour logic, pedestal subtraction
    - 128 channels in 3 µm CMOS $t_{int} \approx 200$ ns, $t_{sample} \approx 0.5$ µs
- 1990: Amplex for UA2 Si pads - feedback resistors using FETs
  - 16 channel 3µm CMOS, precise control of non-linear R
    - more conventional RC filters implemented: $\tau_{peak} = 0.75$ µs
- Early 1990s – LHC developments began
  - originally 66 MHz beam crossing rate, later 40 MHz => $\tau \approx 25$ ns
    - almost x 10^6! - from 120 Hz at Mark-II in a decade
    - but 1-2 µm processes

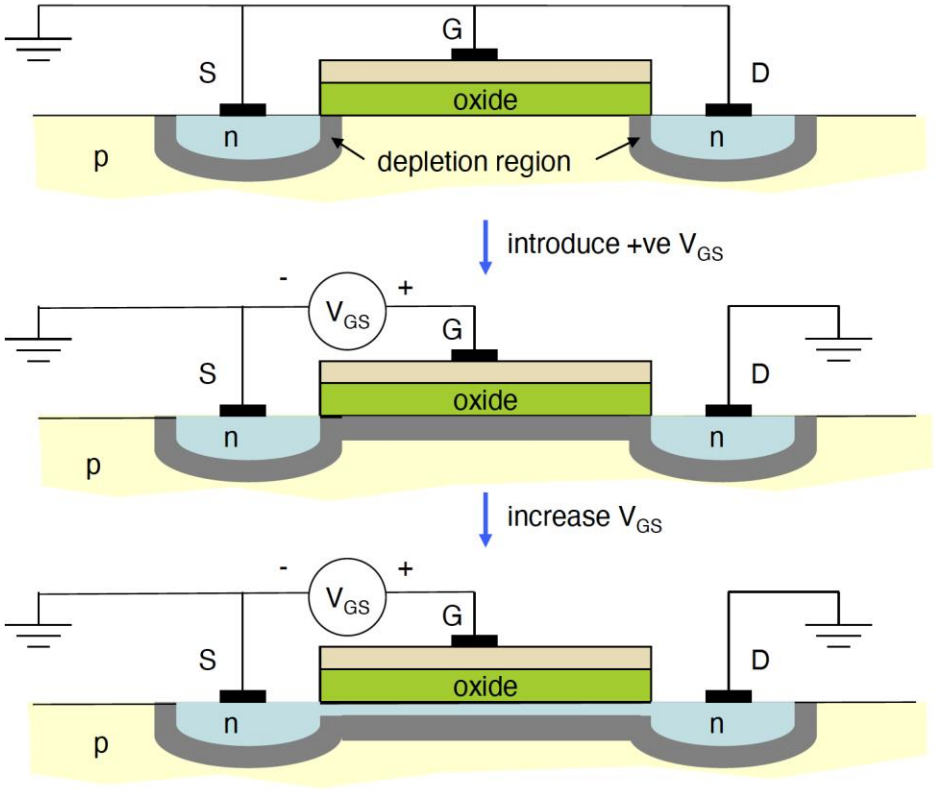
Part of the Microplex circuit



MOSFETs – in principle and practice

well known to many present here…

- Transistor is simple device: layout and behaviour, especially digital
  - but also many good analogue properties, if needed



channel just forms at $V_{GS} = V_T$ = threshold voltage

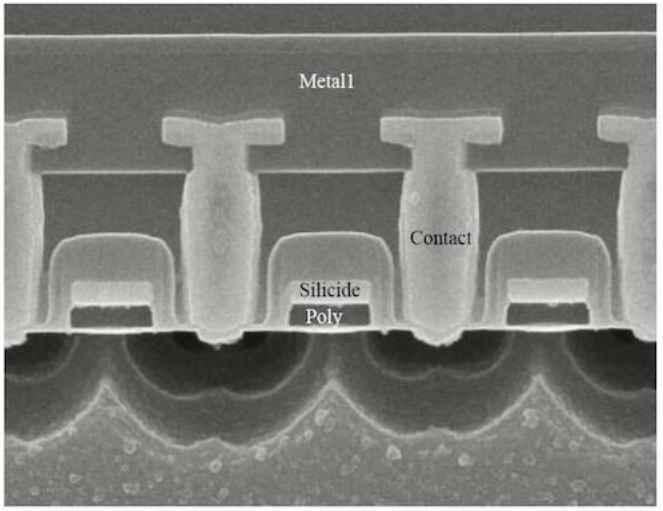


Figure 5.22 SEM image of the cross-section of three MOSFETs.

1990s: many investigations of noise vs power, radiation tolerance in multiple processes

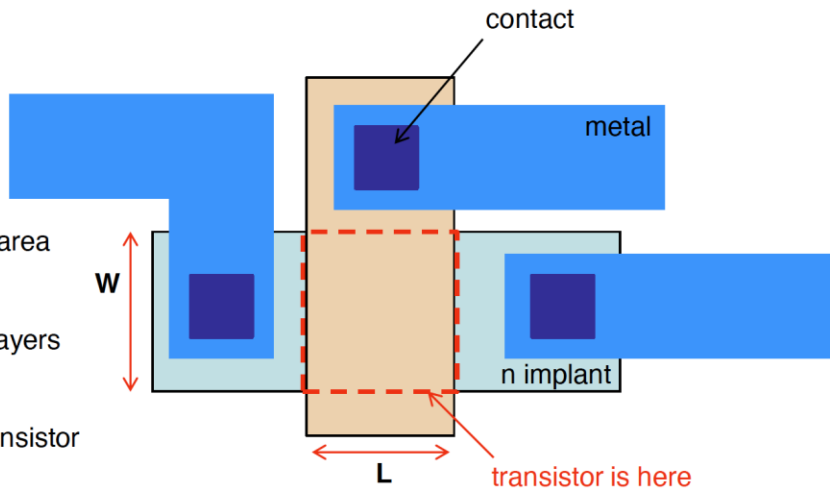
MOSFET design

designer draws the masks

NMOS transistor is formed where gate area crosses n implanted area

contact regions are defined and metal layers used for connections

only the width **W** and length **L** of the transistor are under the designer's control



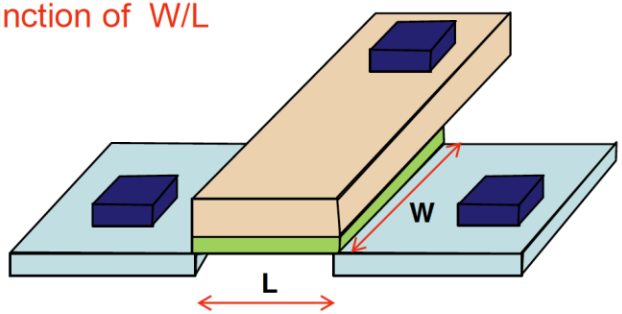
It really was like this around 1985! Our engineers were learning this new technology.

Circuit properties mainly scale with feature size

L, W, t_{ox}, V =>
L/S, W/S, t_{ox}/S, V/S

transconductance is a rather simple function of W/L

In practice today, sophisticated computerised design software is used to lay out transistors often with libraries of frequently used circuits



plus a lot of complex simulation tools and checking to validate designs

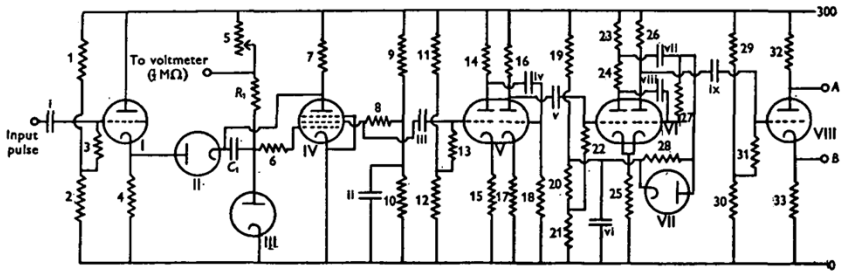
Table 6.3 CMOS scaling relationships.

Parameter	Scaling
Supply voltage (VDD)	S
Channel length (L_{min})	S
Channel width (W_{min})	S
Gate-oxide thickness (t_{ox})	S
Substrate doping (N_A)	S^{-1}
On current (I_{on})	S
Gate capacitance (C_{ox})	S
Gate delay	S
Active power	S^3

The low noise era

- We owe a lot to the early nuclear physicists and engineers
  - e.g. the design of the Wilkinson ADC, based on valve circuits, is far from simple

3·1. First, the unit which converts the input pulse into the proportional time pulse will be considered. It is shown in Fig. 1.



- Most of the literature on signal processing originates in the 1960s
  - e.g. Radeka, Goulding, Gatti, Manfredi, Kandiah,…

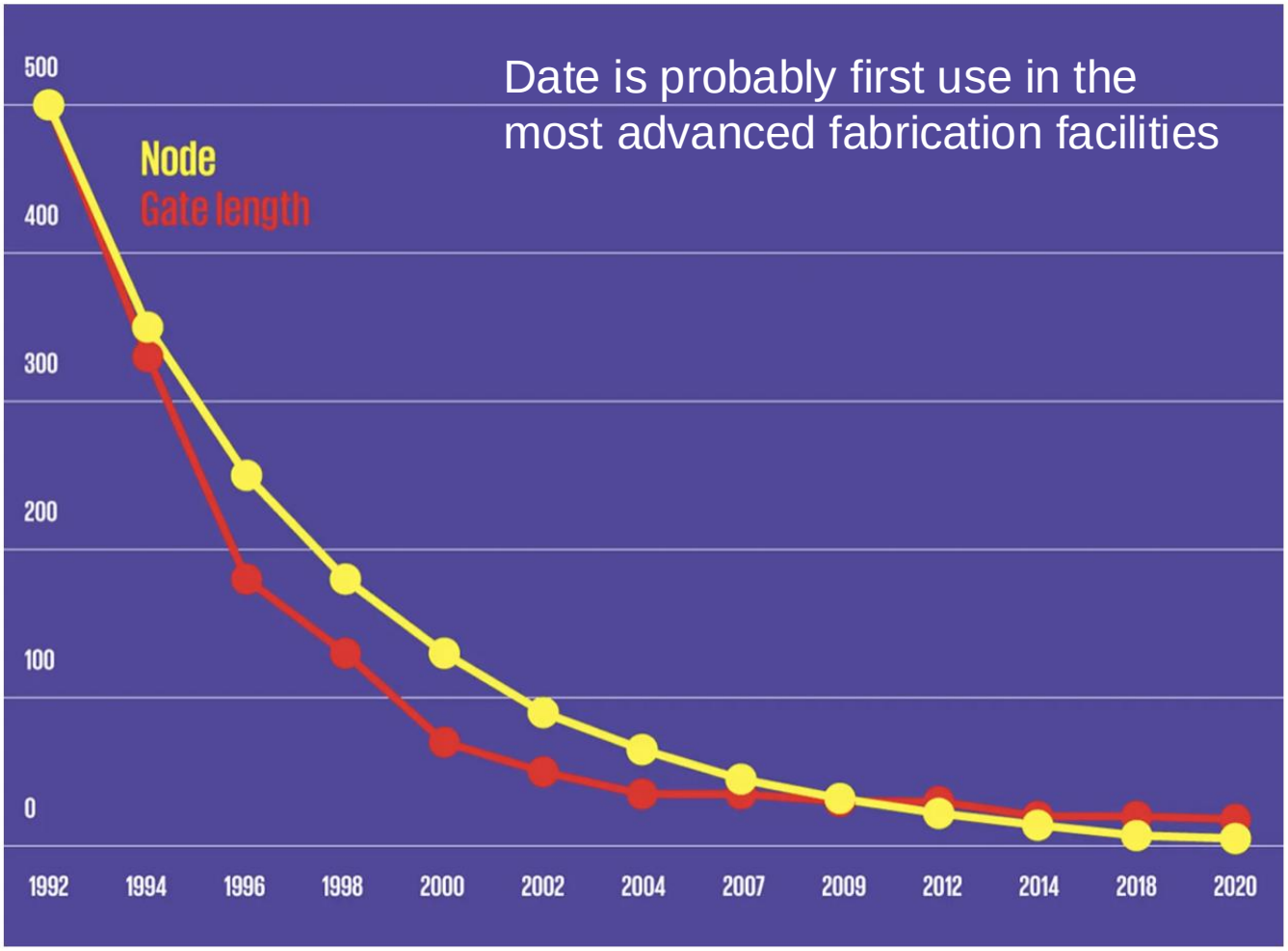
Ann. Rev. Nucl. Part. Sci. 1988. 38: 217–77

LOW-NOISE TECHNIQUES IN DETECTORS

Veljko Radeka

Perhaps driven by absence of gain in silicon sensors (at that time)?

ASIC technology progress



SOURCES: STANFORD NANOELECTRONICS LAB, WIKICHIP, IEEE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2020

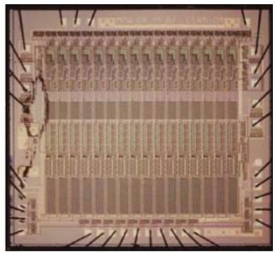
- In 1998 we were designing the APV25 for CMS in 0.25 µm
  - finalised 2000/2001
- We started designing the CBC chip in 2010, in 130 nm
  - completed CBC3.1 in 2018/2019
- Today HEP is designing in 65 nm
  - Some are testing the water with 28 nm
- Note the lag to HEP

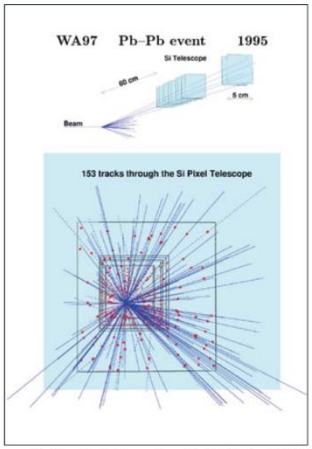
As seen in 2014

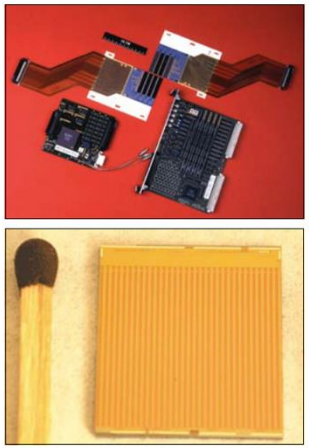
H. Wenninger CERN Courier

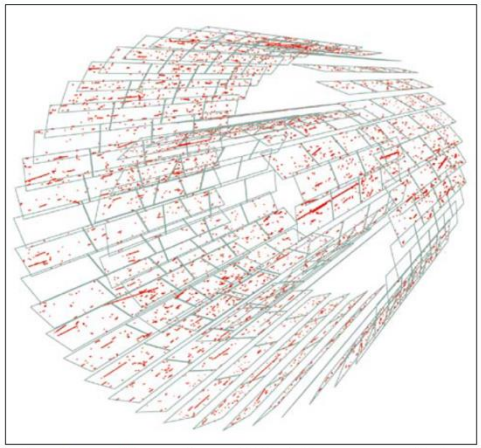
CERN Courier March 2014

Microelectronics at CERN: from infancy to maturity









...p left) allowed UA2 to fit a silicon-pad detector (bottom left) in the 9 mm gap around the beam ...centre), were used in WA97 in the mid-1990s. By 2002, CERN had developed a ...orded muon tracks produced in the nearby beam dump during the first injection tests (right).

The LAA

The LAA programme, proposed by Antonino Zichichi a... Italian government, was launched as a comprehensive... new experimental techniques for the next step in hadro... multi-tera-electron-volt energies. The project provided... for Europe to take a leading role in advanced technolog... physics. It was open to all physicists and engineers inte... A total of 40 physicists, engineers and technicians wer... than 80 associates joined the programme. Later in the... operation of LEP for physics, the programme was com... activities overseen by CERN's Detector R&D Committe...

years 1984–1985 Heijne was seconded to the U... where the microelectronics research facility ... Interuniversity MicroElectronics Centre (IM... apparent that CMOS technology was the way ... rience with IMEC led to Jarron's design of the...

(Earlier, in 1983, a collaboration between S... versity Integrated Circuits Laboratory, the U... and Bernard Hyams from CERN had already i... the "Microplex" – a silicon-microstrip detecto... nMOS, which was eventually used in the MA... SLAC in the summer of 1990. The design w... by Sherwood Parker and Terry Walker. A ne... Microplex design was used in autumn 1989...

of know- ... the group, and from Jim Virdee, who is one of the founding fathers ...

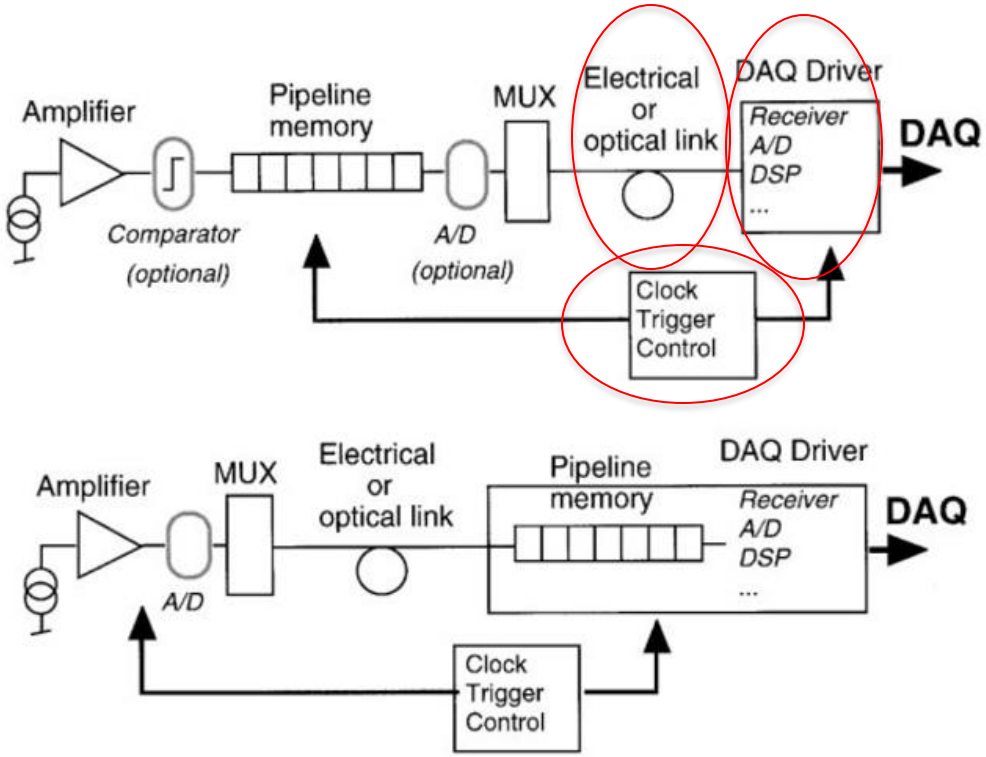
The start of the LAA project in 1986 propelled electronics at CERN into the era of microelectronics, and laid crucial foundations for the success of the LHC experiments.

ASIC design had come of age – and was very mature

All true – but only a part of the picture of making the experiments possible

LHC era

- Developments initially driven mainly by trackers and ECALs
  - Amplifiers, data conversion and FE storage, data transfer, ….
  - Clock and control, Trigger
- Many possible design choices, e.g.:
  - analogue/digital/binary
  - performance
  - commercial or custom
  - radiation tolerance
  - power, cost, risk …
- ASICs came first but other things were essential too, especially
  - optoelectronics
  - trigger processors
  - computer technology evolution
    - which I won't attempt to cover…



a couple of possible variants

How did we get to where we are today?

- Sponsored R&D (US SSC detector R&D 1988, CERN DRDC 1990) played a big role
  - much credit to the wise people who devised those programmes
    - but was there any choice? SSC/LHC detectors were unbuildable
  - **serendipity**: mass commercial electronics era -> internet age
    - 1980s-1990s: RISC processors, PCs, Apple desktops, WWW, modems, mobile phones, laptops,…
  - historians can explain the sequence but all were driving greater miniaturisation
    - many "invisible" components, like connectors, packaging, batteries, not just ICs

Several crucial areas - **commercially driven** - not by HEP

- Integrated circuit electronics
  - emergence of **accessible ASIC processes**, and design tools
  - significant investment in **training** of new generation of engineers as designers
- Optoelectronics
  - practically non-existent before LHC, and fortuitous **technology co-evolution**
- Off-detector electronics
  - **programmable logic** evolved dramatically from mid-1990s

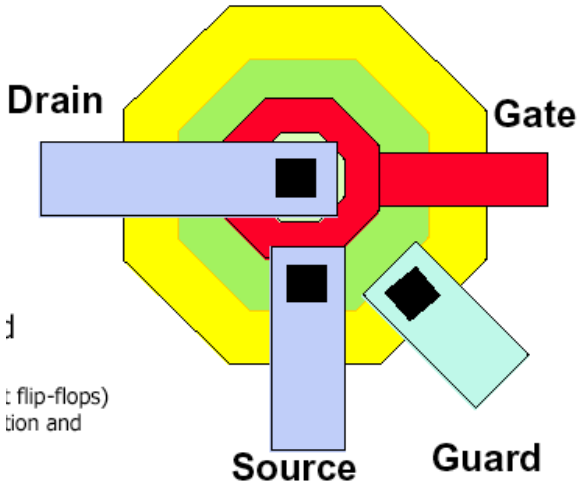
Example: CMS silicon µstrip tracker ASICs

- Began in 1991 in RD20 DRDC project
  - amplifier (several variants) + already proven pipeline concept
  - several prototype chips in supposed rad-hard 1.2 µm technology, 32- then 128-channel
    - plus a couple of non-rad hard ASICs, for detector prototyping (NB important!)
    - By 1997: APV6 might have been a candidate for final system
    - many irradiation studies of single transistors (noise) and chip performance
  - Along the way, some important innovations
    - programming chip parameters via serial command interface (I2C) using software control
      - **hugely beneficial in accelerating** chip configuration and evaluation
      - primitive (by today's standard) signal processing on chip (e.g. deconvolution) to save power

- Bad luck – which turned out to be good luck – in September 1997
  - Foundry move of 1.2 µm process **reduced** radiation tolerance (marginal anyway)
  - Unexpected **positive** CERN results on "standard commercial" 0.25 µm radiation tolerance
    - In 1998 switched process – which was a turning point – for **APV25** (Sept 1999)

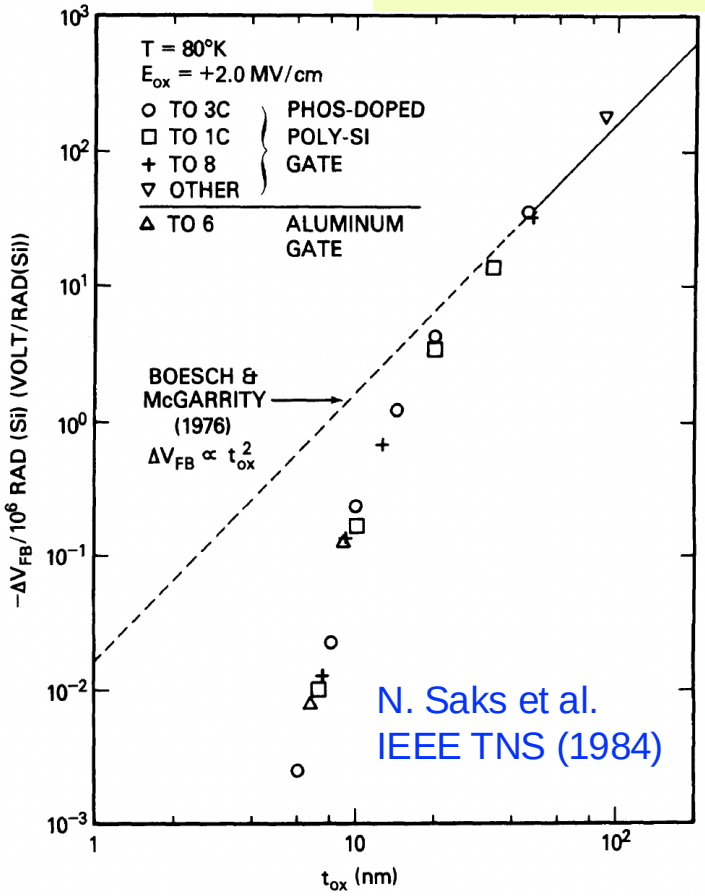
Radiation behaviour of commercial CMOS

- Evidence of radiation tolerance in mid-1980s, improving with thinner oxides
  - tunnelling of carriers reduces trapped oxide charge
  - but confusing results from commercial chip evaluations
- negative effects attributed to leakage paths around NMOS transistors
  - *cured in CERN 1997 with enclosed gate geometry*



This was a **hugely important** breakthrough

ΔV_{FB}/Mrad vs t_{ox}



Coda

- APV25 switch to IBM 0.25 µm was incredibly successful
  - engineers from RAL, Imperial & CERN transferred design quickly
    - well characterised process: designs matched simulations
  - big gains from scaling 1.2 µm to 0.25 µm
  - radiation hardness was well in excess of requirements

- Others took note, for many detectors and sub-systems

- It wasn't quite the end of the story
  - unexpected yield variations were experienced at the early production stage
  - weak points in the (not quite standard) manufacturing process were identified
    - by IBM specialists - and fixed – we would not have been able to
    - production quality was subsequently excellent – very high yield of good chips

Opto-electronics

- First(?) mention: B. Leskovar (1990) SSC workshop
  - *Optical data transmission at the SSC* IEEE Trans.Nucl.Sci. 37 (1990) 271-287
    - extremely detailed discussion, including radiation hardness issues – did anything follow?
- Many DRDC projects started in 1991, including RD12 & RD23
  - RD12 proposed optical distribution of TTC signals at the LHC
    - commercial parts using 1300 nm lasers and SM fibres, but not radiation hard
  - RD23 proposed optoelectronic modulators for data transmission **inside** the experiments
    - technologies: $LiNbO_3$ and Multi Quantum Well reflective modulators
- $LiNbO_3$ well established but several drawbacks
  - bulky, polarisation maintenance, cost
- MQW attractive but more speculative
  - very reliant on commercial device progress
- Other technologies became accessible
  - Fabry-Perot edge emitters, VCSELs
  - both successfully deployed in CMS & ATLAS

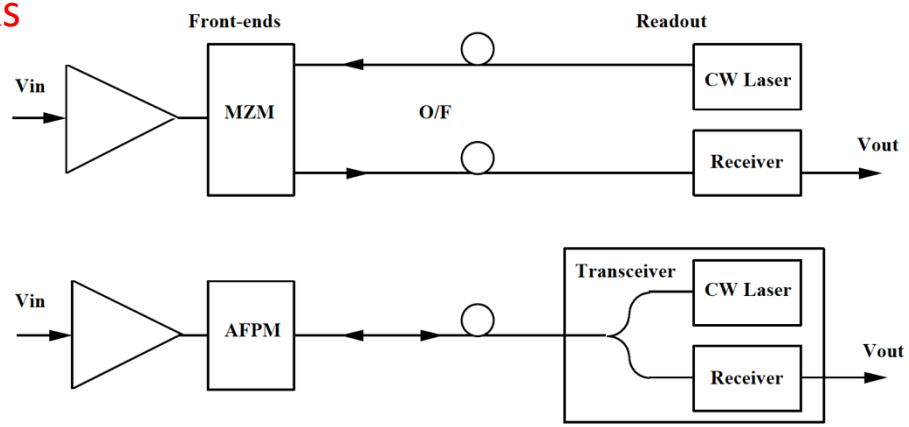


Fig. 3.1 - Optical links with transmission/reflection intensity modulators

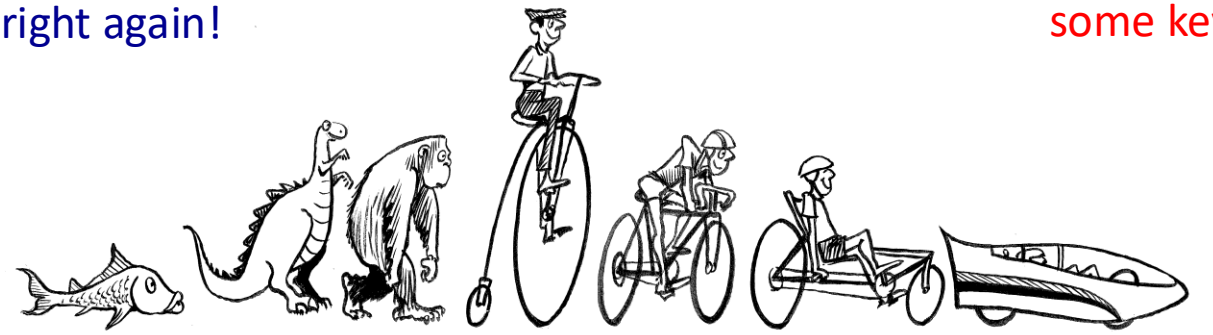
Comments on optoelectronics

- Advantages of optical data transfer – partly informed by hindsight
  - (much) reduced material in cables
  - lower power (probably by a big factor)
  - (much lower) risk of excess noise and (likely greatly) improved signal integrity
  - higher (total) bandwidth
  - standardisation – probably not perfect but a big step forward
    - e.g. CMS used the same technology for tracker (40 MHz analogue) and ECAL (800 Gbps)

fortunately we did not have to make the comparisons in practice

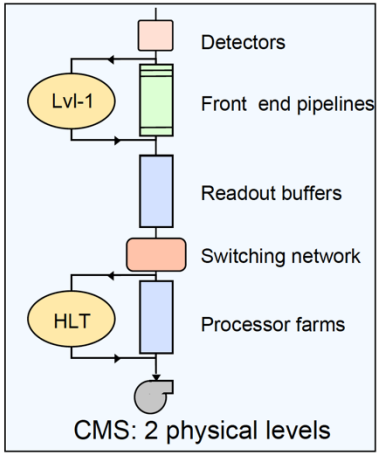
- In a revised version of history, LHC experiments might have failed
  - or at least been much less effective
- The R&D projects were quite risky, but evolved successfully
  - Darwin was right again!

Thanks again to some key individuals



Triggers

- One of the most popular subjects in these conferences
  - many excellent comprehensive introductory lectures, especially in HEP schools
    - no point in trying to replicate them, especially given the huge subject matter
- A few key facts:
  - aim is to reduce data rate to storage for offline analysis
  - almost invariably requires multiple stages (trigger levels)
  - selection should be unbiased, and preserve the (often rare) physics
  - so far, so conventional…
- Now, for some provocation…
  - there are many ways to skin a cat
  - In HEP, you can guarantee that many of them will appeal, but not to everyone
  - the biggest problem is to achieve the objective using available technologies
  - hence: adapt the design to fit the technology, e.g. clever algorithm, fewer bits, favourite processor, ASIC,… or move the goalposts…



Trigger requirements

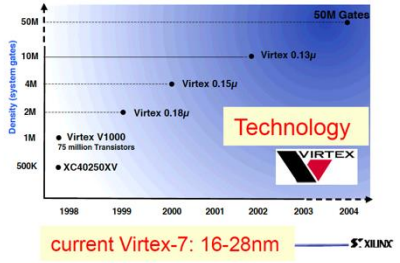
- High – as possible - efficiency for the most interesting events
  - should not introduce bias
- Large (enough) rate reduction
  - but can pass unwanted (with hindsight) events as BW permits
- Fast decision
  - to match hardware constraints, mainly at FE
- Deadtime free
  - to maximise good data, and $\varepsilon^N << 1$
- Flexible enough to adapt to changing experimental conditions
  - physics programme also evolves and typical early focus is on limited number of searches
- (affordable in $ & W)

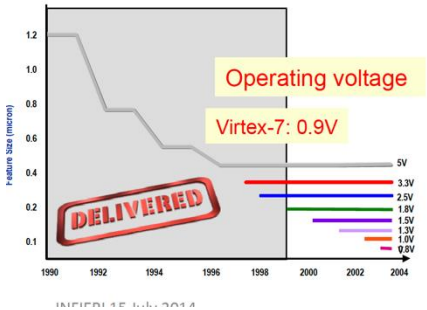
Digital processing & FPGAs

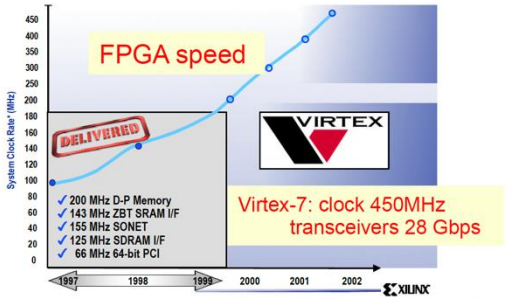
- 1980s: board based processors
  - COTS: various processor technologies: RISC, transputers, microprocessors, ….
  - custom: assemble arrays of digital chips to implement required design logic
    - wire-wrap for correctable prototyping, then solder to PCB, but…
- 1990s: technology evolution
  - commercial switches, networks, fast links, traffic management, ever faster computers,..
    - but not sufficient for first level triggers:
  - gradually (useful) FPGAs materialised
    - first major talk at LEB99
- 2010+:
  - huge progress with FPGAs
    - speed, BW, connectivity, flexibility,…
  - it seems feasible that most (all?) L1 triggers could be FPGA-based
    - but many practical issues of cooling, optical connectivity, board design, programming, complexity, …

P Alfke (Xilinx Corp)

The view in 1999







	1965	1980	1995	2010(?)
Max Clock Rate (MHz)	1	10	100	1000
Min IC Geometries (µ)	-	5	0.5	0.05
# of IC Metal Layers	1	2	3	10
PC Board Trace Width (µ)	2000	500	100	25
# of PC-Board Layers	1-2	2-4	4-8	8-16

- Every 5 years: System speed doubles, IC geometry shrinks 50%
- Every 7-8 years: PC-board minimum trace width shrinks 50%

How to succeed in a changing world?

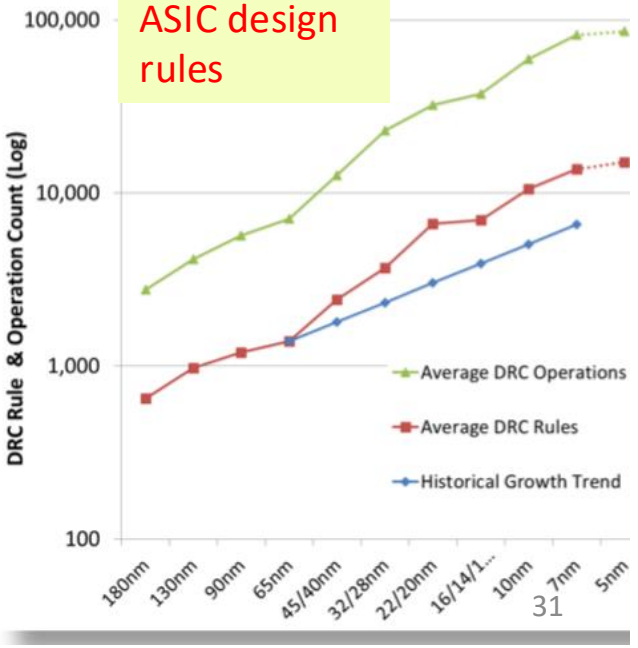
- What does history tell us? (for later discussion?)
  - many issues were overcome, so can be avoided in future
    - it's rare that the same problems (**not usually mistakes**) occur the same way
  - effort is always in short supply
  - many problems are "small" – but with big repercussions
  - manufacturing is sometimes an issue – but natural quality variations occur

- Nevertheless, today designs are remarkably successful
  - Quality of design tools
  - Quality of manufacture
  - Experienced designers
  - Comprehensive simulations
    - no guarantee though!
  - Prototyping
  - Careful evaluation (eventually in situ)

At a price, e.g.:

NB log scale

Evolution of ASIC design rules



slide from Marcus French RAL 2022

ASIC Design skills and approaches changing

The Issue:

- Its not just us – the whole industry is facing the same challenge
- Must work with validated IP to manage risk
- Strict QA is demanded at all stages

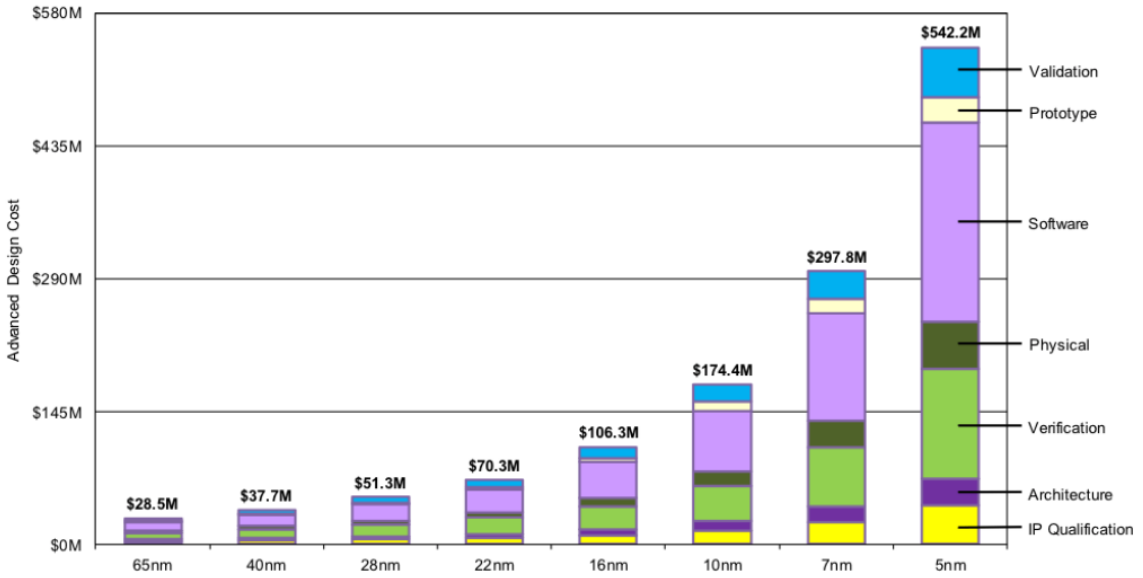
Consequences:

- Increased stress on design teams
- The software is becoming more specialised requiring committed teams dedicated over longer periods
- More effort required for the un-sexy verification and other tasks
- Links with National Labs and CERN are now mandatory

We simply can't work in the 'old' ways…

Even if not using such advanced processes, the same challenges are present – note breakdown by task

Design cost vs technology node

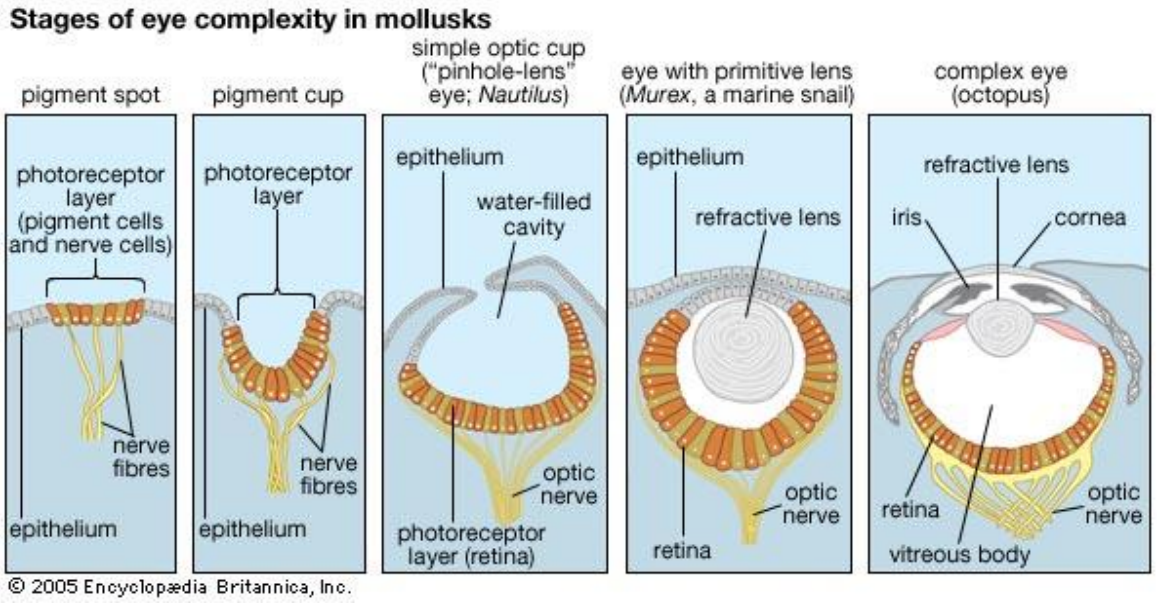


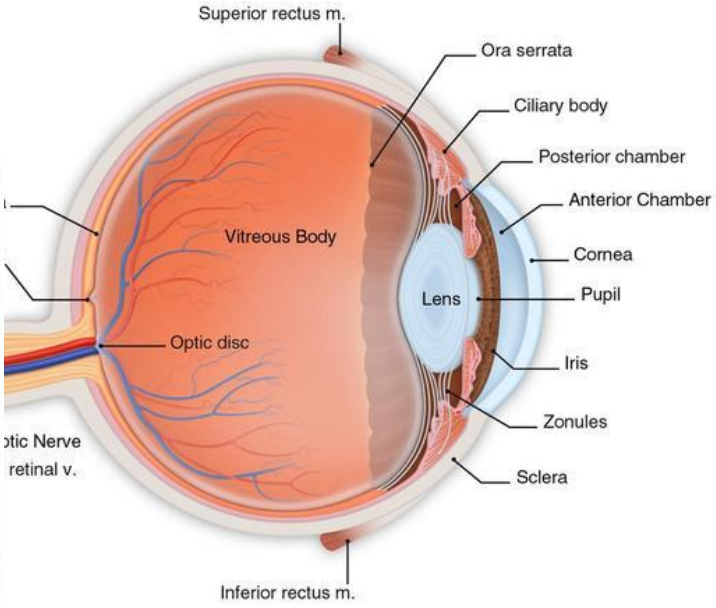
From: Semiconductor Engineering

This probably applies everywhere in our electronics

The era of complexity

- Evolution happens naturally
  - creeping changes, whose dramatic scale only becomes obvious in comparison with the past
  - our systems are of increasingly high complexity
    - no time for discussion of how to operate or program them but many years were needed, to construct and debug them, and provide tools to use them
- Which stage are we at and what will happen next?





Beware of some consequences…

- Evolution also can have other effects
  - corrections may be required…

  - magnification needed to see small details
    - as sometimes being observed in upgrade projects, e.g. …
    - There are 27 D flip-flops that are expected to contribute to this failure mode. Out of the 2^{27} possible states, 2^{20} of them result in entering the dysfunctional state (which reduces to 1/128 or ~ 0.8%).

Some conclusions

- Our electronics has changed dramatically in CERN's lifetime
  - but the objectives (e.g. triggering, position, time and energy measurement) remain

- The LHC fortuitously coincided with the internet era
  - explosion of relevant technology development – high volume, low unit cost
    - much of it accessible to small users, such as HEP
  - **it is arguable that the biggest changes in detector technology were in electronics**
    - it has enabled implementation of increasingly complex functionality

- BUT greater complexity = longer development times and more resources
  - higher risk and less flexibility for small projects
  - How to manage this for the next generation?

- Not to be forgotten
  - electronics is commercially driven
  - and cannot be assumed to align with science

"When examining these new contracts, gentlemen, please note that in Paragraph 48 the word 'golden' has been replaced by 'plywood' and 'parachute' is now 'toboggan.'"

Acknowledgements

- There are too many people to name individually
  - and I would risk missing many

- Some are still active, others retired…

- I thank them all nevertheless!!

Backup

Some references

G.W. Clark, *The Contributions of Bruno B. Rossi to Particle Physics and Astrophysics*, Atti del XXV Congresso Nazionale di Storia della Fisica e dell'Astronomia, Milano, 10-12 novembre 2005, (Milano: SISFA, 2008): R1.1-R1.16.

Walter Bothe and Bruno Rossi: The birth and development of coincidence methods in cosmic ray physics. Luisa Bonolis arXiv:1106.1365v2 [physics.hist-ph] 29 Jul 2011

Rossi, B *Method of Registering Multiple Simultaneous Impulses of Several Geiger Counters*, Nature 1930, 125: 636.

Rotblat, J *Application of the coincidence method for measurements of short life periods* Proc Roy Soc A 1941, 177: 260

G. Fidecaro *The discovery of rare pion decays at the CERN synchrocyclotron*. in 60 Years of CERN experiments and discoveries *Adv. Ser. Direct.High Energy Phys.* 23 (2015) 397-414

C W Fabjan and H G Fischer *Particle detectors* 1980 Rep. Prog. Phys. 43 1003

E. Gatti & P. Manfredi *Processing the Signals From Solid State Detectors in Elementary Particle Physics* Riv. Nuovo Cim. 9N1 (1986) 1-146

V. Radeka *Low-noise techniques in detectors* Ann. Rev. Nucl. Part. Sci. 1988. 38:217-277

A. S. Schwarz *Heavy flavor physics at colliders with silicon strip vertex detectors* Phys. Rept. 238 (1994) 1-133

G. Hall *Semiconductor particle tracking detectors* 1994 Rep. Prog. Phys. 57 481

G. Hall & A. A. Grillo *ASICs for LHC intermediate tracking detectors* NIM A1050 (2023), 168115