Redefining electronic boundaries with 3D integration and advanced packaging

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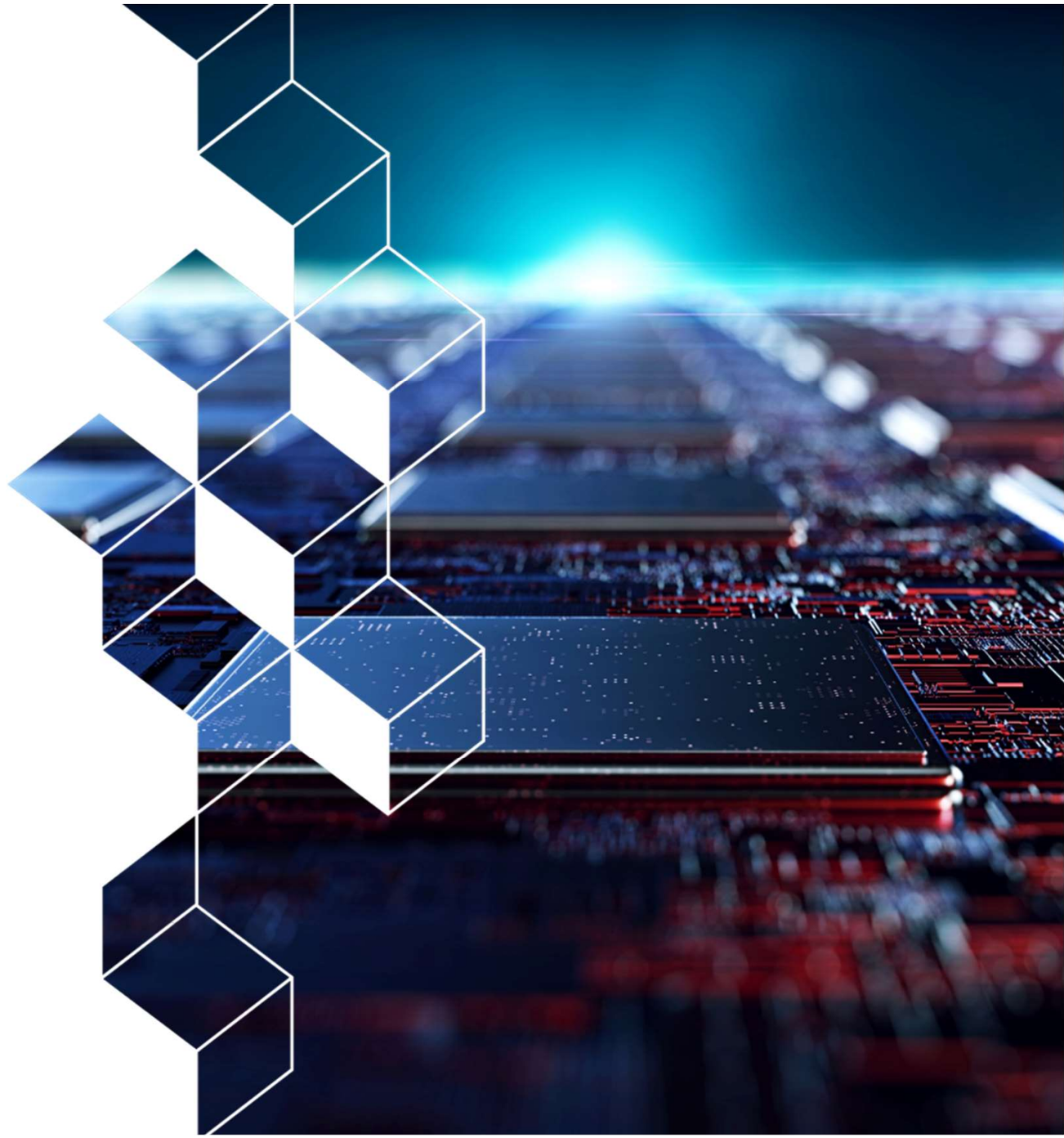

Outline

- **Going vertical ?**
- **3D integration toolbox**
- **Fields benefiting from 3D architectures**
- **A few words about fan-out wafer level packaging**

1.

Going vertical ?

Not really a new idea !

Three-Dimensional IC Trends

YOICHI AKASAKA

Invited Paper

VLSI will be reaching to the limit of minimization in the 1990s, and after that, further increase of packing density or functions might depend on the vertical integration technology.

Three-dimensional (3-D) integration is expected to provide several advantages, such as 1) parallel processing, 2) high-speed operation, 3) high packing density, and 4) multifunctional operation.

Basic technologies of 3-D IC are to fabricate SOI layers and to stack them monolithically. Crystallinity of the recrystallized layer in SOI has increasingly become better, and very recently crystal-axis controlled, defect-free single-crystal area has been obtained in chip size level by laser recrystallization technology.

Some basic functional medels showing the concept or image of a future 3-D IC were fabricated in two or three stacked active layers.

Some other proposals of subsystems in the application of 3-D structure, and the technical issues for realizing practical 3-D IC, i.e., the technology for fabricating high-quality SOI crystal on complicated surface topology, crosstalk of the signals between the stacked layers, total power consumption and cooling of the chip, will also be discussed in this paper.

Introduction

The ultimate IC structure of the future is thought to consist of stacked active IC layers sandwiched by insulating materials.

Various devices or circuit functions, such as photosensors, logic circuits, memories, and CPUs, will be arranged in each active layer and, as a result, a remarkable improvement in packing density and functional performance will be realized.

In 1979, it was reported that polysilicon deposited on insulator can be melted and recrystallized by laser irradiation [1] and that the crystal perfection of the layer can be adequate to allow the fabrication of devices.

The quality of the recrystallized layer can be characterized by carrier mobility. As shown in Fig. 1, the electron mobility reported so far has increased year by year and has attained a value comparable to bulk crystals. This improvement was a trigger for starting research and development of 3-D ICs.

A partial 3-D structure has already been tried for a dynamic memory (DRAM) cell [2], [3]. For high-density RAMs, such as the 4-Mbit DRAM, the area of the memory cell capacitor is limited, so in order to increase the cell capacitance, a 3-D structure, i.e., a trench cell or a stacked capacitor cell, has been tried. This partial 3-D structure will be used in 2-D VLSIs within a few years.

To achieve a breakthrough in the packing density of advanced VLSIs, it is reasonable to consider a 3-D structure, containing either partially or completely stacked active layers. Fig. 2 shows a forecast of the development of 3-D ICs schematically, as 3-D technology progresses. This figure was obtained from the 3-D IC Research Committee of the 3-D

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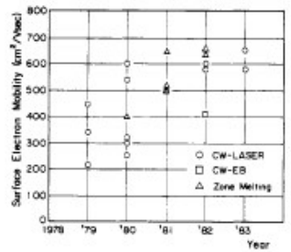


Fig. 1. Progress of surface carrier mobility of MOSFET fabricated on SOI layer. ○—CW laser; □—electron beam; △—carbon strip heater.

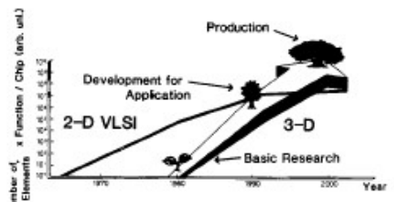
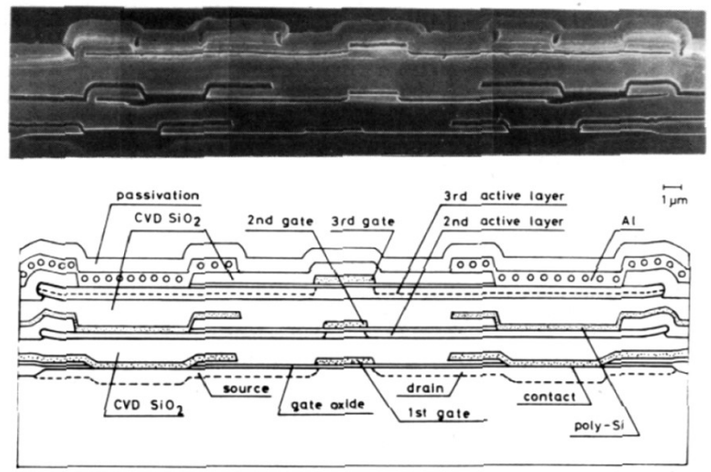


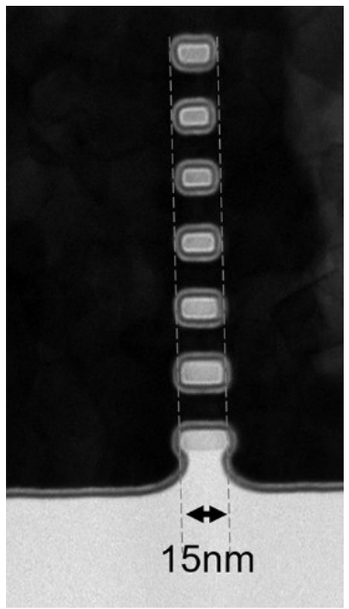
Fig. 2. Forecast of progress of 3-D technology.

Y. Akasaka, Proceedings of the IEEE, Vol. 74, NO. 12, Dec. 1986

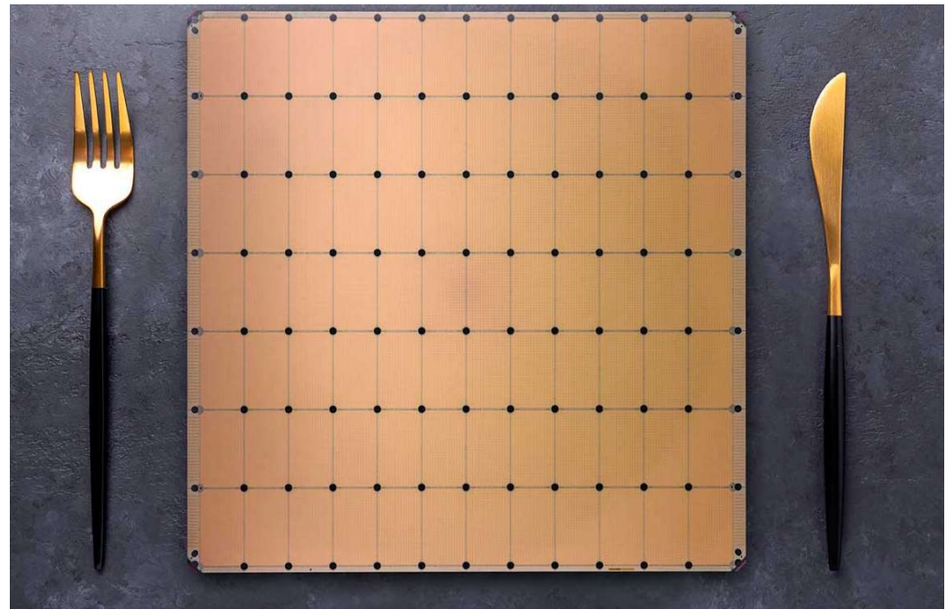


Akasaka expected 3D IC production around 2000…

But Moore's law has taken up a lot of space…



7-level stacked “Nanosheet” gate all around transistor,
CEA-Leti 2020



Cerebras WSE-2, 2.6 Trillion transistors, 7nm TSMC
© Elizaveta Elesina / Cerebras

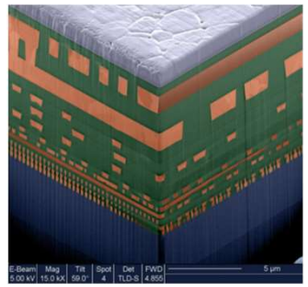
Moore's law puts pressure on interconnects

- **Consequences of miniaturization**

  Dramatic R.C product increase → interconnect delay

- **Countermeasures to reduce R.C**

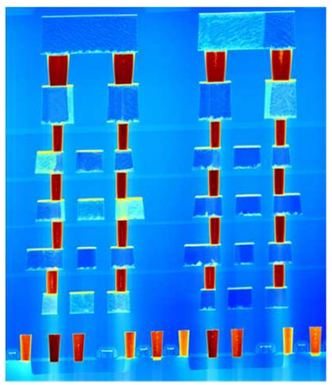
  Switch from Al to Cu & low-k dielectrics, air gaps



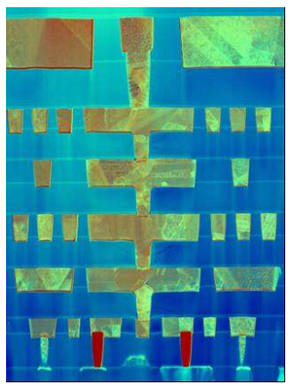
Circuit cross section

CMOS node	130 nm	32 nm
Interco. layers	6	9
M1 min. pitch	350 nm	112,5 nm
M4 min. pitch	756 nm	168,8 nm
M6 min. pitch	1204 nm	337 nm

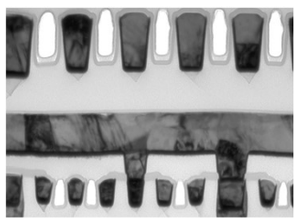
Back end of line design rules (Intel)



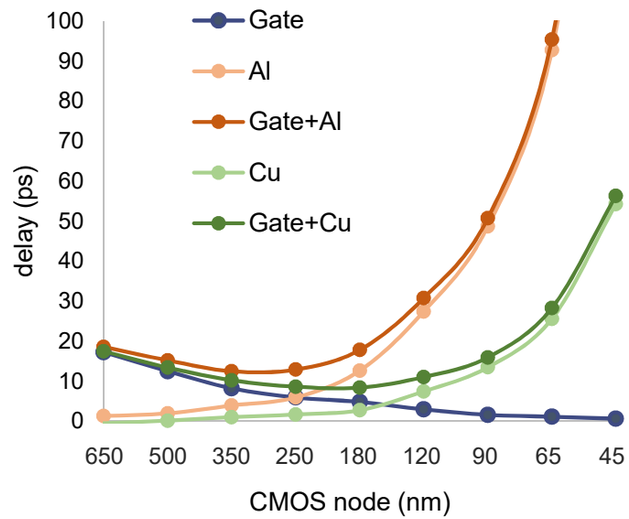
Al lines / W vias
SiO_2 dielectric



Cu line & via
Low-k dielectric



Intel 14nm CMOS BEOL



$$I_{ON} = \frac{1}{2}\mu_0 . C_{ox} . \frac{W}{L} . (VG - VTh)^2$$

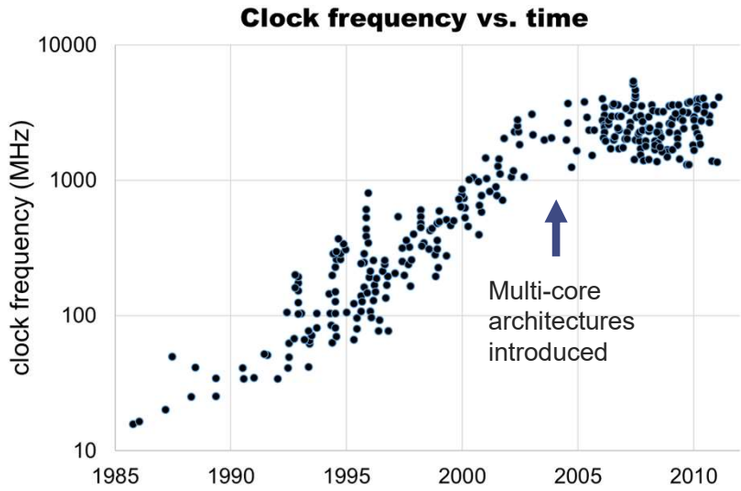
$$\tau_{gate} = \frac{C_G \, V_{DD}}{I_{ON}}$$

$$\tau_{interconnect} \propto RxC$$

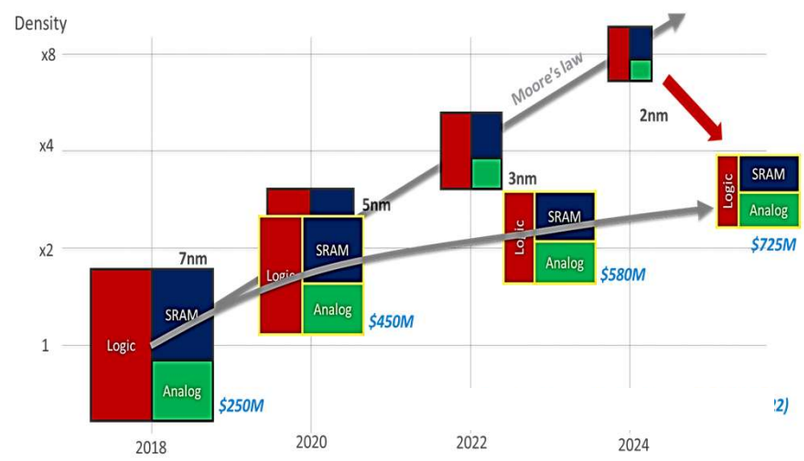
- **R.C delay has become a major performance issue**

New paradigms are needed

- **Interconnects Bottleneck**
  Circuit frequencies limited
  Limited bandwidth between chips
- **Scaling becomes costly**
  High manufacturing cost, low yield with large die
  High development cost: masks, IP porting, verif…
- **Heterogeneous architectures needed**
  More processing: AI, perception accelerators…
  More data to handle: memory capacity, fusion…
  More modularity, scalability & sustainability



A. Danowitz (Stanford University)

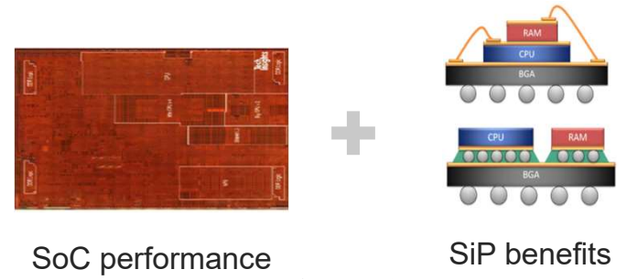


Cost of advanced designs (IBS, July 2022)

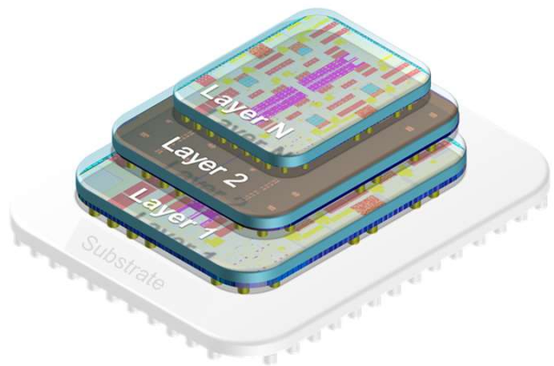
How to reach them ?

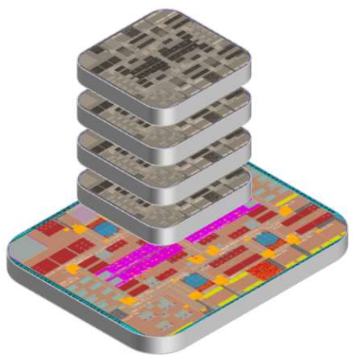
3D benefits for advanced systems

- **Best of all trends: Moore + more than Moore**
  System on Chip performance + System in Package diversity
- **High-performance interconnections**
  Low R, L, C + massively parallel vertical processing
- **Modern answers to design needs**
  Partitioning, IP reuse, scalability & density, hetterogeneity

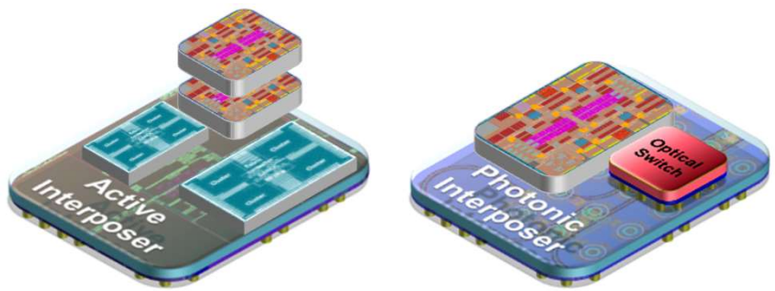


SoC performance SiP benefits

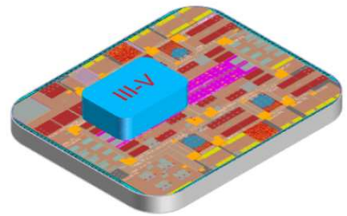




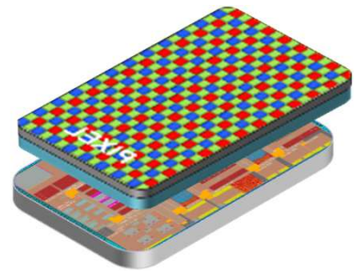
Memory on Logic



Chiplet-based integrations



III-V on Logic



Sensor on logic

2.

3D integration toolbox

Morphology of a 3D circuit

- **<u>Thin</u> stacked layers**

  Layer 1 (# bottom die) / (…) / Layer N (# top die)

- **Layer-to-layer vertical interconnects**

  Miniaturization trend: pillars, hybrid bonding …

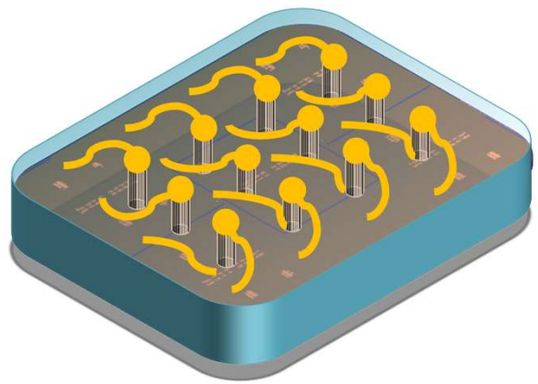
- **Intra-layer vertical interconnects**

  Communication between frontside and backside of each layers

  Through silicon Vias (TSV)

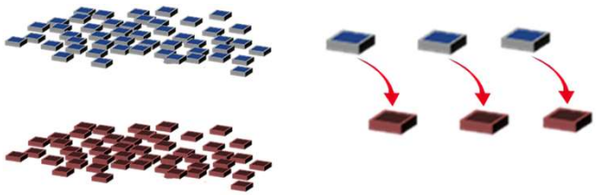
- **Intra-layer in-plane interconnects (2D)**

  ReDistribution Layers (RDL)



Assembly configurations

Die to die

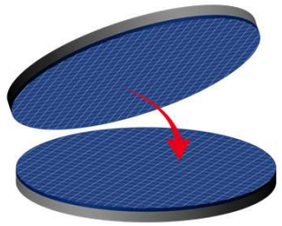


- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

- Low assembly throughput
- Low alignment accuracy
- Very high cost

Pure packaging operation

Wafer to wafer

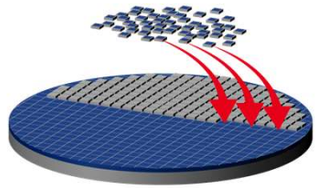


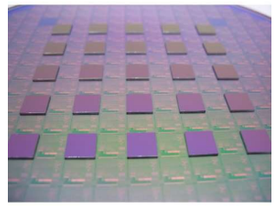
- Collective process
- High assembly throughput
- High alignment accuracy

- Yield loss
- Strong design limitation

Mass production for image sensors and memories

Die to wafer





- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

- Low assembly throughput
- Low alignment accuracy

Breakthrough processes needed

Wafer bonding techniques

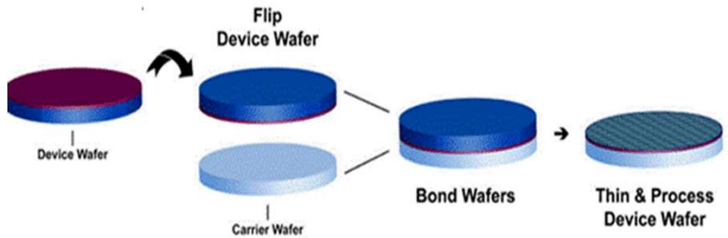
- **Why & how ?**

  Thin wafer processing (<300µm)

  Wafer-to-wafer 3D stacking

  Temporary or permanent bonding

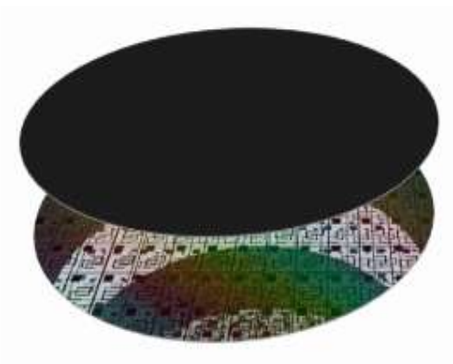
50 µm thin silicon wafer

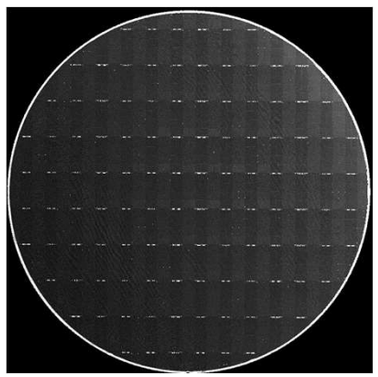


Thin wafer processing on carrier

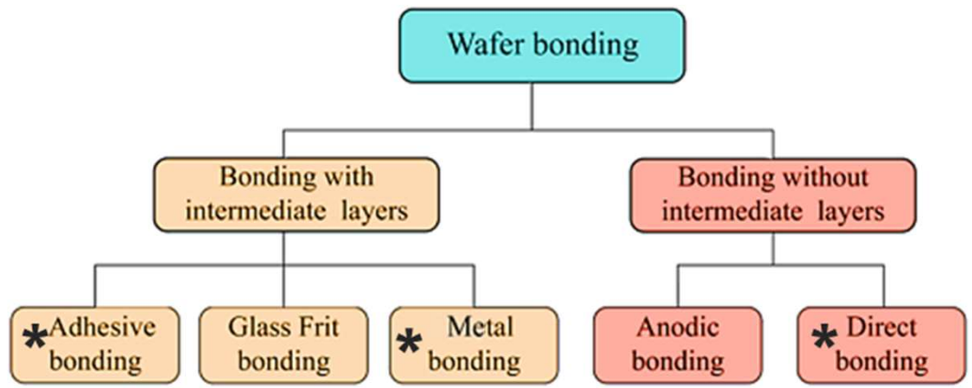
- **A wide range of processes**

  Each with own strengths and weaknesses





Scanning acoustic microscopy



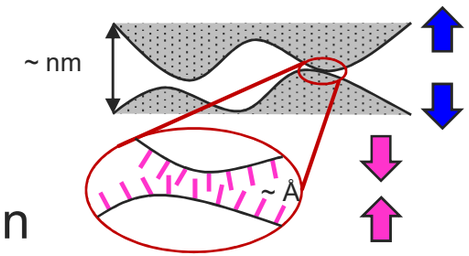
* mostly used processes for 3D-IC purpose

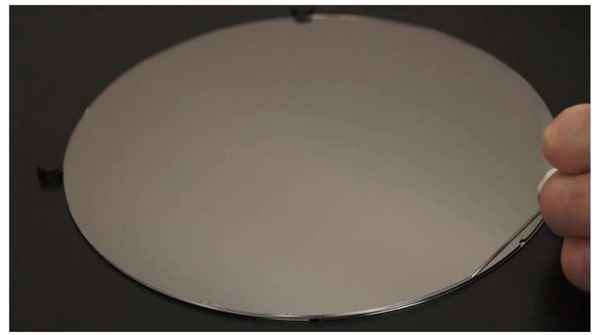
Direct bonding process

- **Bonding without added material**

  Based on attraction of very smooth surfaces

  Flatness & cleanliness at all scales → planarisation





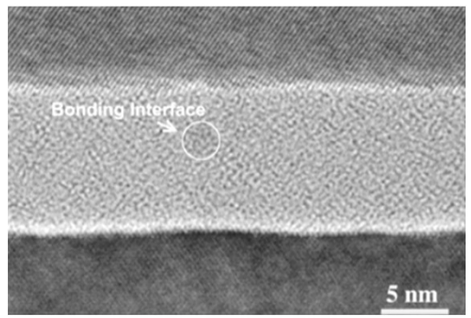
Bonding wave: glass to Si & Si to Si bonding

- **SiO_2/SiO_2 bonding**

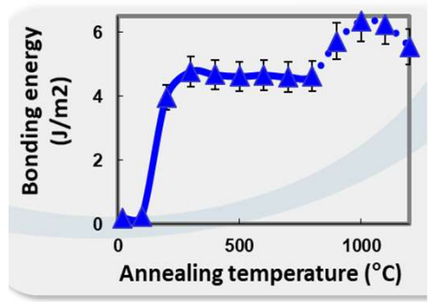
  Required roughness < 0,65nm rms [1]

  Van der Waals interaction at T_{amb}

  Covalent bonds formed after annealing



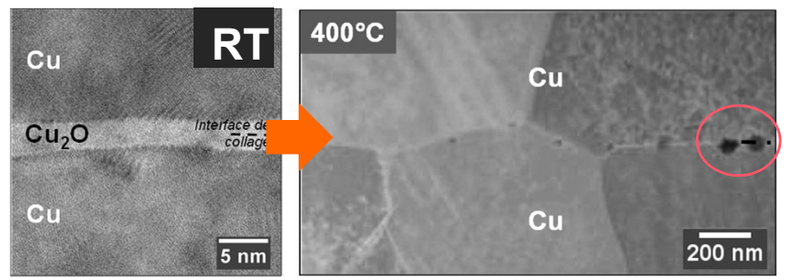
SiO_2/SiO_2 interface after annealing



- **Cu/Cu bonding**

  Required roughness < 0,5nm rms [2]

  Cu recrystallization during annealing > 200°C [3]



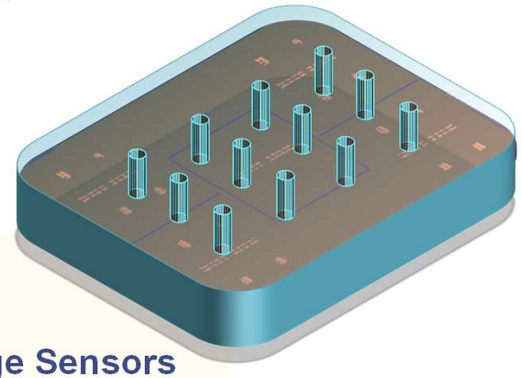
Cu/Cu interface before/after annealing

[1] F. Rieutord, et al. *ECS Trans.,* vol. 3, no. 6, pp. 205–215, 2006

[2] H. Moriceau, *Microelectronics Reliability*, vol. 52, no. 2, pp. 331–341, 2012

[3] L. Di Cioccio, et al., *J. Electrochem. Soc.,* vol. 158, no. 6, pp. P81–P86, 2011

Through silicon via (TSV) technologies

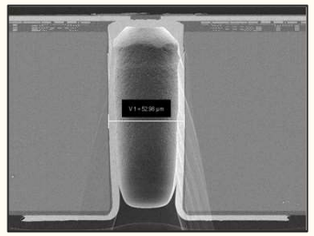
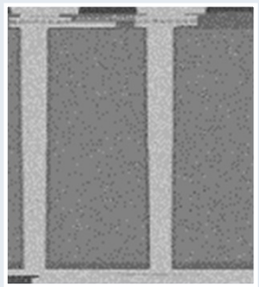
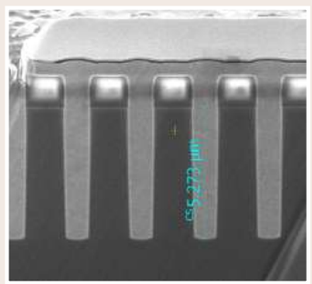


TSV pitch

100-500µm
Ø 40-100µm
R_{TSV} = 2-10 mΩ
C_{TSV} = 2 pF

20-50 µm
Ø 2-15 µm
R_{TSV} = 20 mΩ
C_{TSV} = 0.1 pF

1-10 µm
Ø <2 µm
R_{TSV} = 0,5-1 Ω

TSV last low density		100 TSV/mm^2 ➔ low I/O count	**CMOS Image Sensors** **X-Ray focal plane arrays** **IR sensors**
TSV middle		1 000 TSV/mm^2 ➔ Core/Chips	**System in Package** **Interposers / Chiplets**
High density TSV		100 000 TSV/mm^2 ➔ Logic blocs	**3D Imagers** **Displays** **Power Delivery Network**

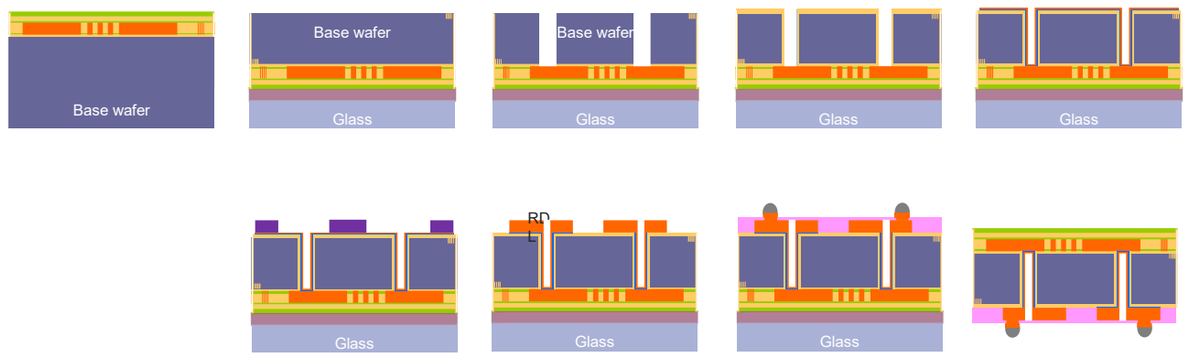
“TSV last” low density process

- **Done <u>after</u> full CMOS process [4]**

  Wafer bonding on carrier & low temp. process

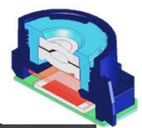
  AR (= height/diameter) increased over time

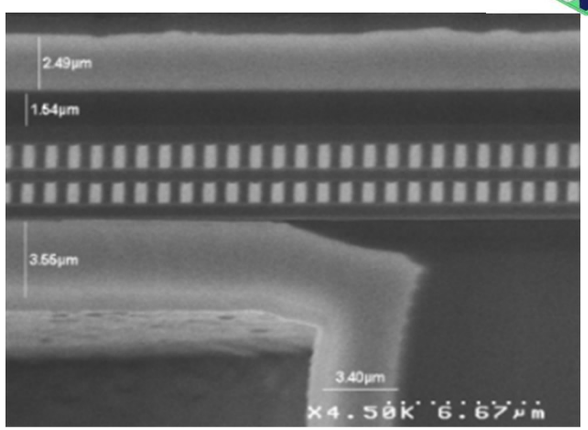
  Keep out zone + alignment → area penalty



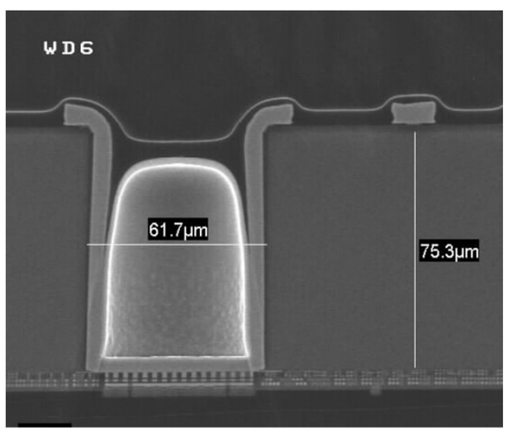
- **Industrially mature since 2008**

  CMOS image sensors

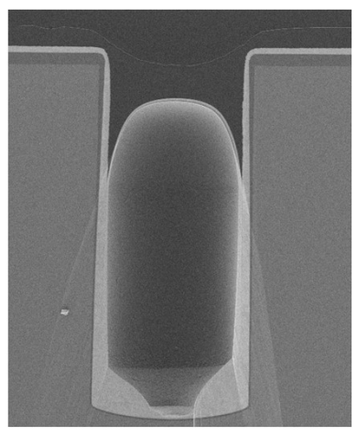




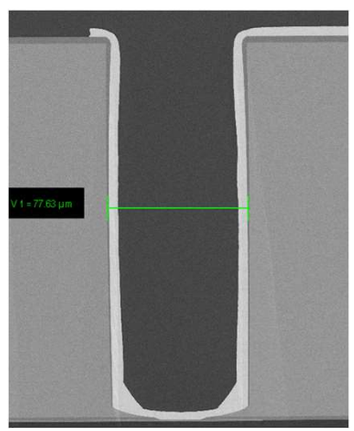
TSV contact on Metal1 layer



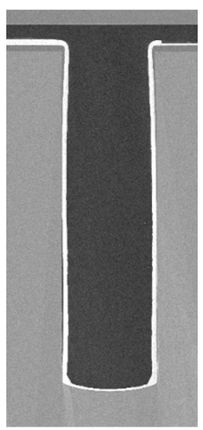
AR 1,2 after passivation



AR 2 after passivation



AR 2,5 after RDL



AR 3,7

AR

[4] D. Henry et al., Electronic Components and Technology Conference, 2008

“TSV middle” process

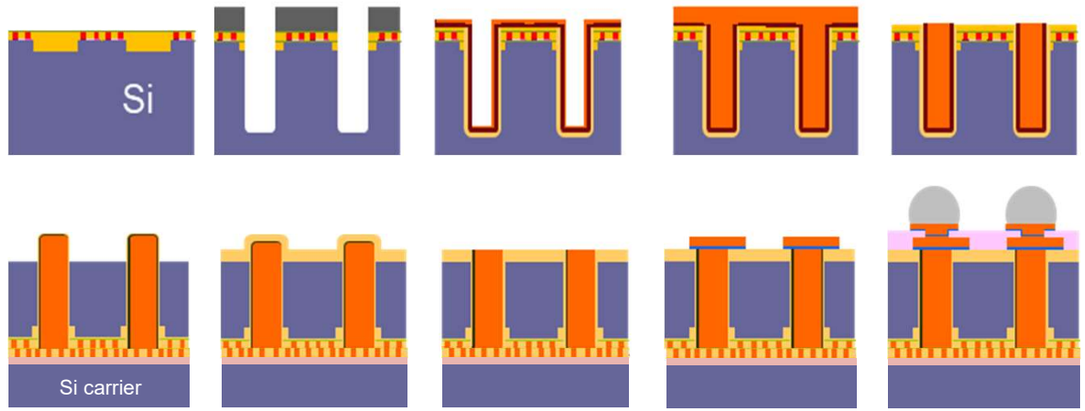
- **Done <u>during</u> CMOS process [5]**

  Aspect ratio usually > 10, Diameter 2-15 µm

  TSV etched & filled with Cu prior to BEOL process

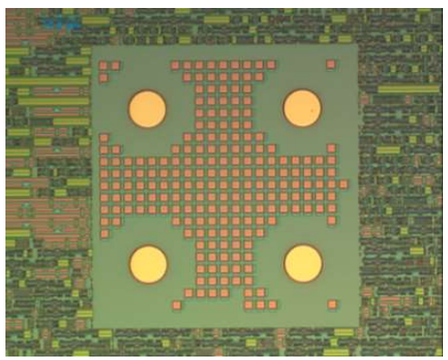
  TSV revealed on backside after Si thinning

  Reduced keep out zone vs. TSV last

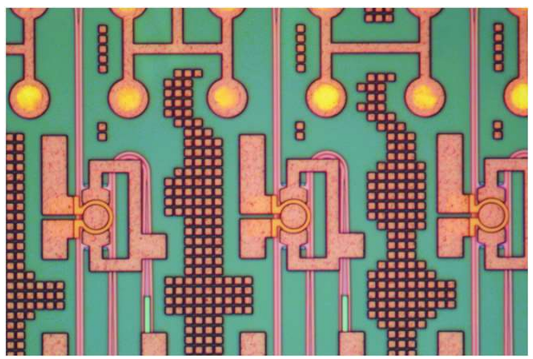


- **Industrially mature since 2013**

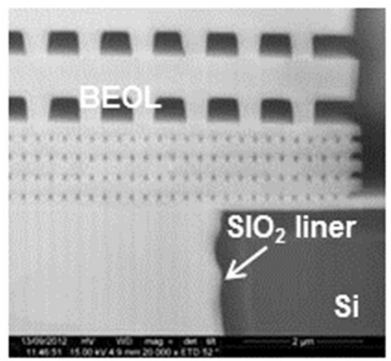
  FPGA (Xilinx), DRAM stacks



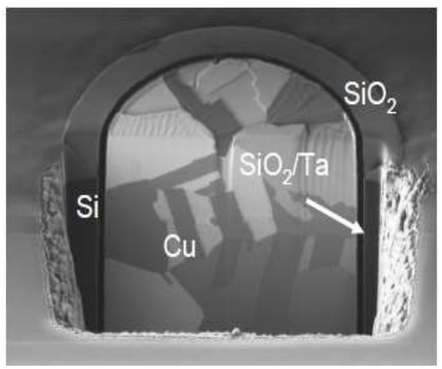
TSV Middle after CMP



TSV co-integrated with microring resonators



TSV & CMOS BEOL



TSV structure

[5] P. Coudrain et al., EPTC 2012

“High density TSV” (HD-TSV) process flow

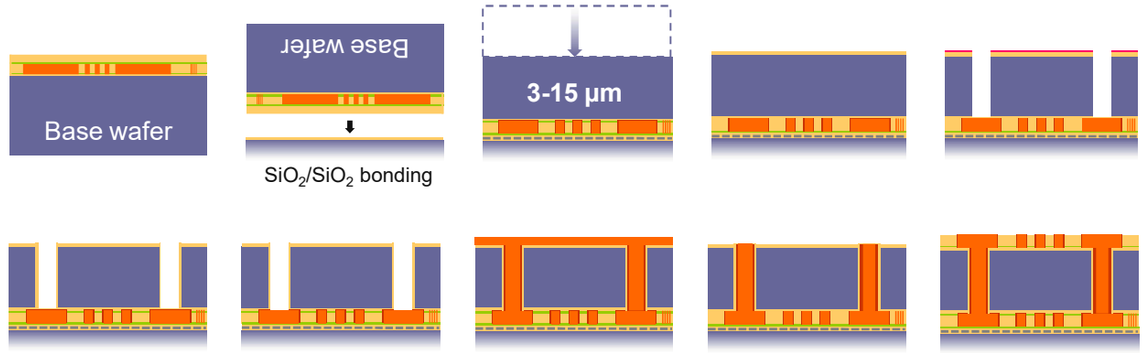
- **Done <u>after</u> circuit processing [6]**

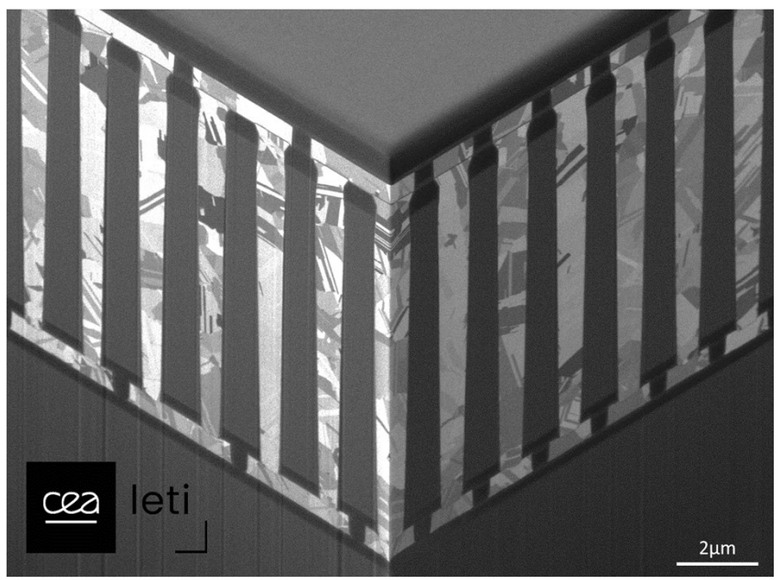
  Diameter typically < 2µm & height <15 µm

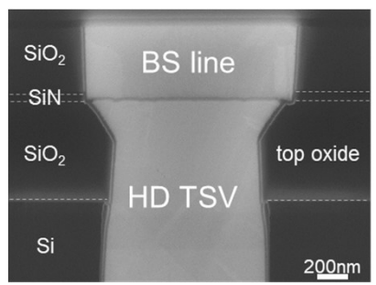
  Ultra-uniform Si thinning (TTV < 1µm) → direct bonding

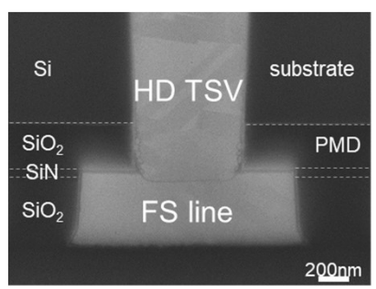
- **R&D activity**

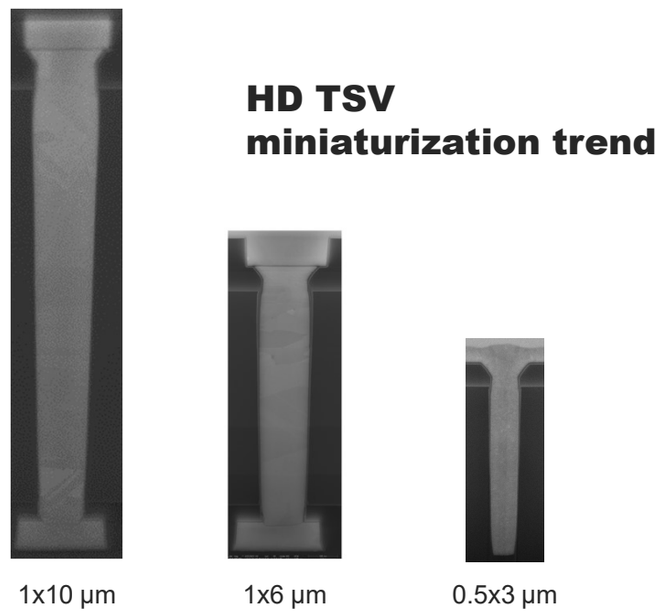
  Power delivery network (PDN), SPAD arrays





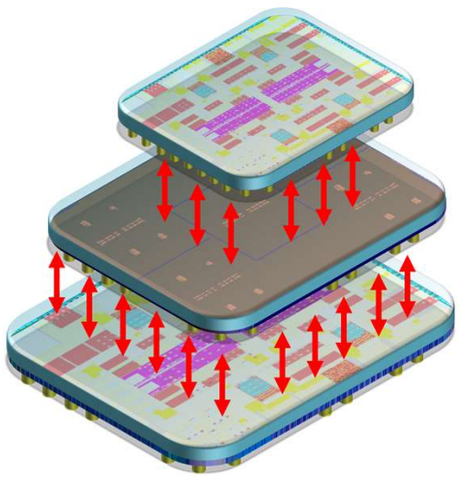




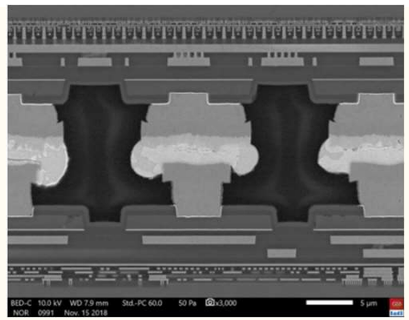
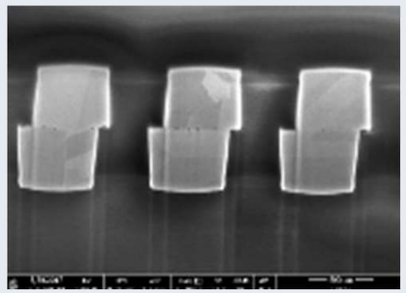
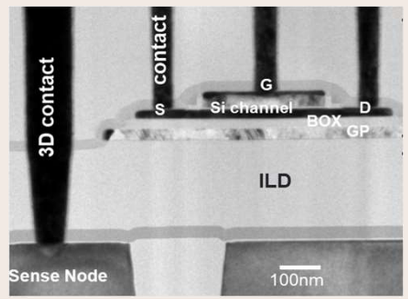


[6] S. Borel et al., ECTC 2023

Layer-to-layer 3D interconnects



3D pitch

3D pitch				
> 100µm	**Solder-based**		10^3/mm^2 Circuit level	**Die to Die** **Die to Wafer** **Wafer to Wafer**
100nm-10µm	**Hybrid bonding**		10^6/mm^2 Logic-block level	**Die to Wafer** **Wafer to Wafer**
<100nm	**Sequential 3D**		10^8/mm^2 Transistor level	**Wafer to Wafer**

Solder-based interconnects for flip-chip

- **Solder material choice linked to temperature**

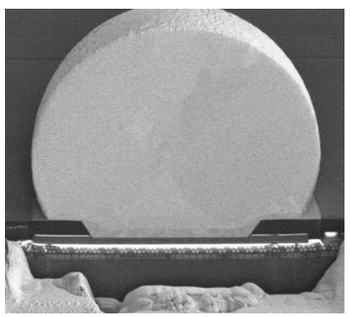
  SnPb (183°C), SnAg (221°C), (…) In (152°C)

- **Interconnects processing**

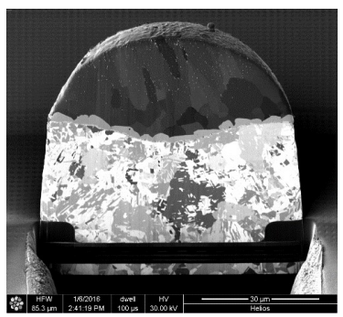
  Paste printing, ball serigraphy for large geometries

  Semi-additive process (ECD) for reduced pitch

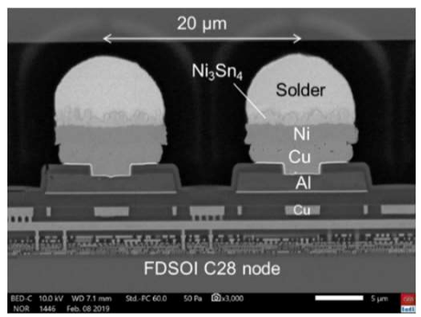
  Polymer underfill systematically added in free space



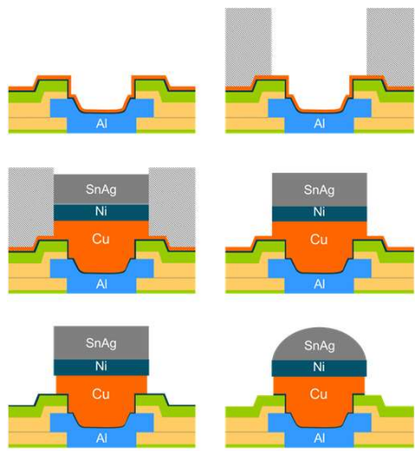
200µm diameter SnAgCu
Paste printing



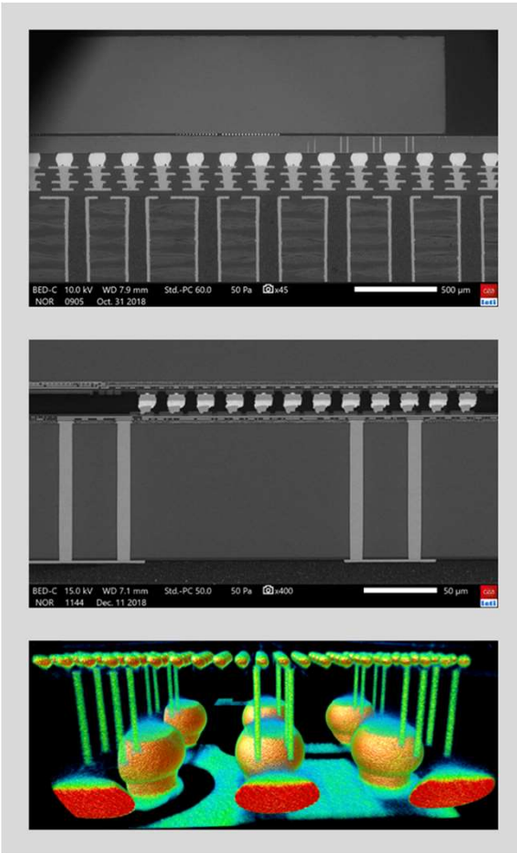
70µm diameter Cu/SnAg
ECD



10µm diameter Cu/SnAg Pillars
ECD



Semi-additive process



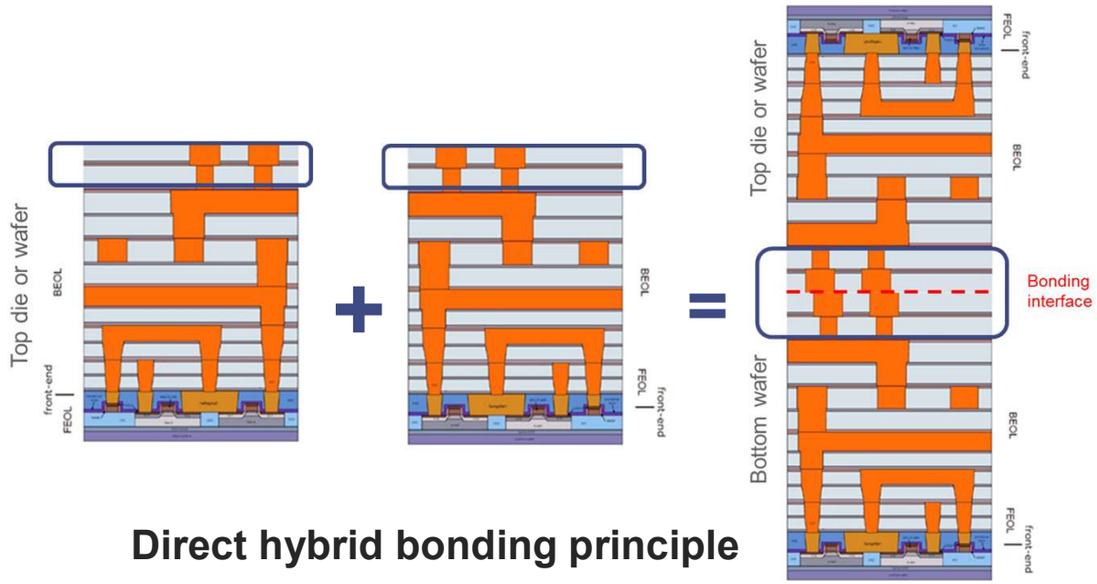
2-layer stack on BGA: 10µm Pillars between top and bottom and 70µm bumps between bottom and BGA [7]

- **Well mature technique, but limited in density**

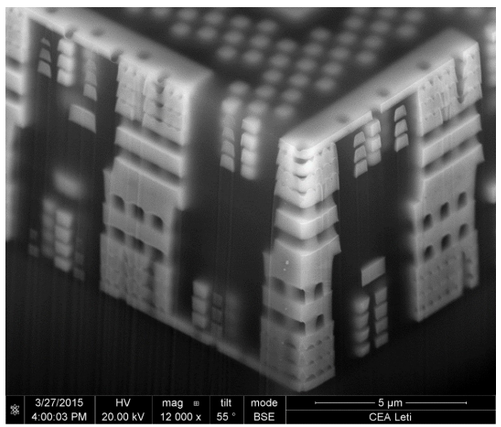
[7] P. Coudrain et al., ECTC 2019

Direct hybrid bonding process: a hot topic !

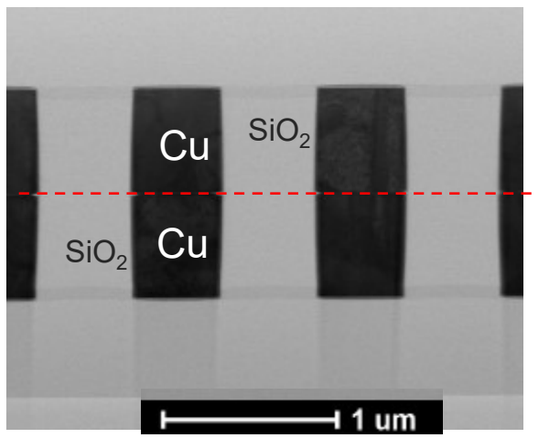
- **Mix SiO_2/SiO_2 & Cu/Cu bonding**
  Precautious chemical mechanical polishing
  Specific design rules to control dishing in Cu
- **Unprecedented interconnect pitch**
  1 µm pitch demonstrated in 2017 [9], 0.4 µm in 2024
  Precision alignment is key: 50nm expected in 2025

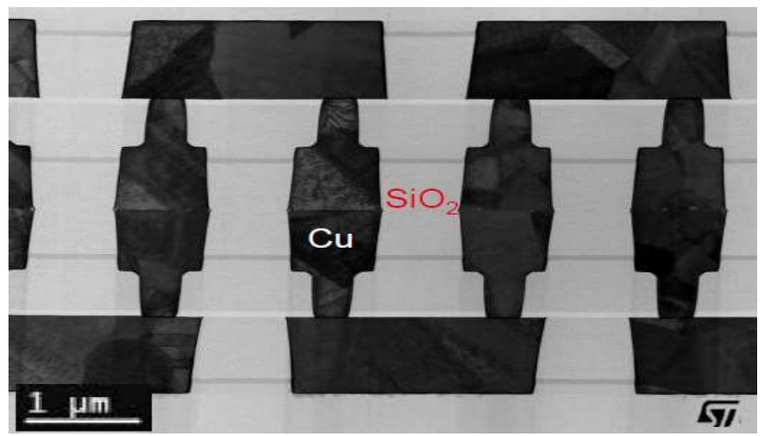


Direct hybrid bonding principle



[8] Y. Beilliard, PhD Thesis, Univ. Grenoble Alpes, 2015

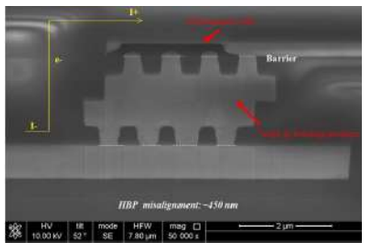




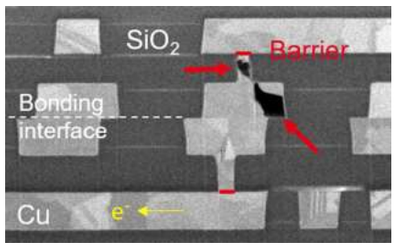
[9] J. Jourdon et al., IEDM 2018

Extensive reliability studies on hybrid bonding

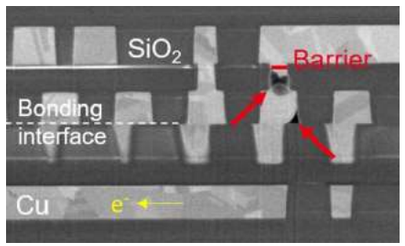
Electromigration performance vs. pitch reduction



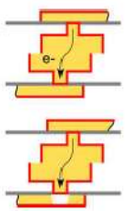
7.2 µm pitch

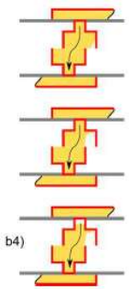


3.4 µm pitch



1.4 µm pitch

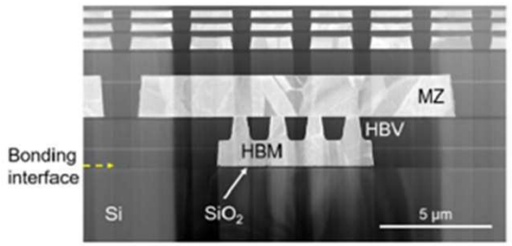




- With pitch reduction, EM defect moves from BEOL to hybrid bonding levels, but **extrapolated lifetimes are not affected at use conditions** [10,11]

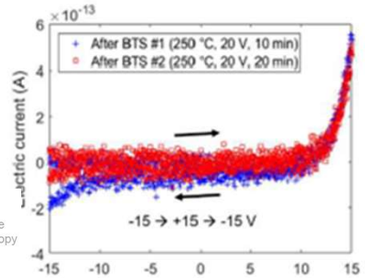
[14] S. Moreau et al., ECTC 2016
[15] S. Moreau et al., IRPS 2023

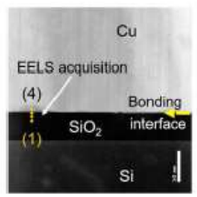
Susceptibility to Cu diffusion ?

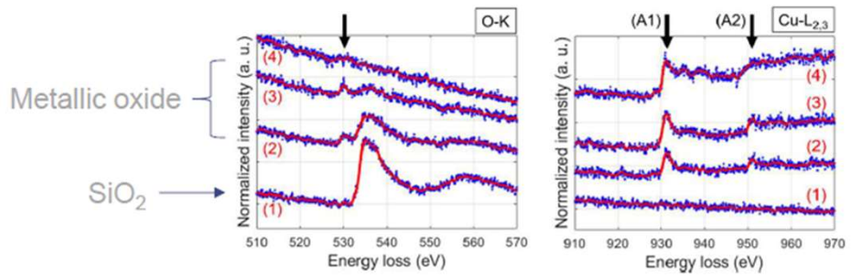


BTS + TVS

BTS: Bias Temperature Stress
TVS: Triangular Voltage Sweep
TEM: Transmission Electron Microscope
EELS: Electron Energy Loss Spectroscopy







- **No diffusion identified**, thanks to the presence of 3 nm Cu_2O layer barrier, stable with time and temperature

[16] Ayoub et al., IRPS 2022
[17] Ayoub et al., Micro rel. 2023

Hybrid bonding with Cu/SiCN (imec)

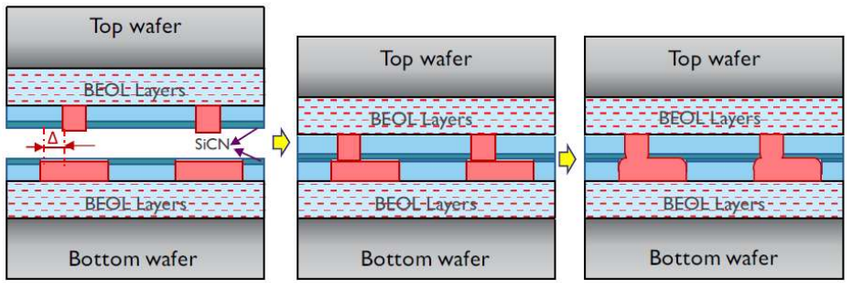
- **Hybrid surface Cu/SiCN [13]**

  Annealing down to 250°C with SiCN

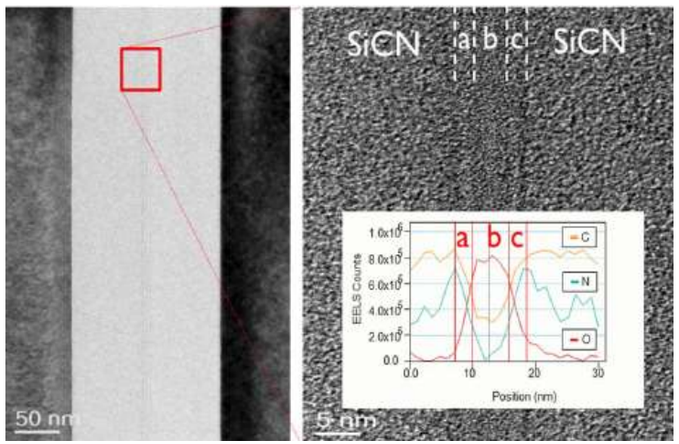
  Cu protrusion on top wafer

  Cu recess on bottom wafer

- **Dissymmetrical pad sizes**



Process flow for SiCN hybrid bonding



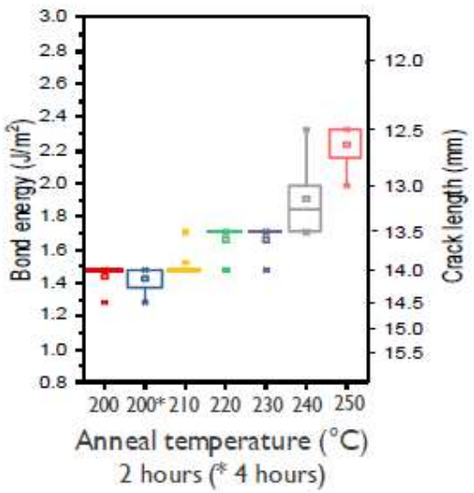


Fig. 11. TEM 540 nm pad on 1260 nm pad array at 1.8 µm pitch.

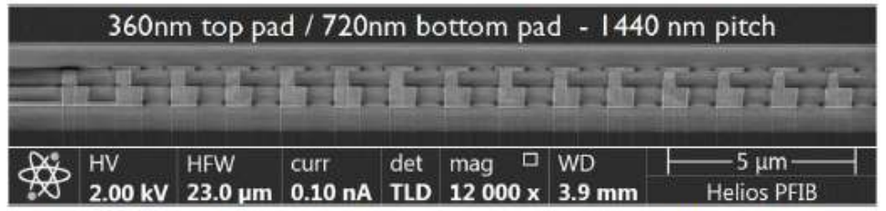


Fig. 13. FIB-SEM cross section; 360 nm pad on 720 nm pad at 1.44 µm pitch.

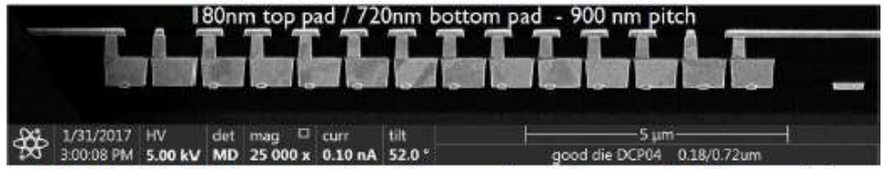


Fig. 15. FIB-SEM cross section; 180 nm pad on 720 nm pad at 0.9 µm pitch.

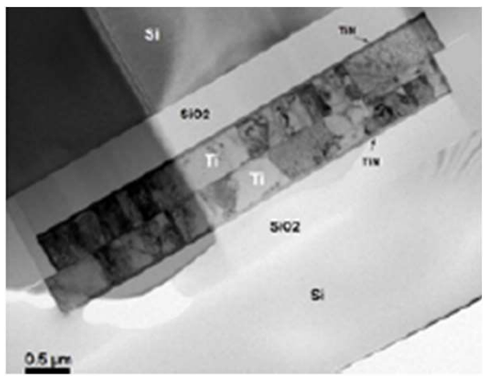
[13] E. Beyne et al., IEDM 2017

Non Cu-based bonding

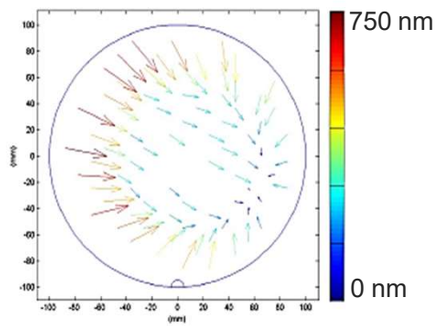
- **Ti/Ti hybrid bonding [18]**

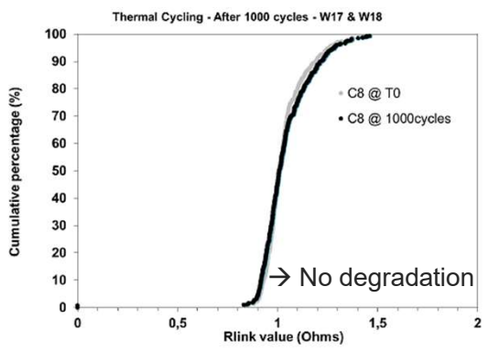
3x3 µm² pad, 7 µm pitch with sub-µm alignment

Reliability & RF characterisations up to 40 GHz



Interface after thermal storage (top) and thermal cycling (bottom)

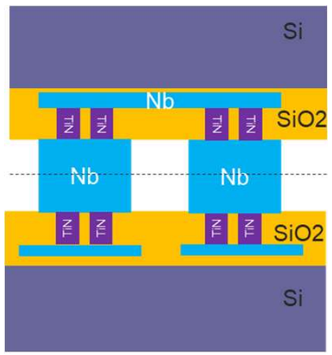


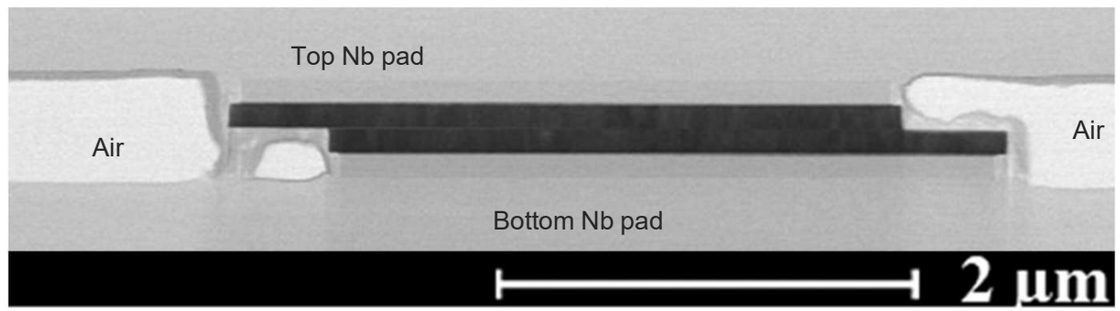


- **Nb/Nb bonding [19-20]**

Superconducting interconnects

3x3 µm² pad, 7 µm pitch with sub-µm alignment





[18] A. Jouve et al., ECTC 2020
[19] P. Renaud et al., ECTC 2024
[20] J. Charbonnier, ESTC 2024

Die-to-wafer hybrid bonding challenges

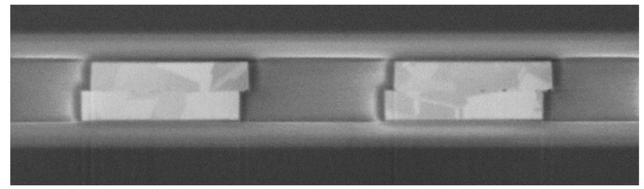
- **Known Good Die strategy [21-22]**

  Probing marks to make compatible with bonding

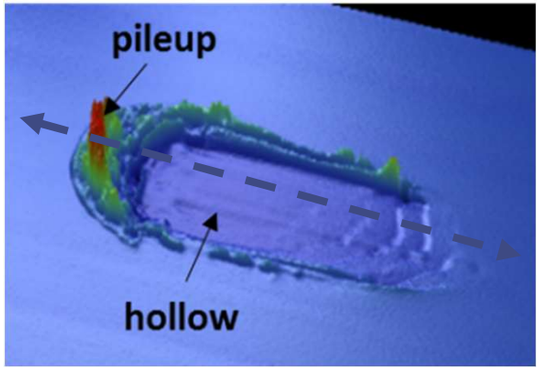
- **Pitch reduction trend [23]**

  Alignment precision is the key to success

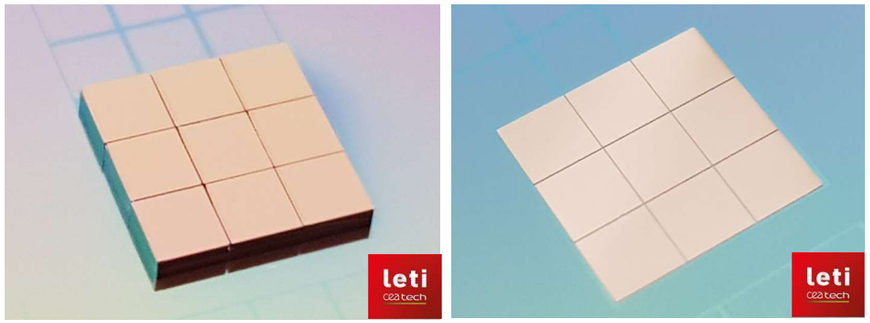
  Multi-pitch for design flexibility, reduced interdie-space



5µm interconnection pitch

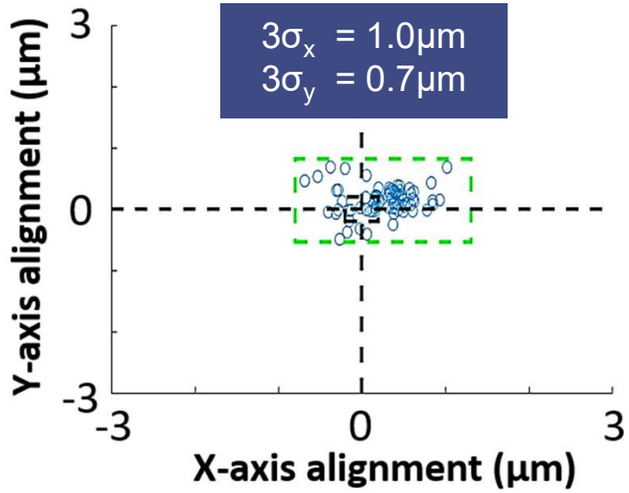


Probing marks



3 x 3 mm² | 3 x 3 mm² post thinning

Die-to-wafer integration with 40µm inter-die spacing [24]



Alignment precision for 5µm pitch

- **500nm D-T-W alignment precision is expected in 2024-25**

[21] E. Bourjot et al., 3DIC 2019
[22] E. Bourjot et al., ECTC 2021
[23] E. Bourjot et al., ESTC 2022
[24] P. Metzger et al., Minapad 2022

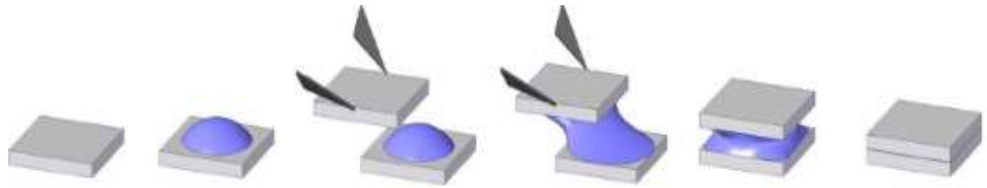
Self-assembly approach for hybrid bonding

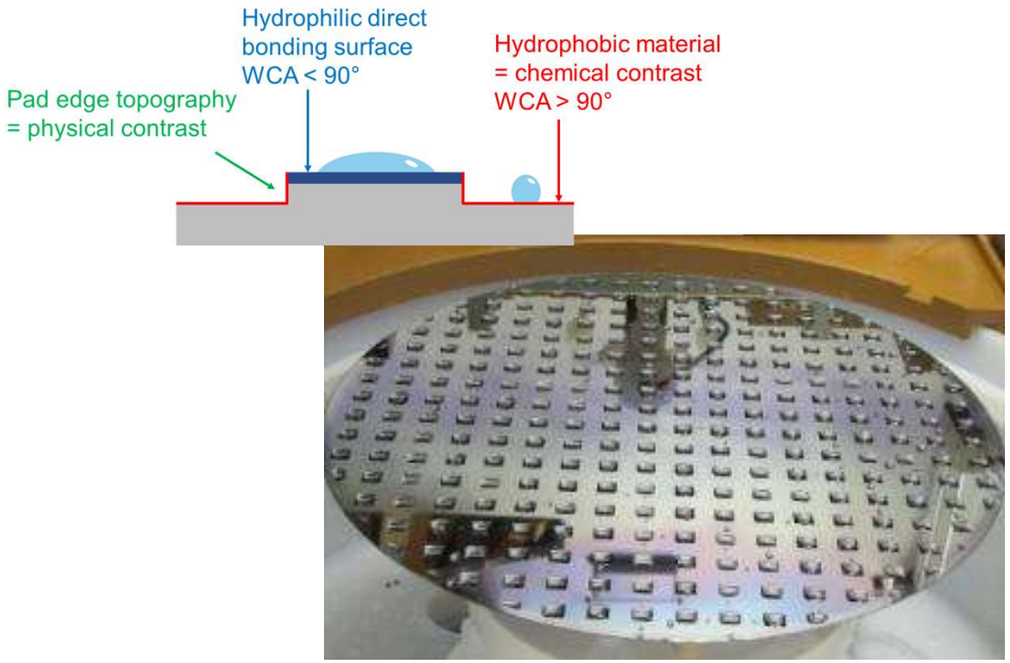
- **Capillary-assisted process** [25-27]

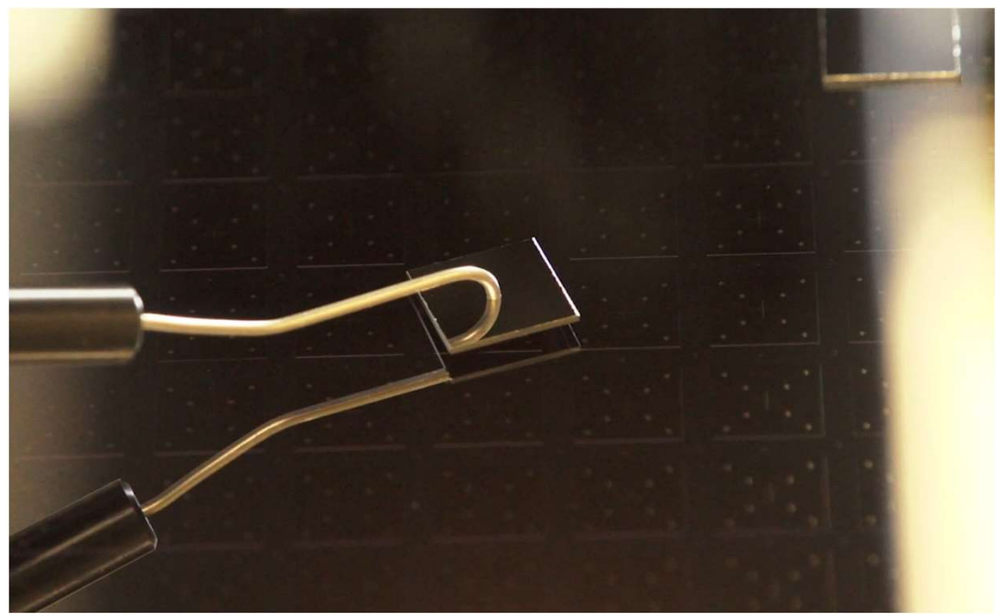
  Drop of water between chip and substrate

  Liquid capillary tension minimizes surface energy

  Water confinement controls alignment accuracy







[25] S. Mermoz, PhD thesis, Univ. Grenoble, France, 2015
[26] A. Jouve et al., ECTC 2019
[27] A. Bond et al., ECTC 2022

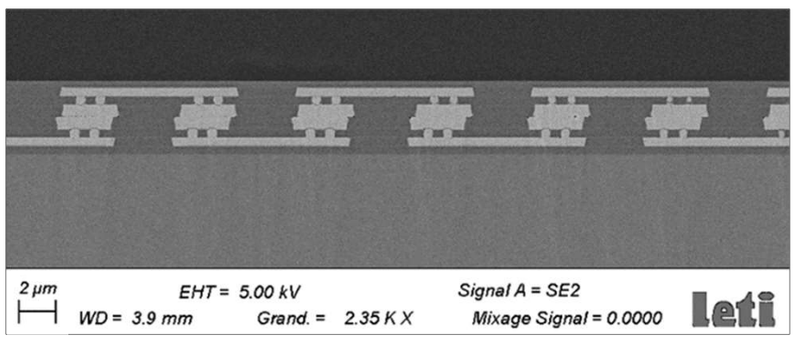
Self-assembly performance [28]

- **Electrical performance**

  Daisy chains up to 50 000 connexions with resistance similar to standard die-to-wafer hybrid bonding

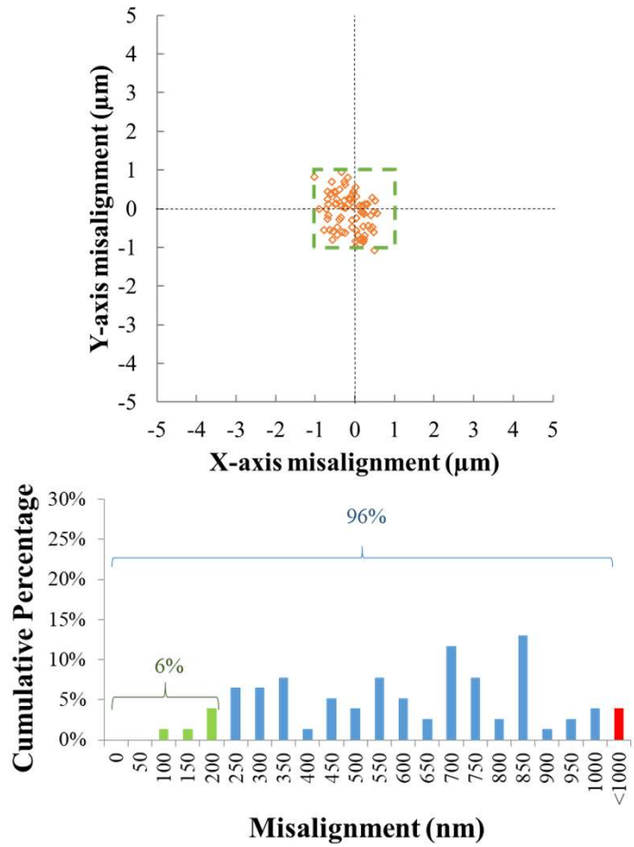
- **Alignement performance**

  Better ultimate alignment is achieved with self-assembly

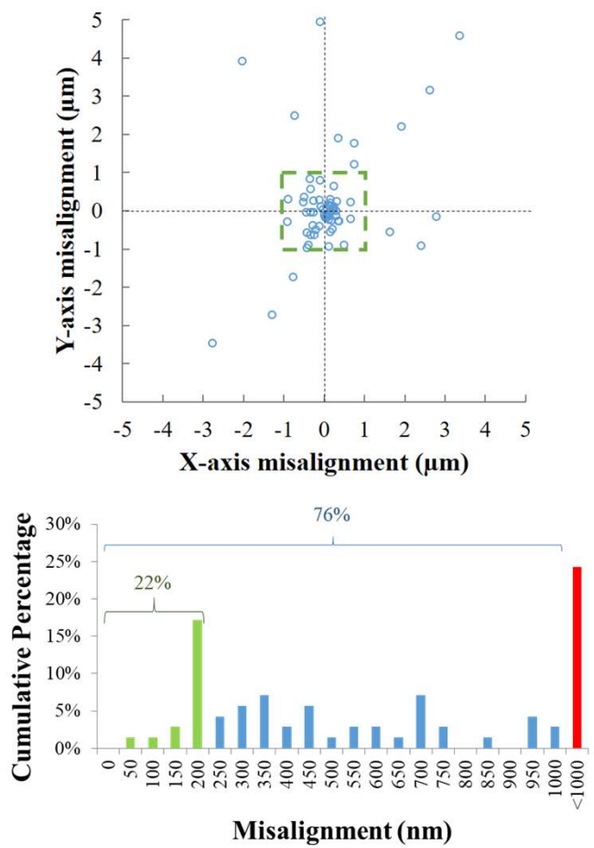


Self aligned daisy chains

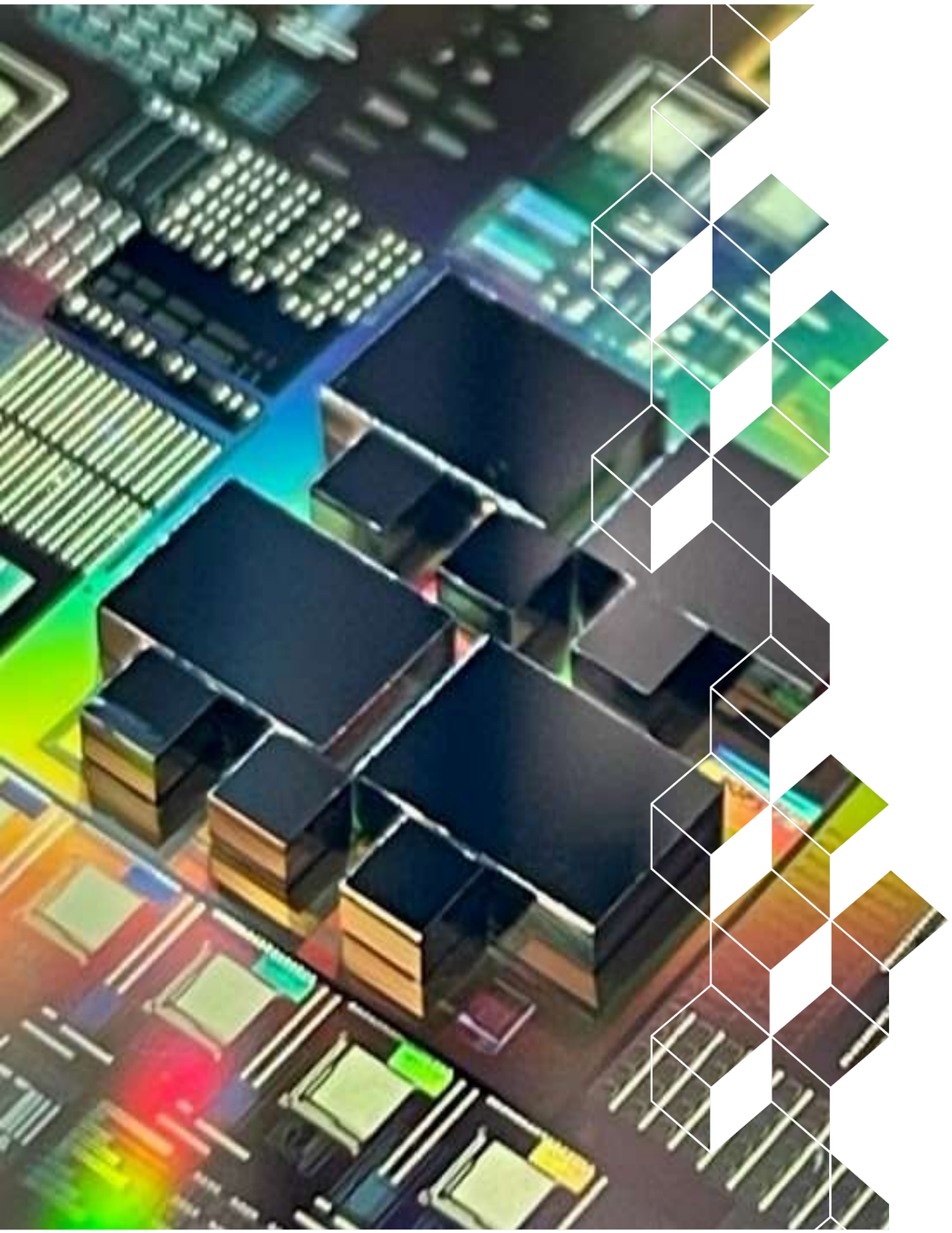
Standard bonding



Self-assembly bonding



[26] A. Thiolon et al., ESTC 2024



3.

Fields benefiting from 3D architectures

(a few)

Benefits of 3D Integration for image sensors

- **Dimensions**

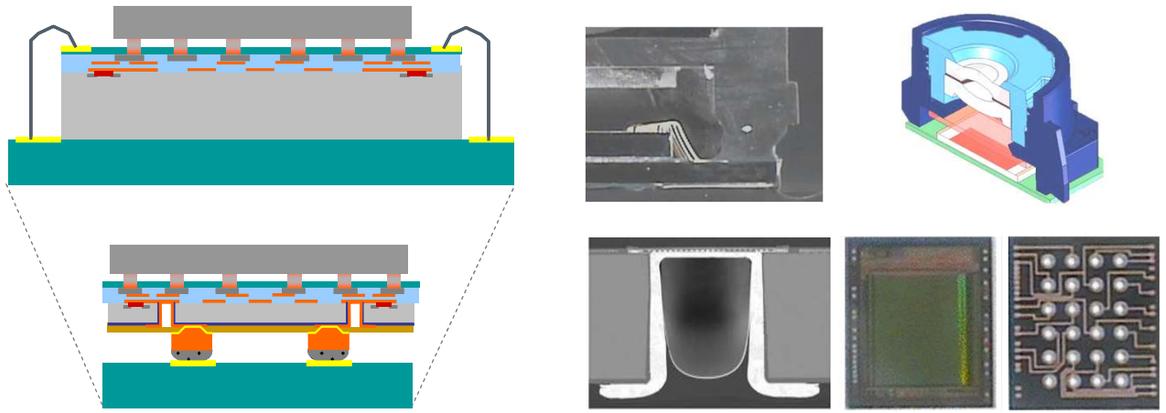
  Reduced form factor (x,y,z)

  Abuttable sensors for RX & IR sensing

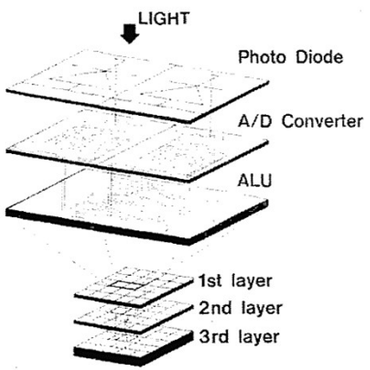
- **New architectures!**

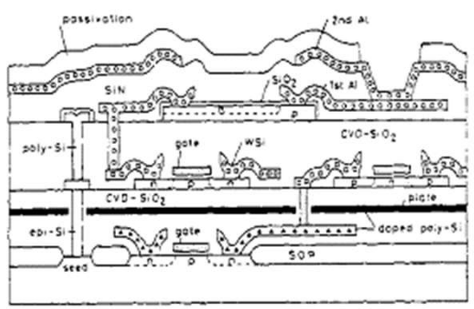
  Parallel pixel processing

  Layers functionalization & optimization



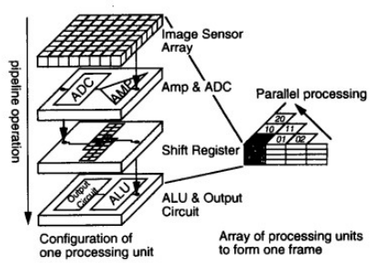
[4] D. Henry et al., Electronic Components & Technology Conference, 2008

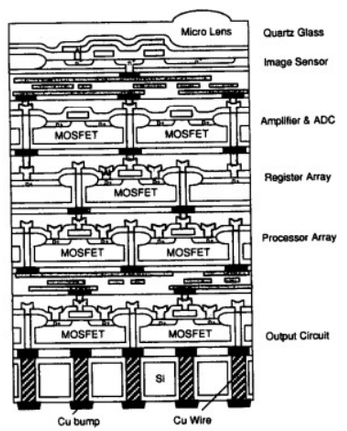




Mitsubishi [29]

[29] T. Nishimura et al., IEDM, 1987





Tohoku University [30,31]

[30] H. Kurino et al., IEDM, 1987

[31] T. Tanaka et al., IEDM, 2007

3D image sensor integrated by µbumping

- **CMOS image sensor with image signal processor (ISP) [32]**

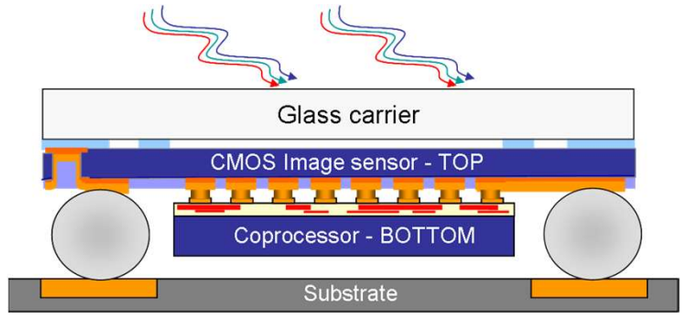
  Compactness & energy efficiency improvement

- **3D technology features**

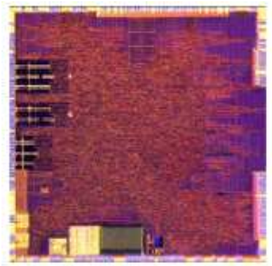
  1.4µm pixel CIS with TSV last integration

  ISP with Fan-In RDL & µbumps

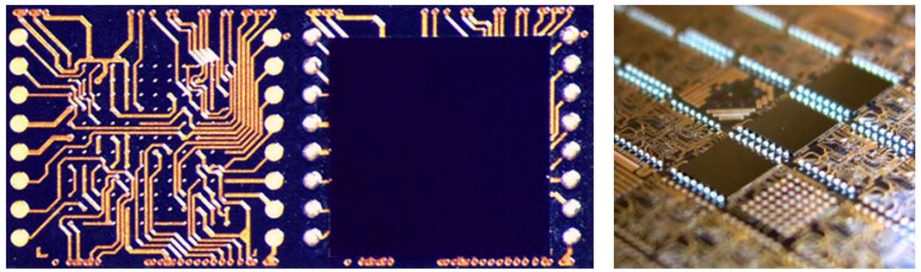
  ISP bumping on CIS backside



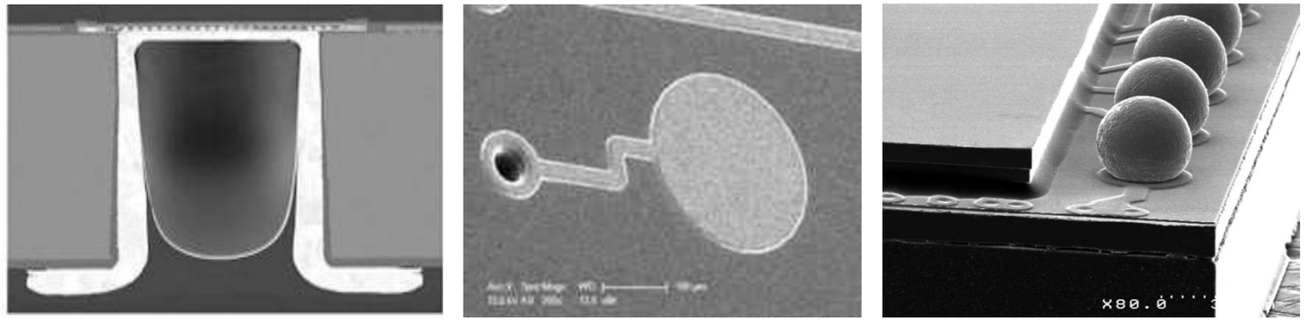
3D sensor cross section



	CMOS	BEOL	I/O count	Dimensions
Image sensor	130 nm	3ML + AP	80	5.0x4.4 mm^2
Coprocessor	65 nm	7ML + AP	164	3.4x3.5 mm^2



CIS backside without & with ISP stacking



Post-balling overview

[32] P. Coudrain et al., Electronic Components & Technology Conference, 2013

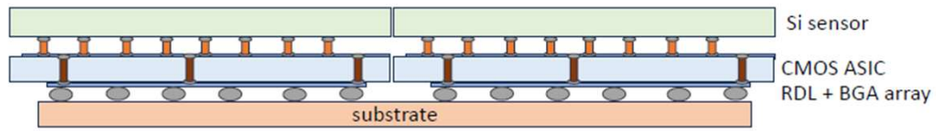
Medipix hybrid pixel detectors

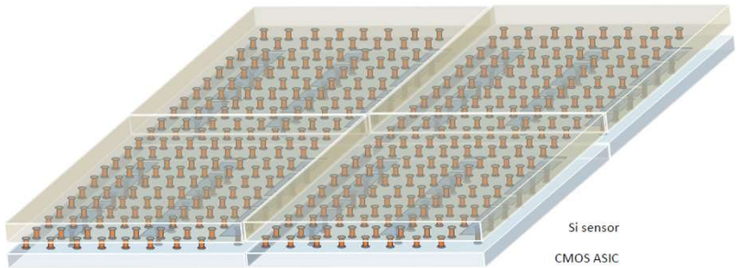
- **Abuttable detector on ROIC**

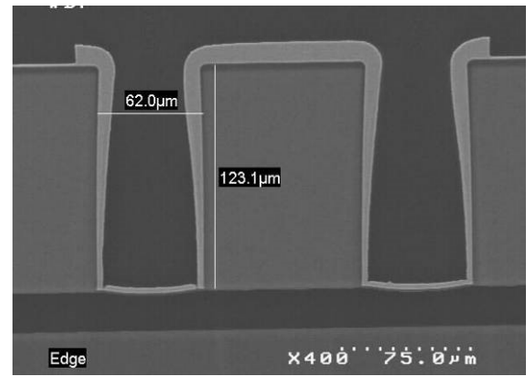
  Abuttable sensors assembly with no dead zone

  TSV last integration, 100 TSV per chip [33]

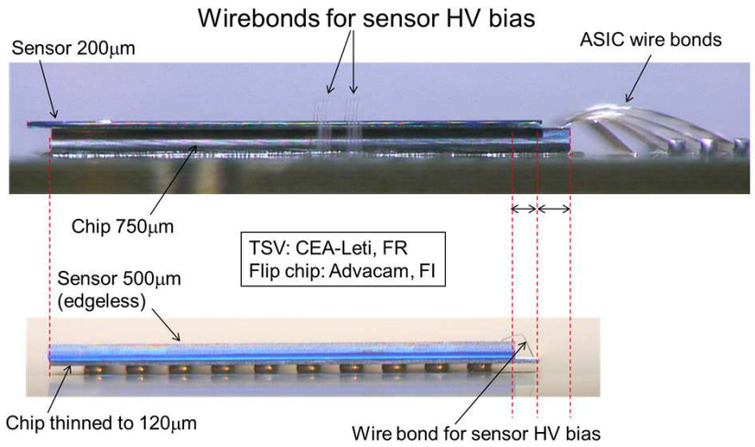
  Height 120 µm, diameter 60 µm

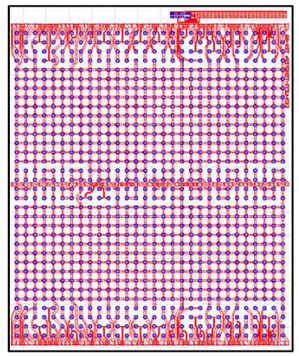




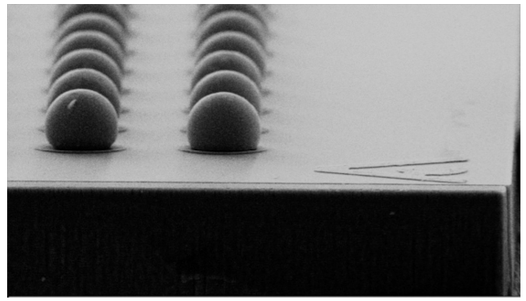


LHCb Vertex Locator





24x30mm

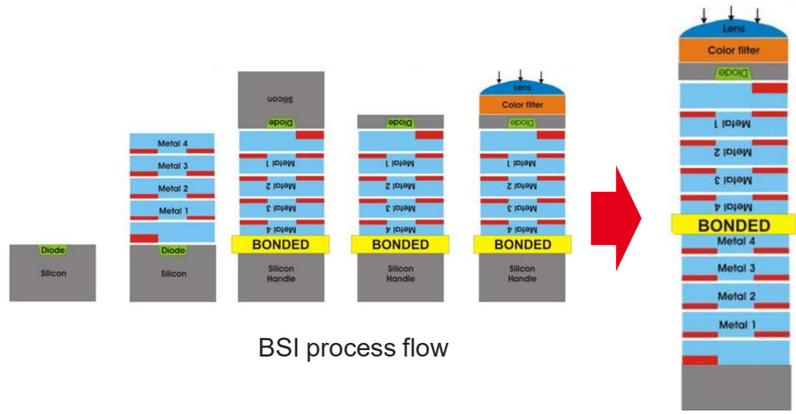


TSV & backside SEM views

[33] D. Henry et al., ECTC 2013

Backside illumination as enabler for 3D CIS

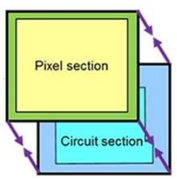
- **Backside illumination process requires wafer bonding on a carrier. There's just one step to 3D integration: replace carrier by a functional wafer!**

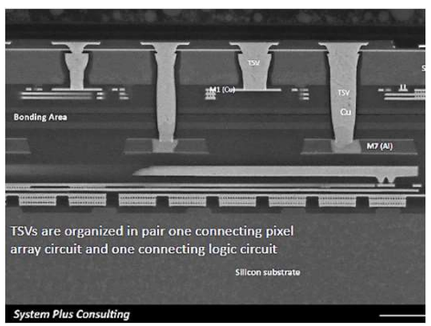


BSI process flow

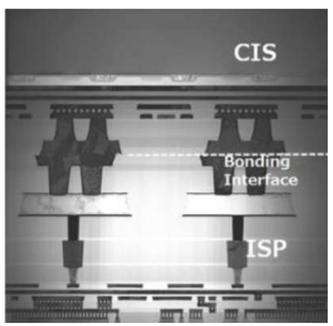
- **2-layer CIS (2013)**

  Oxide bonding [34] followed by hybrid bonding [35]





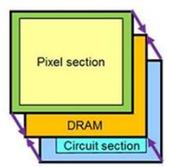
SiO2/SiO2 bonding

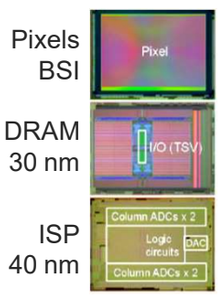


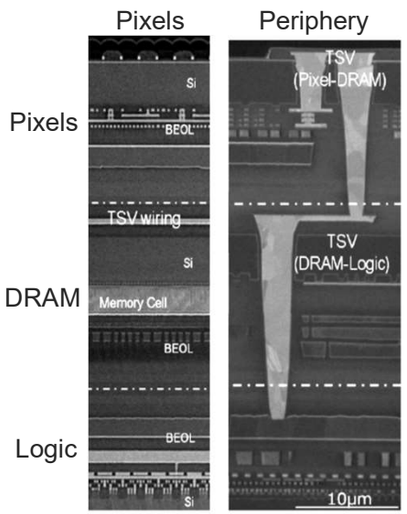
Hybrid bonding

- **3-layer CIS (2017)**

  Intermediate DRAM layer [36]







[34] Sony ISX014 1/4 Inch 8 MP, 1.12 µm Pixel Size Exmor RS Stacked Back Illuminated CIS Imager Process Review
[35] Y. Kagawa et al., IEDM, 2016
[36] H. Tsugawa et al., IEDM, 2017

Smart imager developments

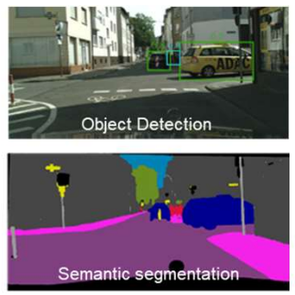
- **From imagers to vision sensors**

  Edge-AI applications for autonomous vehicle

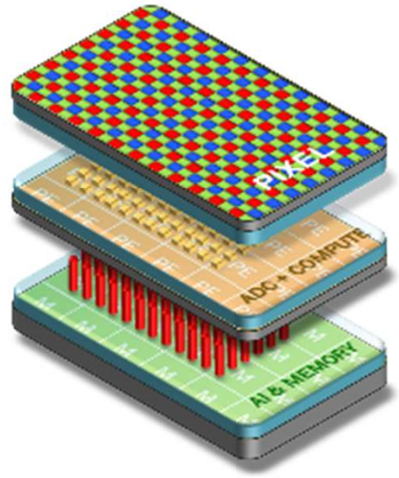
- **3-layer scheme [37]**

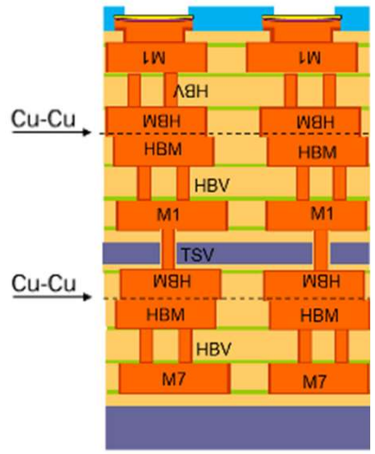
  Pixel array / Readout IC / AI & memory layer

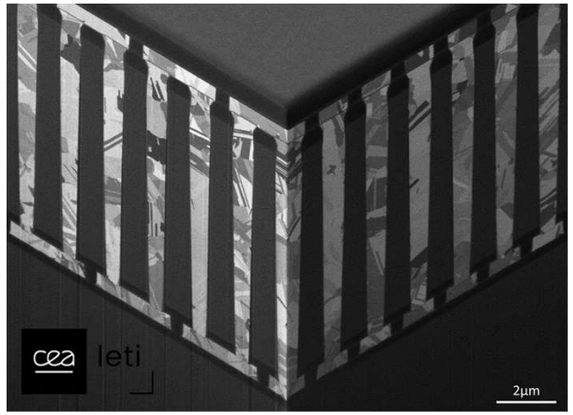
  2 hybrid bonding with 1x10µm HD-TSV



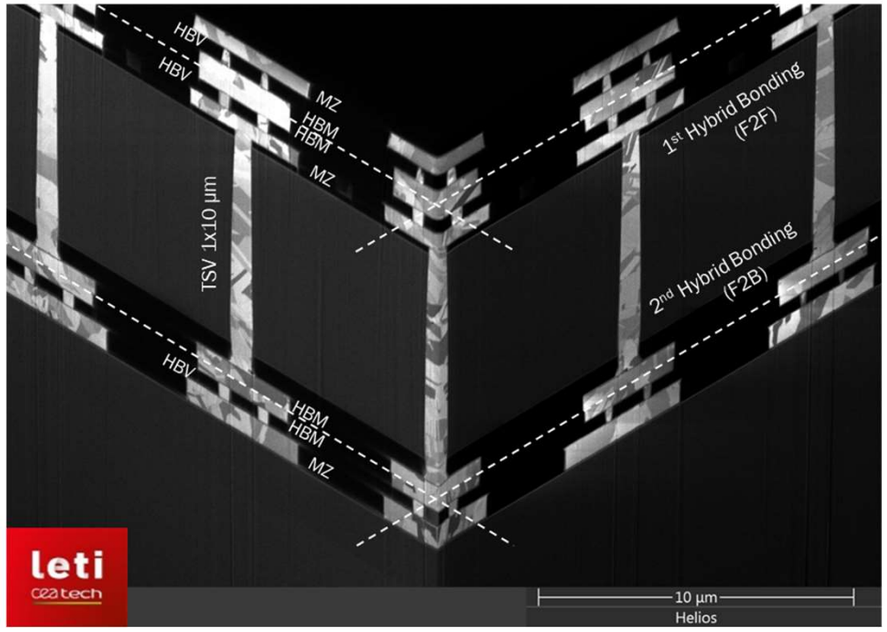
Autonomous vehicle functions



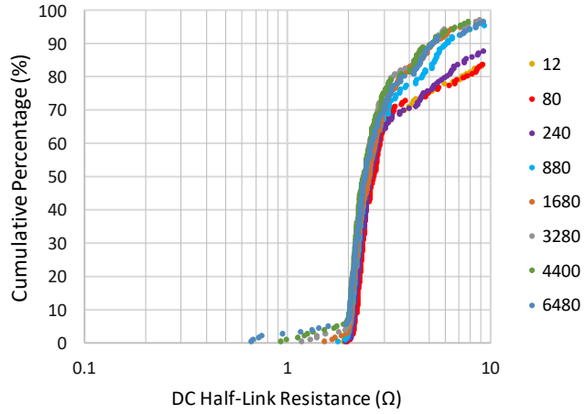




1x10µm TSV (2µm pitch), R_{TSV} = 500mΩ
Misalignment HB2: max. 1 µm (avg 200 nm)
Misalignment HB1: max. 350 nm (avg 100 nm)



Complete structure with 2 hybrid bonding and 1x10µm HD TSV [38]



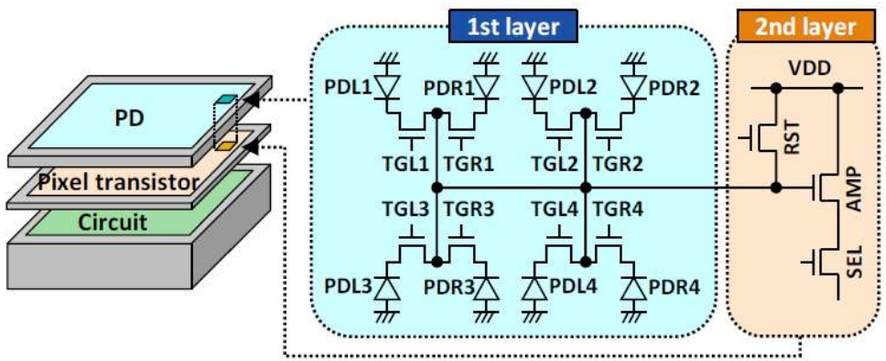
Electrical characterization of hybrid bonding/HD TSV transitions

[37] J. J. Suarez Berru et al., ECTC 2023

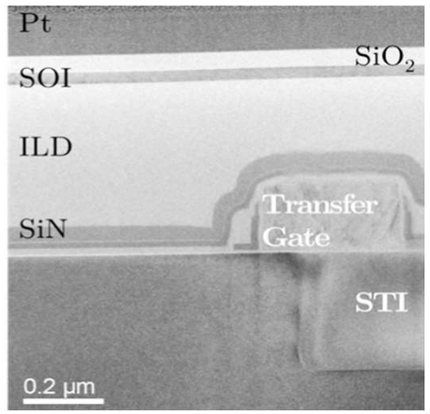
[38] S. Nicolas et al., ECTC 2024

2-layer stacked 4T pixels CMOS Image Sensors

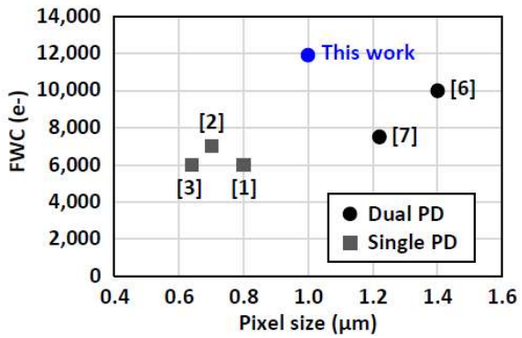
- **Pixel split for full well increase [39]**
  BSI pinned photodiode + transfer gate on layer 1
  RST, source follower & read transistors on layer 2
- **Sequential integration mandatory**
  Misalignment between layer << 1 µm
  Mono. Si transfer + low temp. CMOS process

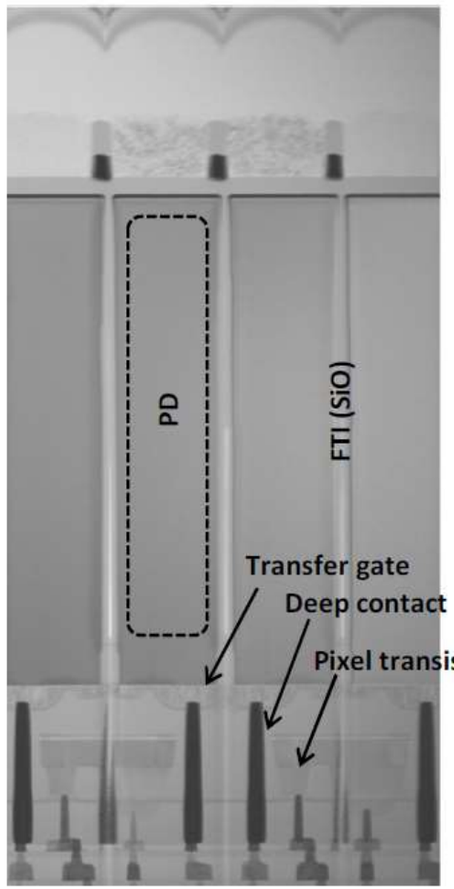


2-layer pixel schematics based on 3D sequential integration



Monocristalline Si layer transfer [1]

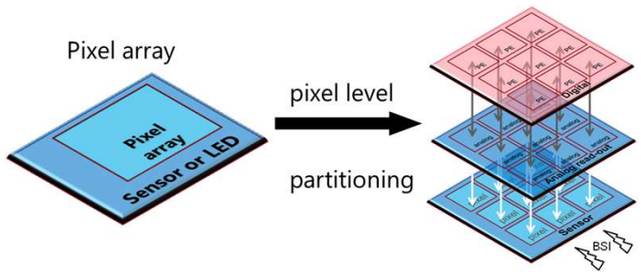




Deep photodiodes, oxide-based full trench isolation (FTI), 1µm dual photodiodes [40]

[39] P. Coudrain, IISW 2009
[40] K. Zaitsu et al., VLSI symp. on technology & circuits, 2022

Sequential 3D combined with hybrid bonding

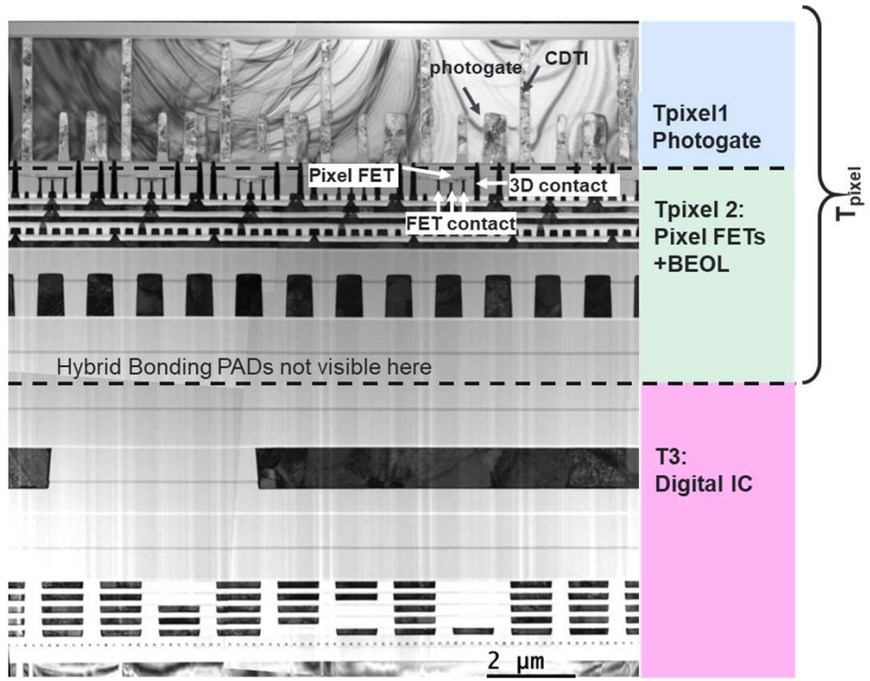


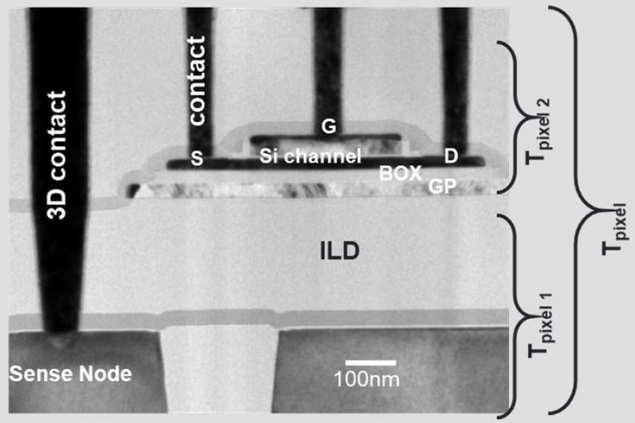
Increased diode area

44% for 1.4µm pitch

Smart pixel

Adaptation, calibration
Pre-processing





- Sequential CMOS process
- Low temperature top level
- Nm-scale alignment between gate levels
- Applicable to heterogeneous and CMOS 3D

Opportunity for pixel partitioning with pitch in the µm range and distributive computing for high efficiency [41]

[41] F. Guayder et al., IEDM 2022

3D integration for SPAD sensors

- **Separating detection & readout [42]**

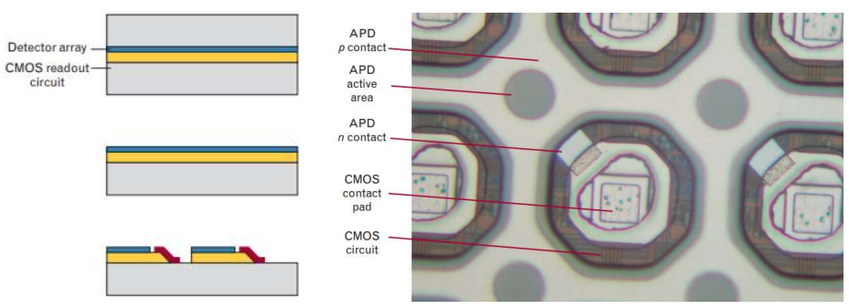
  Layer optimization: CIS (90nm) & CMOS (22nm)

  Better sensitivity, high FF, low DCR, functionality

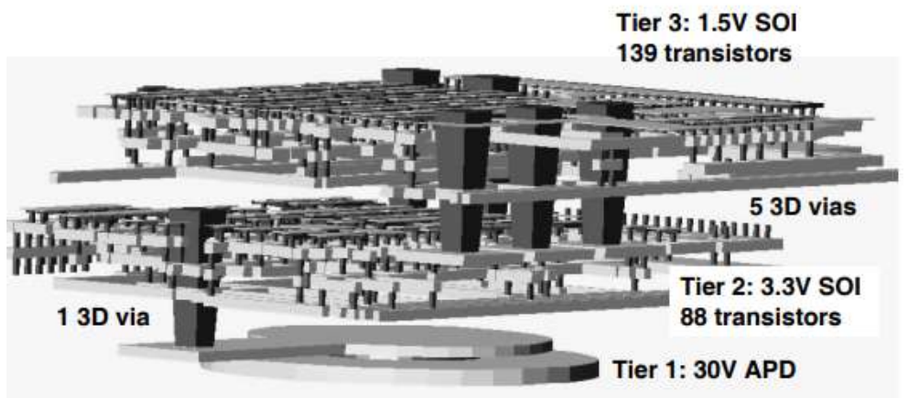
- **3D technology largely evolved**

  Bridges [43], oxide bonding with metal vias [44]

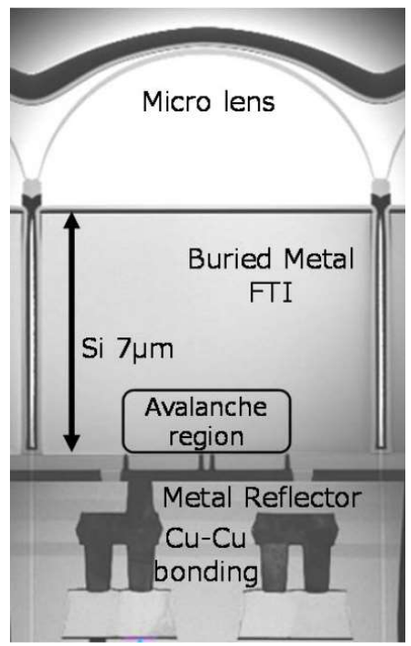
  Bumping, hybrid bonding [45]



32 × 32 array “bridge-bonded” APD/CMOS [40]



3D Geiger-Mode APD with Two SOI Timing Circuit Layers [3]



BSI 10 µm SPAD pixel with FTI & Cu-Cu bonding [43]

[42] E. Charbon, C. Bruschini & M.-J. Lee, ICECS 2018

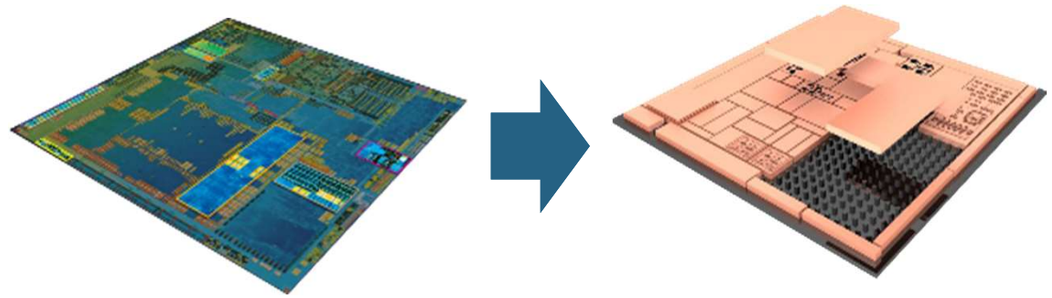
[43] B. Aull et al., Lincol Lab J.; Vol 13, no. 2, pp. 335-350, 2002

[44] B. Aull et al., ISSCC 2006

[45] K. Ito et al., IEDM 2020

Chiplet approach: Heterogenous IC design

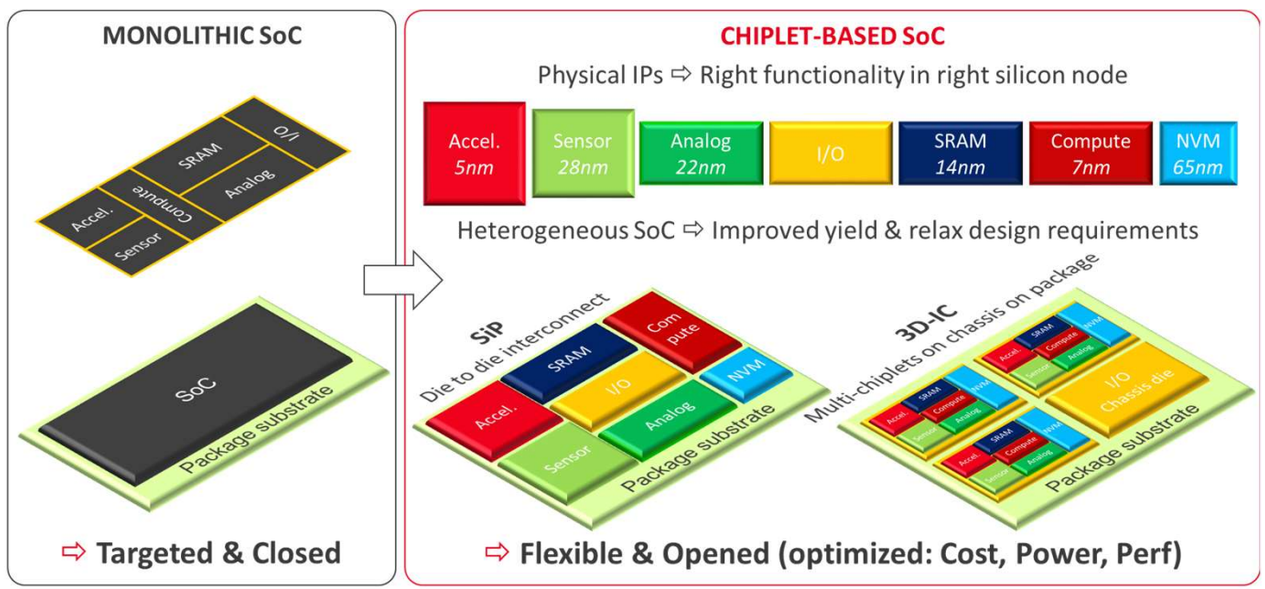
- **Interposer & chiplets**
  Interconnects performance → R.C delay
  Exceeding latency & bandwidth limits
  Cost/form factor advantages



The end of "all for the SoC" paradigm (image from DARPA)

- **Appropriate partitioning**

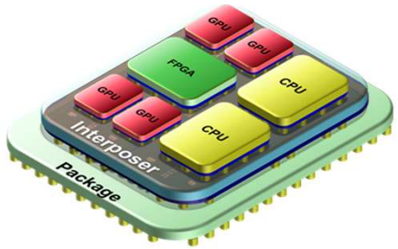
- **Heterogeneous IC design**
  Optimized technology for each function
  specialization by app.: CPU, GPU, AI (...)
  Standardization (coming soon, hopefully)



Trendy application fields for interposers

• Active interposers

Interconnect performance, power management, network on chip…



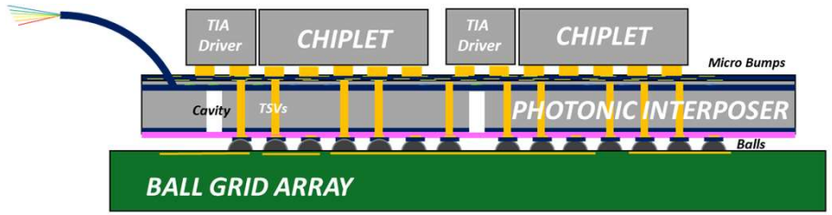
Chiplet on interposer topology

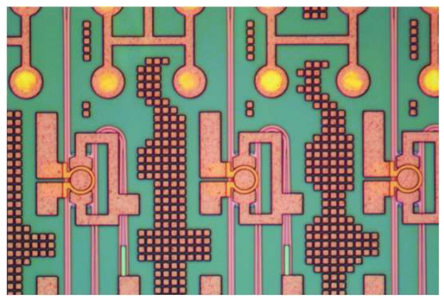
INTACT active interposer [46]

- **Chiplets 28nm FDSOI** 6x22mm²
- **Interposer 65nm** 200mm²

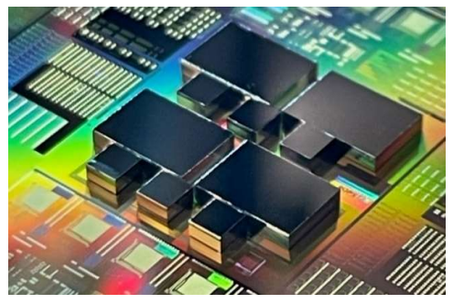
• Photonic interposers [47]

Reduced on-chip latencies & energy consumption, increased bandwidth





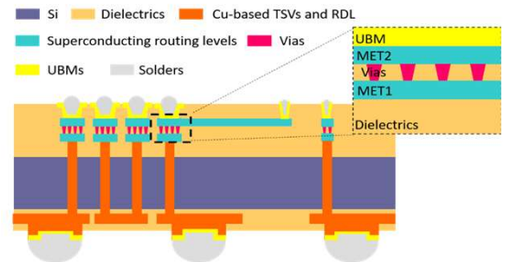
TSV mid (12x100µm) co-integraton with µ-ring resonators after Metal 1

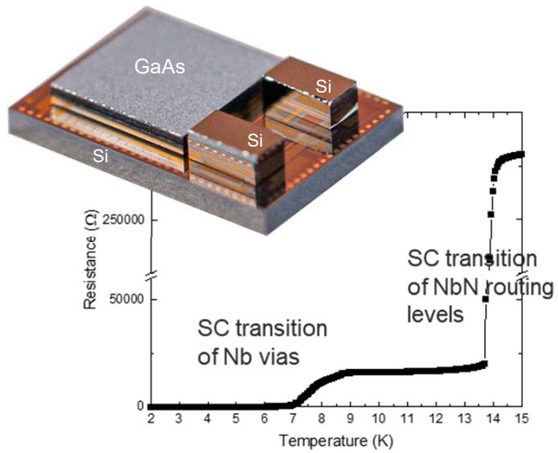


Silicon Photonic Interposer with 4 chiplets and 6 electro-optical drivers in 28nm FD-SOI

• Quantum interposers [48]

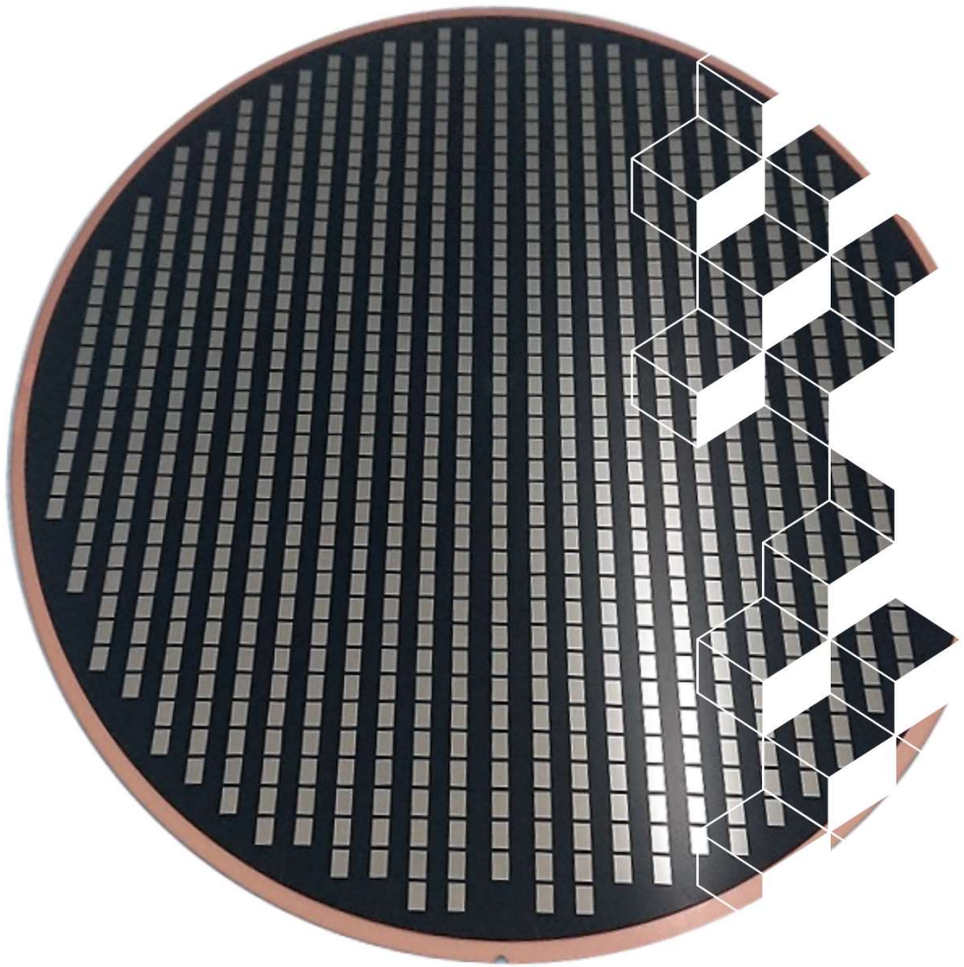
Superconducting routing





Superconducting interconnect assessment

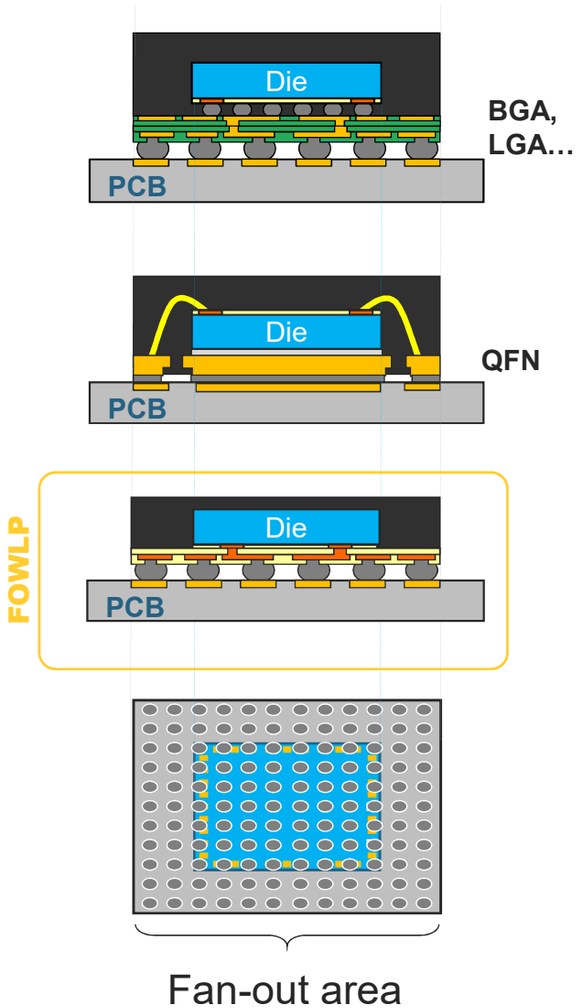
[46] P. Coudrain et al., ECTC 2019
[47] D. Saint-Patrice, ECTC 2023
[48] C. Thomas et al., Materials for Quantum Technology, 2, 3, 035001, (2022)



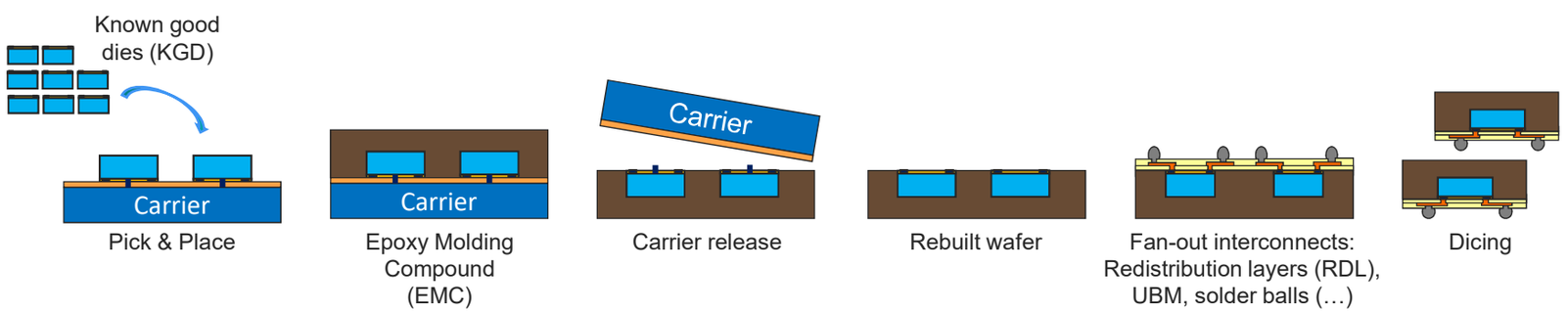
3.

A few words about fan-out wafer level packaging (FOWLP)

The idea behind fan-Out wafer-level packaging



- **Blossoming of interconnections beyond the chip physical footprint**
- **Collective process, without intermediate substrate such as BGA or QFN**
- **Based on a wafer reconstruction approach (ex. eWLB[49])**

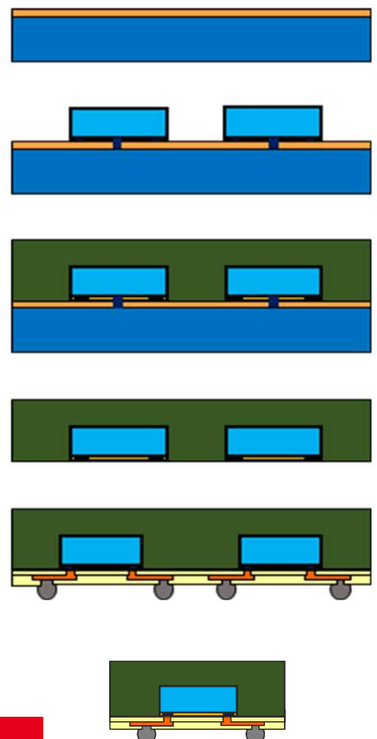


[49] M. Brunnbauer et al., "Embedded Wafer Level Ball Grid Array (EWLB)" , International Electronics Manufacturing Technology Conference, 2008

FOWLP process in a nutshell

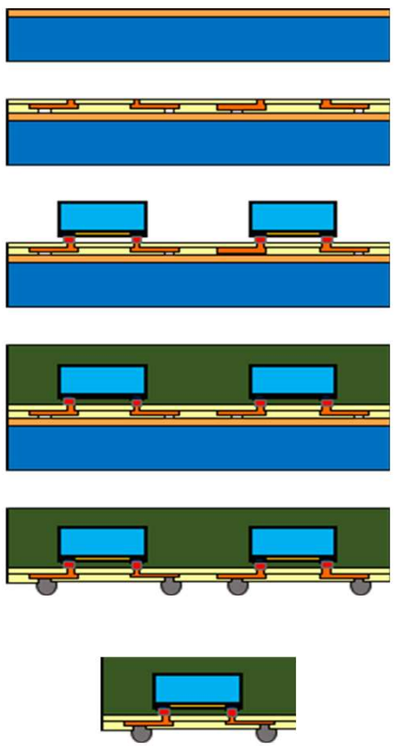
- **A multitude of integration schemes, based on wafer reconstruction**

« Chip 1st »

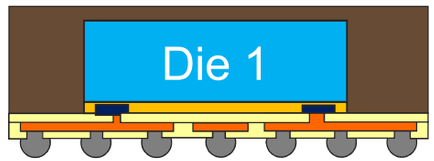


or

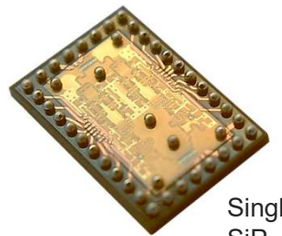
« Interconnects 1st »



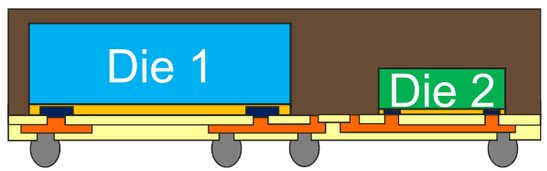
Architecture complexity



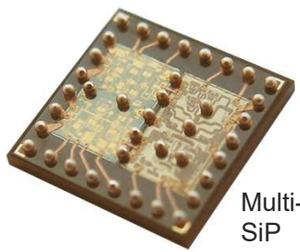
System-in-package (SiP)



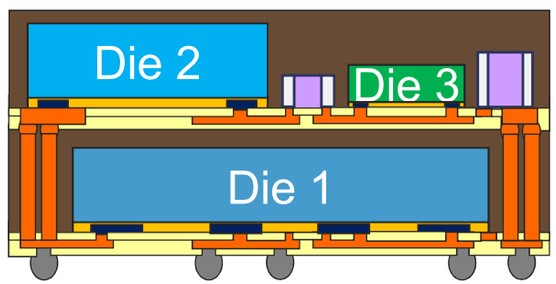
Single die SiP



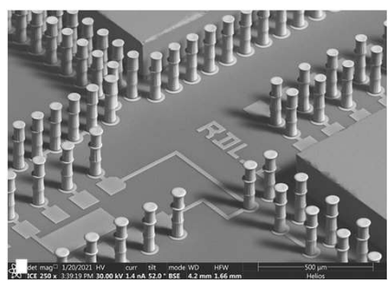
Multi-chip SiP



Multi-chip SiP



3D SiP

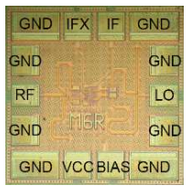


Through Mold Interconnnects

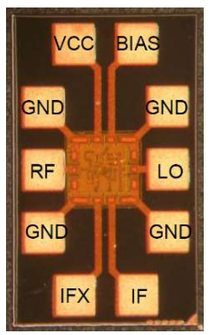
FOWLP high frequency applications examples

• 77 GHz automotive radars [50]

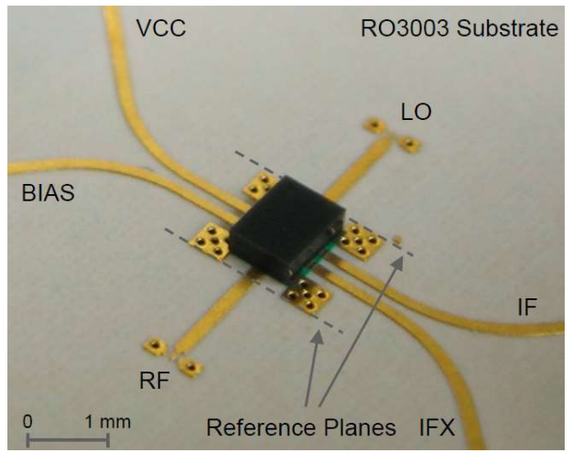
Chip surface no longer defined by that of I/O pads, as connections are extended outside the chip



SiGe mixer die
(550 x 550 x 100 µm³)



eWLB SiP
(2.5 x 1.5 mm²)

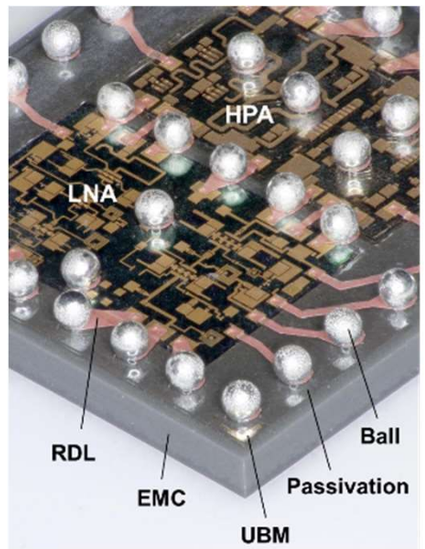


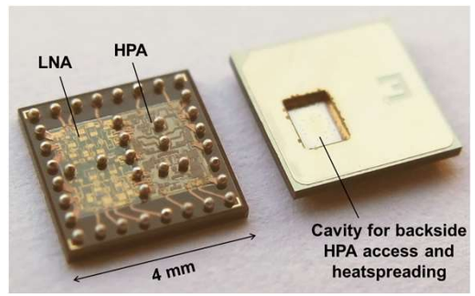
Package	G (dB)	NF_{SSB} (dB)
On Wafer	21.4	11.7
Package P11	18.7	16.8

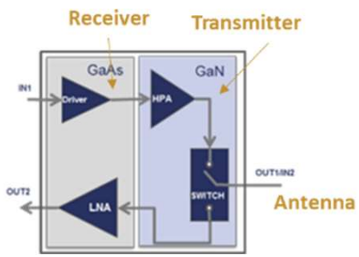
SiP on characterization board

• 5G Front-End modules [51]

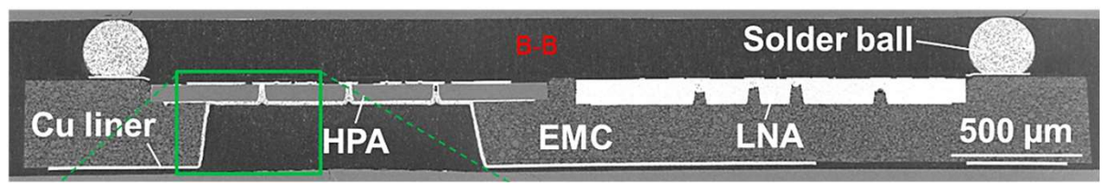
GaAs LNA & GaN HPA co-integration within package. Thermal dissipation from backside cavity



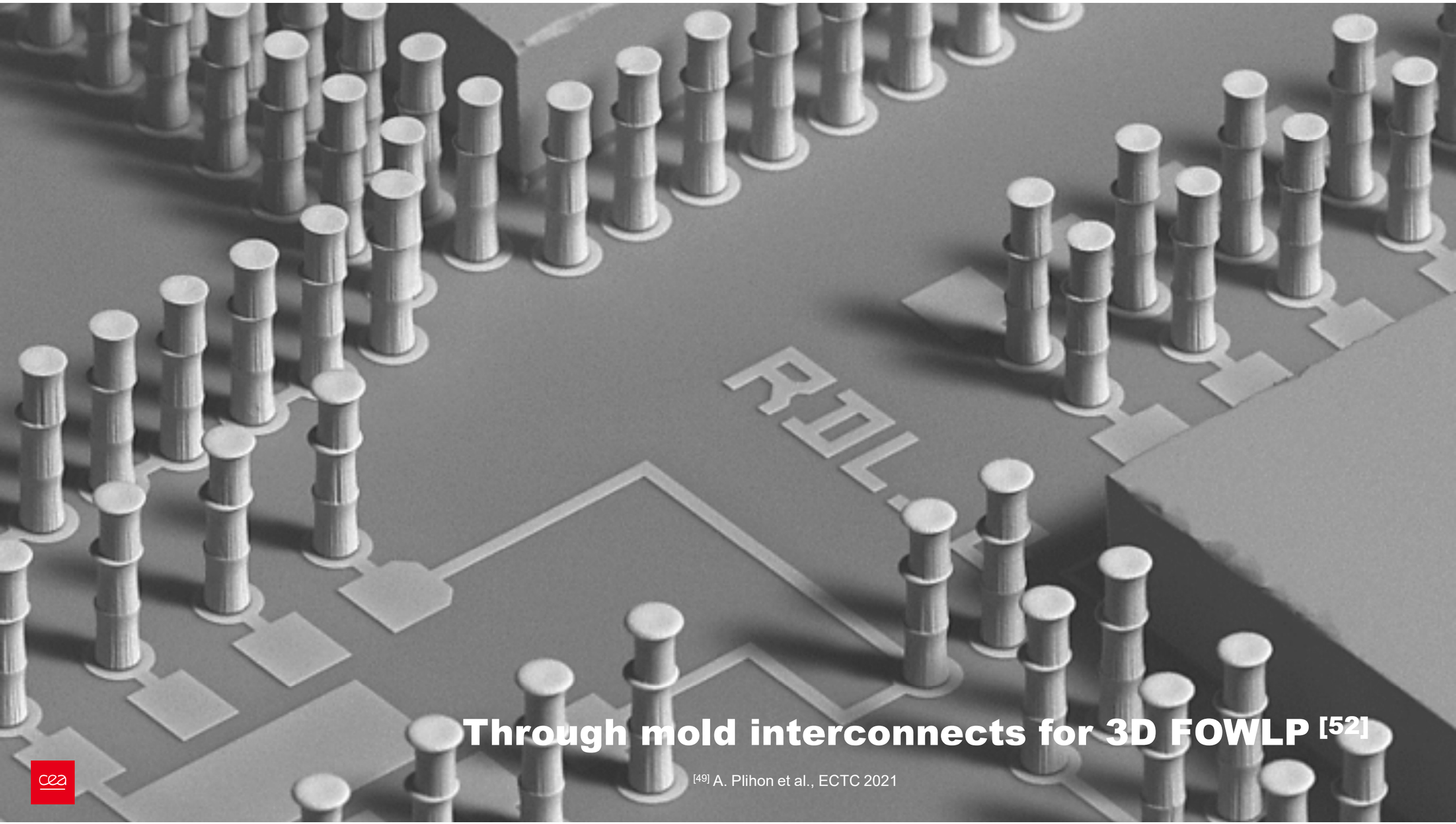




Award 2021



[50] M. Wojnowski et al., ECTC 2008
[51] A. Garnier et al., ECTC 2021



Through mold interconnects for 3D FOWLP [52]

[49] A. Plihon et al., ECTC 2021

Take-home messages

- **Advanced packaging has become a driver of innovation in electronics, System-in-Package becomes the norm**

  3D approaches able to answer design needs

  Image sensors played pioneering role in the advent of adv. packaging

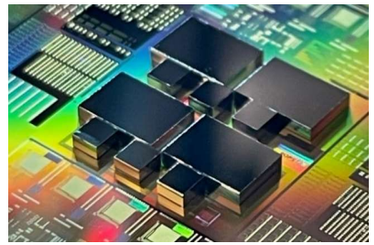
- **It is now conceivable that any heterogeneous architecture can be realized in one way or another, but…**

  Cost-performance trade-off, timely development

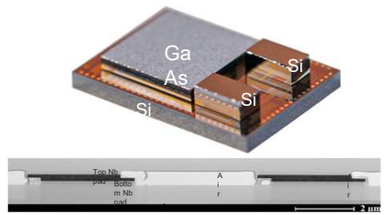
  Standardization & efficiency, ecological impact

  → still very much in the spotlight

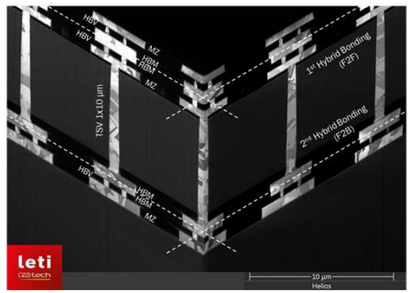
- **Designers are often not fully aware of the toolbox available → come & discuss!**



Chiplets on photonic interposer



Superconducting Nb/Nb bonding for quantum interposers



Double hybrid bonding scheme associated to high density TSV

Thanks for your attention

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