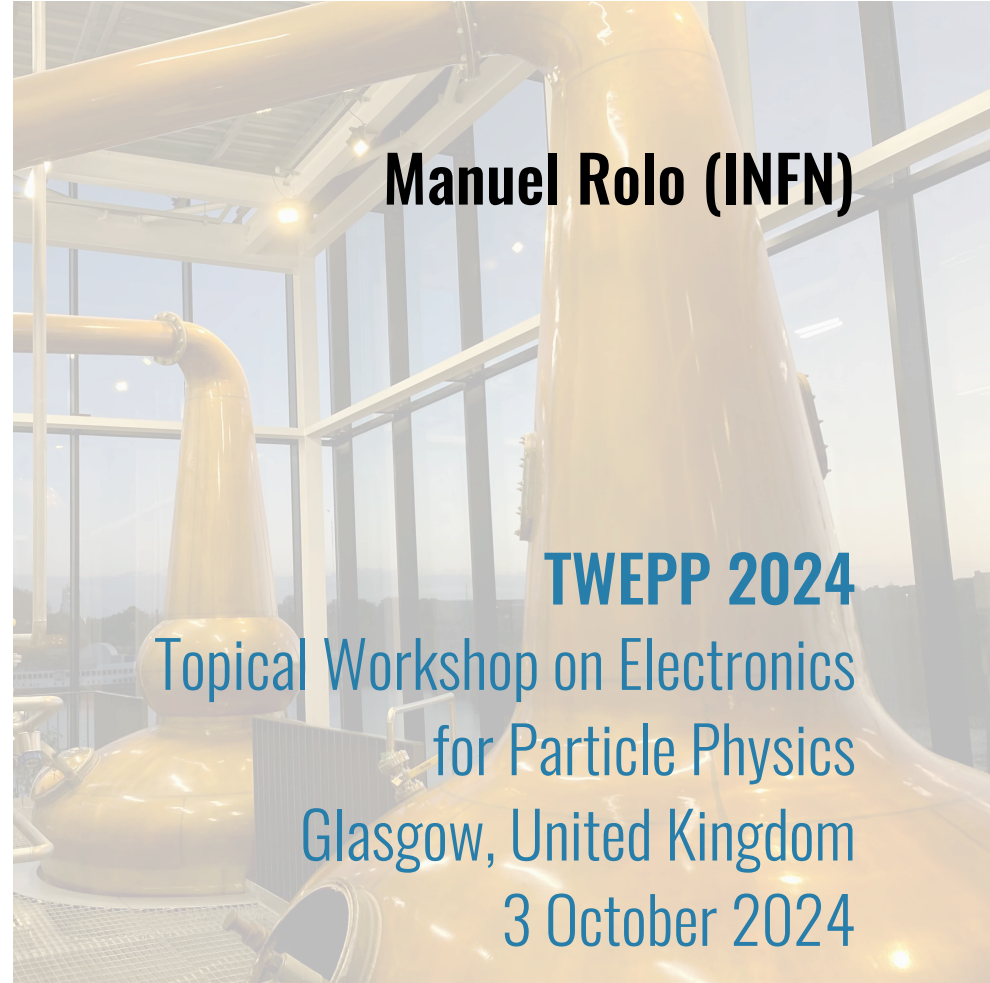


An outlook to the development of cryogenic CMOS electronics for particle physics



Manuel Rolo (INFN)

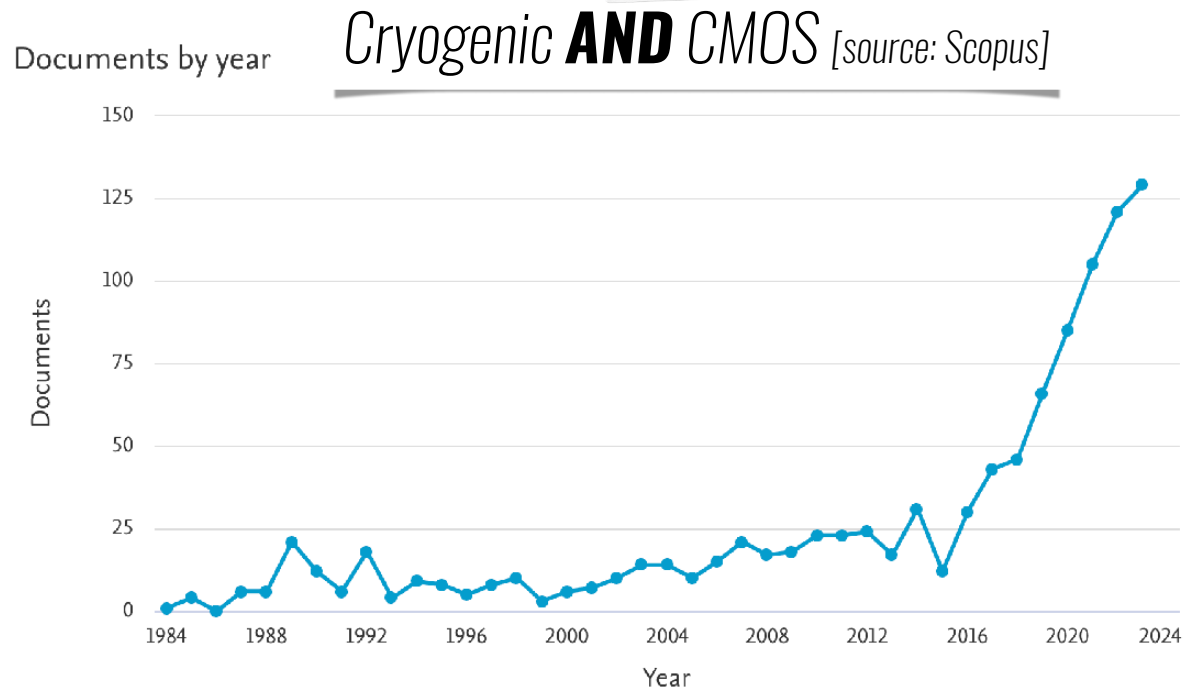
TWEPP 2024

Topical Workshop on Electronics
for Particle Physics

Glasgow, United Kingdom

3 October 2024

Motivation for this talk



R&D on Cryogenic CMOS saw a remarkable increase since 2017!

While CMOS seems to be the most used platform, III-MESFET (switching circuits and power amplifiers) and SiGe (LNAs) are also being used for temperatures down to 4K and below.

1964

Semiconductors at Cryogenic Temperatures

A. K. JONSCHER

Summary—A review is made of those physical properties of semiconductors which are relevant to device operation at cryogenic temperatures. These include carrier density, mobility, hot carrier phenomena, recombination and trapping, and the performance of p - n junctions. A description is then given of the cryogenic operation of semiconductor devices together with an assessment of future possibilities.

A. K. Jonscher, "Semiconductors at cryogenic temperatures," in *Proceedings of the IEEE*, vol. 52, no. 10, pp. 1092-1104, Oct. 1964, doi: 10.1109/PROC.1964.3296.

V. CONCLUSIONS

The foregoing discussion leads to two general conclusions. Firstly, semiconductor devices seem to have found, as yet, no major cryogenic application, although a few very useful specialized devices have been invented. This state of affairs is not so much the fault of the devices or of semiconductor materials as such, but rather is due to the absence so far of any real technological justification for going on a large scale to these extreme temperatures.

Secondly, the properties of semiconductor materials at cryogenic temperatures are so strikingly different from the familiar properties at higher temperatures, that it is reasonable to expect many more device applications to emerge as a result of continued research and development effort in this direction. In this sense, therefore, the present state of the science and art of cryogenic semiconductor devices cannot be regarded as more than a very modest start of a potentially important development. The significant feature of this situation is that most of the relevant fundamental physical background information is already available and ready for exploitation when the real need arises.

The fact that semiconductor devices operating at cryogenic temperature do not find a major application is not related to fundamental flaw of the process or materials, but rather because there seems to be “no real technological justification for going on a large scale to these extreme temperatures”.

In the meanwhile, Feynman.

1959

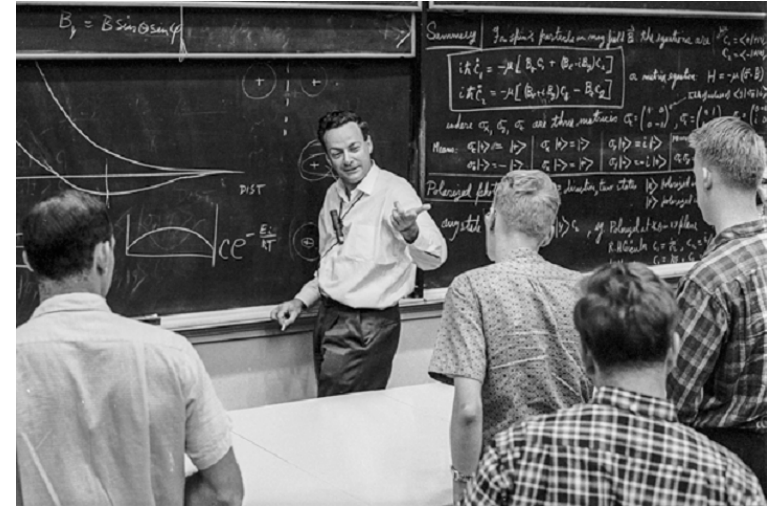
"There's Plenty of Room at the Bottom: An Invitation to Enter a New Field of Physics"

"Why can't we manufacture these small computers somewhat like we manufacture the big ones?"

"Why can't we drill holes, cut things, solder things, stamp things out, mould different shapes all at an infinitesimal level?"

"What are the possibilities of small but movable machines?"

They may or may not be useful, but they surely would be fun to make.



the reason that you would do it might be just for fun. But have some fun!



In the meanwhile, in early 1959 Jack Kilby and Robert Noyce had deposited the first two patents for integrated circuits...

1970

The Role of Low Temperatures in the Operation of Logic Circuitry

ROBERT W. KEYES, SENIOR MEMBER, IEEE, ERIK P. HARRIS, AND
KARL L. KONNERTH, MEMBER, IEEE

The authors are with the IBM Thomas J. Watson Research Center

Abstract—It has often been suggested that operating logical circuitry at low temperatures would have many advantages. The purpose of this paper is to evaluate such suggestions quantitatively. Changes in physical properties of materials upon cooling to low temperatures have been analyzed to determine their impact on the parameters which control the performance of logical circuitry. The following topics have been considered: electrical conductivity, thermal conductivity, thermal energy, heat transfer, superconductivity, liquid helium, low-gap high-mobility semiconductors, and thermal activation of atomic motion.

R. W. Keyes, E. P. Harris and K. L. Konnerth, "The role of low temperatures in the operation of logic circuitry," in Proceedings of the IEEE, vol. 58, no. 12, pp. 1914-1932, Dec. 1970, doi: 10.1109/PROC.1970.8063

The trend toward faster and physically smaller computer circuitry is creating serious problems of packaging. It has been suggested that operation at low temperature may ease some of these problems and may also improve reliability.

The purpose of this paper is to investigate how much improvement can be achieved through lower temperature operation of computer circuitry.

Conclusions concerning the implications of these considerations for logic design are then drawn.

Setting the ground for Quantum Processors

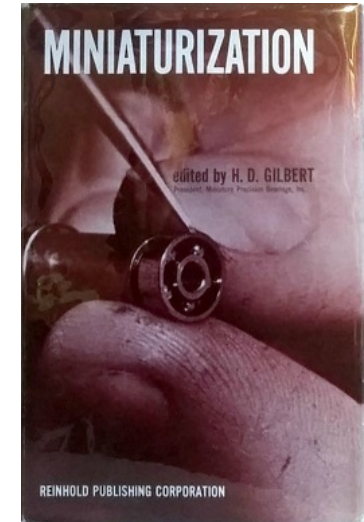
"There's Plenty of Room at the Bottom" could be regarded as one of the founding texts of the concepts of nanotechnology.

In 1959, he is actually interested on the possible use of the **principles of quantum mechanics to create denser information processors.**

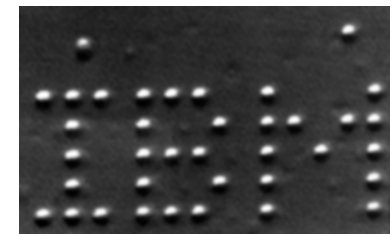
"What would happen if we could arrange the atoms one by one the way we want them?"

"The principles of physics, as far as I can see, do not speak against the possibility of manoeuvring things atom by atom."

*"We can use, **not just circuits, but some system involving the quantised energy levels, or the interactions of quantised spins, etc.**"*

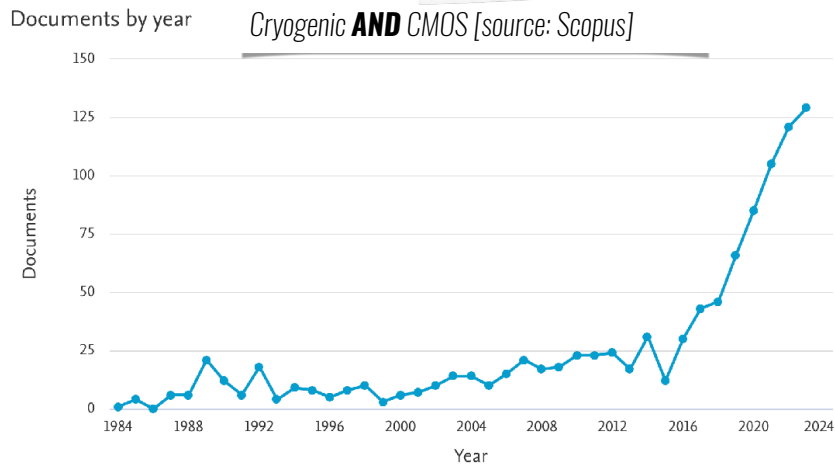


"There's Plenty of Room at the Bottom: An Invitation to Enter a New Field of Physics"



1990: [Donald Eigler](#) and Erhard Schweizer, 35 atoms of Xenon on a nickel surface, pattern is 5nm tall and 17nm wide

(Revised) motivation for this talk



“But the **physical world is quantum mechanical**, and therefore the proper problem is the simulation of quantum physics”

“Now it turns out, as far as I can tell, that you can simulate this with a **quantum system, with quantum computer elements.**”

Simulating physics with computers

Richard P. Feynman (Caltech)

May, 1981

22 pages

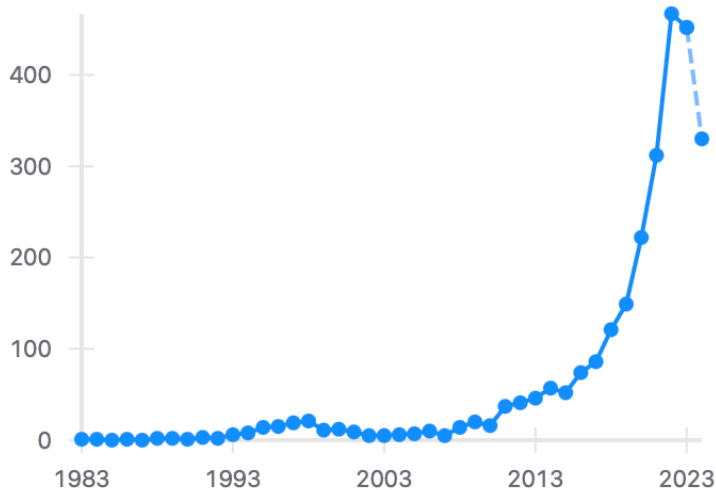
Part of [Selected papers of Richard Feynman: With commentary](#), 923-944

Published in: *Int.J.Theor.Phys.* 21 (1982) 467-488

DOI: [10.1007/BF02650179](https://doi.org/10.1007/BF02650179)

View in: [AMS MathSciNet](#), [ADS Abstract Service](#)

Citations per year

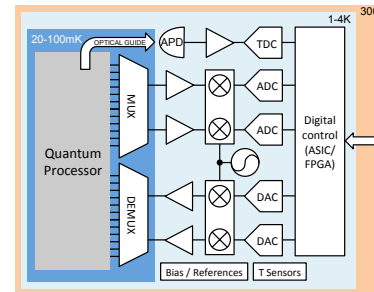
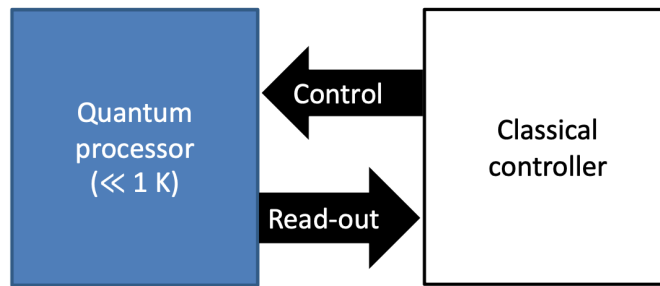
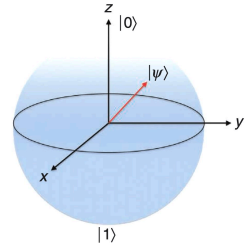


be understood very well in analyzing the situation. And I'm not happy with all the analyses that go with just the classical theory, because nature isn't classical, dammit, and if you want to make a simulation of nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem, because it doesn't look so easy. Thank you.

<https://s2.smu.edu/~mitch/class/5395/papers/feynman-quantum-1981.pdf>

Quantum Computer Electronics in a nutshell

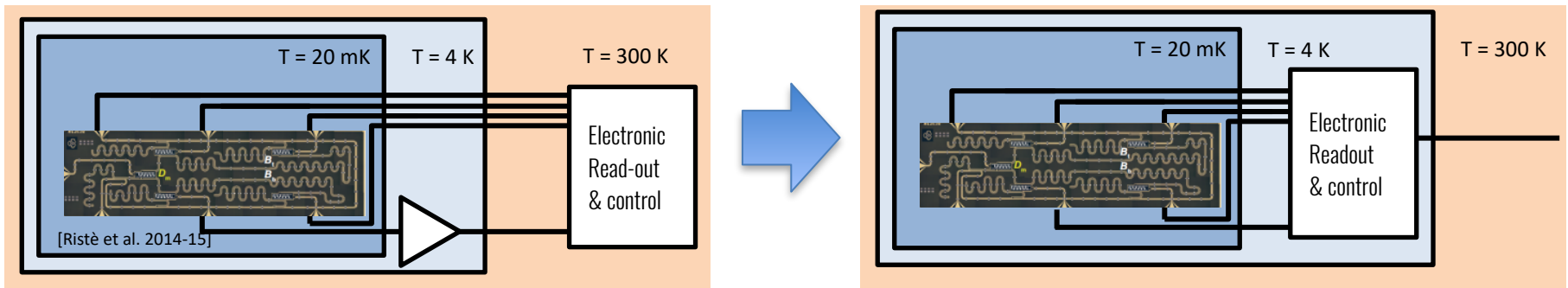
- * The fundamental computational unit of a QC is the array of quantum bits (qubits): the quantum processor
- * Qubits can have a coherent state from $|0\rangle$ to $|1\rangle$ on the continuous Bloch sphere
 - ◆ Superposition is maximum when the vector representing the state of the qubit is on the equator of the sphere
 - ◆ Knowing the state of one qubit implies knowledge of the state of the entangled one
- * Coherence of qubits is required at all times, hence they are monitored and corrected periodically
- * The bidirectional interface between a quantum processor and its classical controller is (opto)electrical



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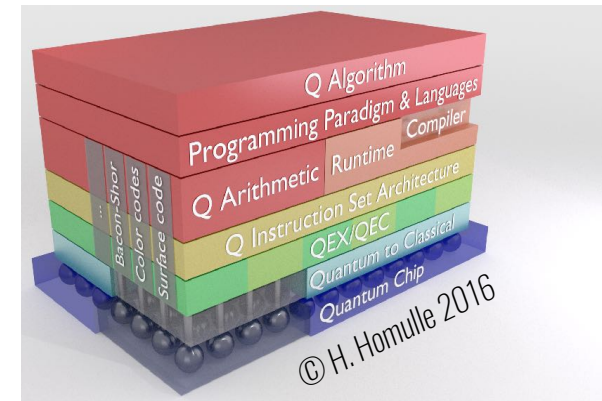
- Qubits generally operate in the mK range, while in the typical (outdated?) embodiment these are interfaced with the controller operating at room temperature
- Solving the wiring bottleneck that arises is the key for scalability, hence the need to design cryogenic electronics capable to operate with stringent requirements in terms of operation temperature, noise and frequency.

Interfacing Qubits with the Classical World



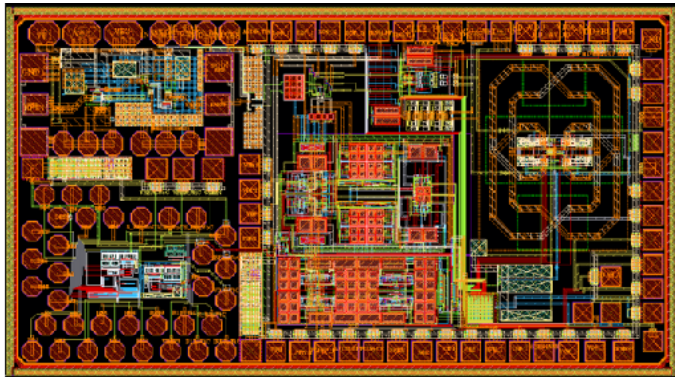
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- **Current envisaged solutions**
 - Electronics at 4 K
 - Only connections to 4 K to 20 mK are needed
- **Ultimate solution**
 - Qubits at 4 K
 - Monolithic integration

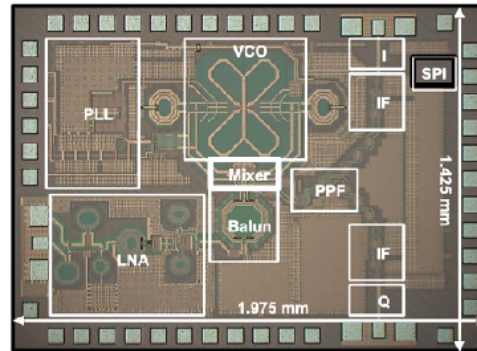


- ▶ *Cryo-CMOS technology is key to **scalability** and **practicality** of quantum computers*
- ▶ *CMOS-compatible qubits could emerge soon*
- ▶ *Other technologies like 3D integration and high-T qubits could be important enablers*

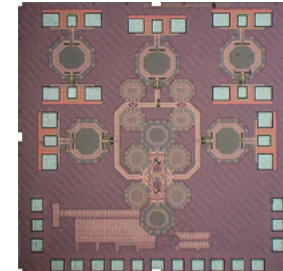
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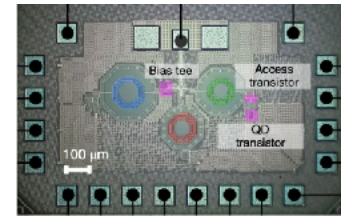
Y. Zou, J. Benserhir, V. Pestic, Y. Peng, December 2023



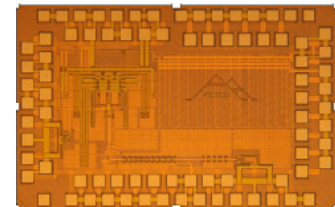
A. Ruffino et al., ISSCC 2021 – Y. Peng et al., JSSC 2022



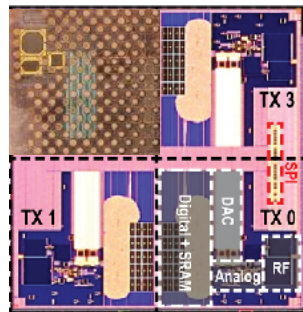
A. Ruffino et al., RFID 2019 & ISSC 2020



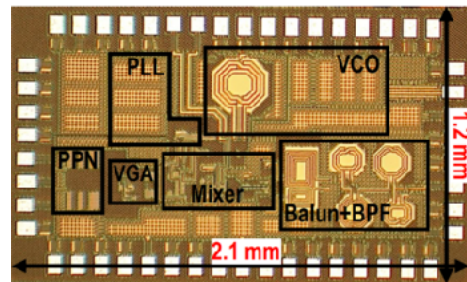
A. Ruffino et al., Nature EI, 2020



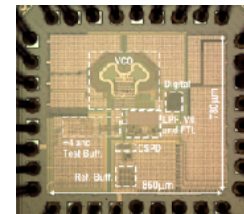
G. Kiene, et al., ISSCC 2021 & JSSC 2023



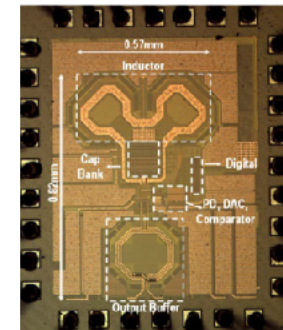
B. Patra, J.v.Dijk et al., ISSCC 2020 & JSSC 2020
X. Xue et al., Nature 2021; Pellerano et al., CICC 2022



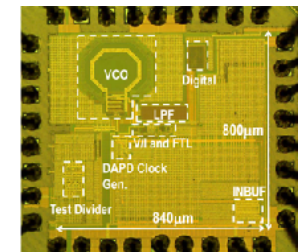
Y. Zou, J. Benserhir, V. Pestic, Y. Peng, September 2022



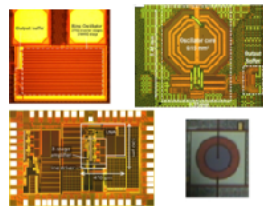
J. Gong, et al., RFIC 2020 & JSSC 2022



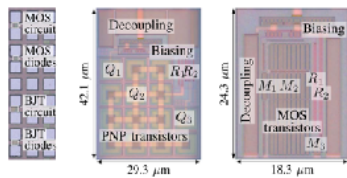
J. Gong, et al., ISSCC 2020 & TCAS 2022



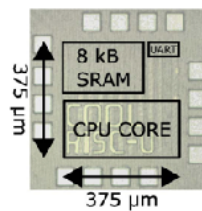
J. Gong, et al., ISSCC 2021 & JSSC 2023



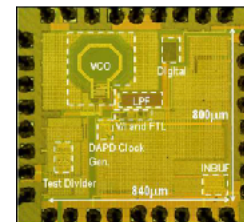
E. Charbon et al., ISSCC 2017; B. Patra et al., JSSC 2017



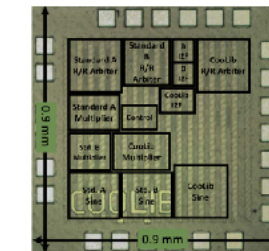
H. Homulle, et al., SS-CL 2018



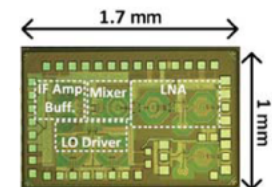
E. Shriek, et al., SS-CL 2020



J. Gong, et al., CICC 2021

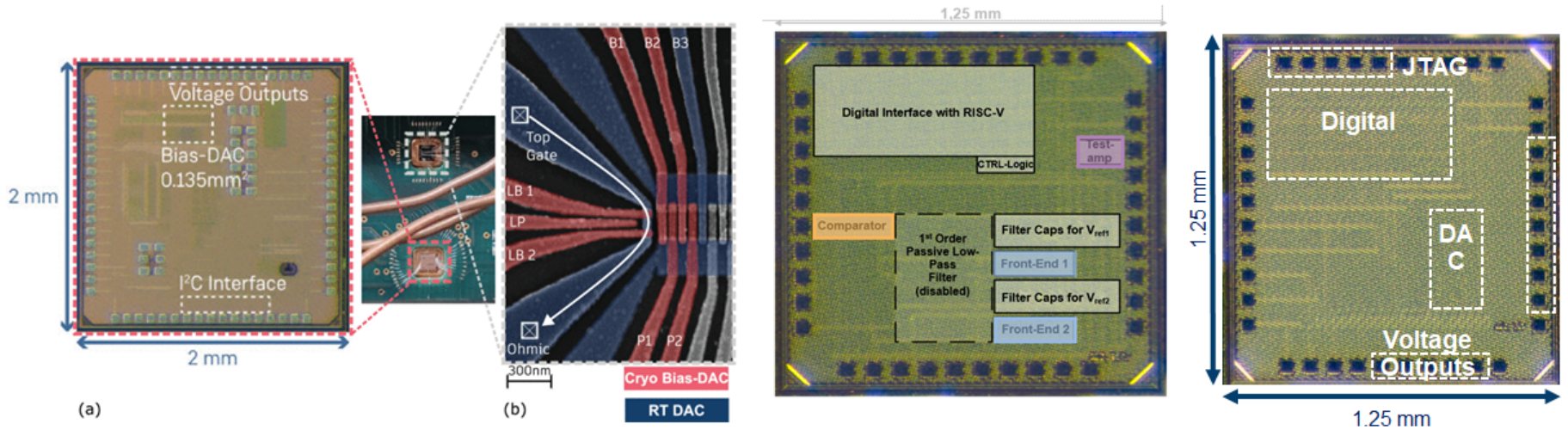


E. Shriek, et al., SS-CL 2020



B. Prabowo, et al., ISSCC 2021

65nm and GF22nm quantum designs at FZJ



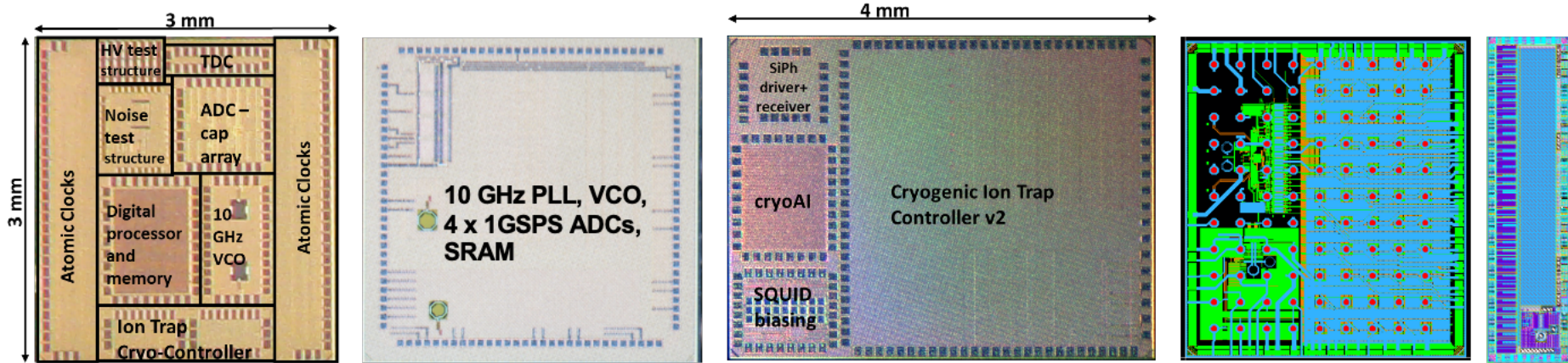
- SQUBIC 65nm Bias DAC @ 44mK with qubit
- QUOCCA 22nm FDSOI readout @4K
- QUOCCA SET 22nm FDSOI bias @4K

[1] L. Schreckenberger et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023-IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023, pp. 161-164, doi: 10.1109/ESSCIRC59616.2023.10268801.

[2] Bühler et al., QUOCCA SET: A Scalable Readout IC for Semiconductor Quantum Dots Using Single Electron Transistors and Correlated Double Sampling

[3] Schreckenberger et al., A Cryogenic 22nm FD-SOI CMOS 12 Channel DAC for Spin Qubit Bias

GF22nm FDSOI quantum chips at Fermilab



GF_test chip: (11/21) Various designs

Michigan: (07/22) 10 GHz PLL, VCO, 4 x 1GSPS ADCs, SRAM

Cryogenic Ion trap controller: (01/23) 16 channel Ion trap control chip

Si Photonic driver/receiver

cryoAI: ultrafast NN for anomaly detection

SQUIDDAC: SLUG_biasing; various level shifter test structures

Glebe: (with Microsoft) 10 GSPS ADC

Sunrock: 32 channel SNSPD readout with ~ps time tagging

Intel's Pando Tree mK CMOS chip

- Intel has introduced a millikelvin quantum research control chip, dubbed Pando Tree.
- closer integration of control electronics to qubits, thereby reducing the wiring complexity and improving overall system efficiency.
- represents a significant step forward in addressing the wiring bottleneck that limits the scaling of QC

Intel's Millikelvin Quantum Research Control Chip, code-named Pando Tree

4 Kelvin

Millikelvin

Horse Ridge II Control Chip

NEW

Pando Tree Millikelvin Control Chip

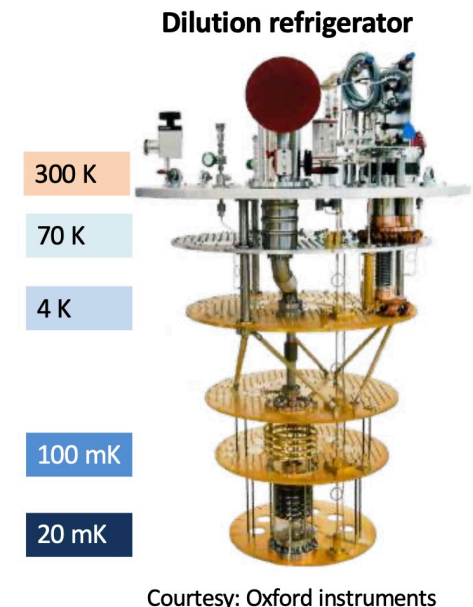
Tunnel Falls Spin Qubit Chip

Tunnel Falls

Pando Tree

- Addresses wiring bottleneck between the 4 Kelvin control chip and the spin qubit chip
- First Intel CMOS circuits operating at millikelvin
- Paves the way to scaling with tighter control/qubit integration

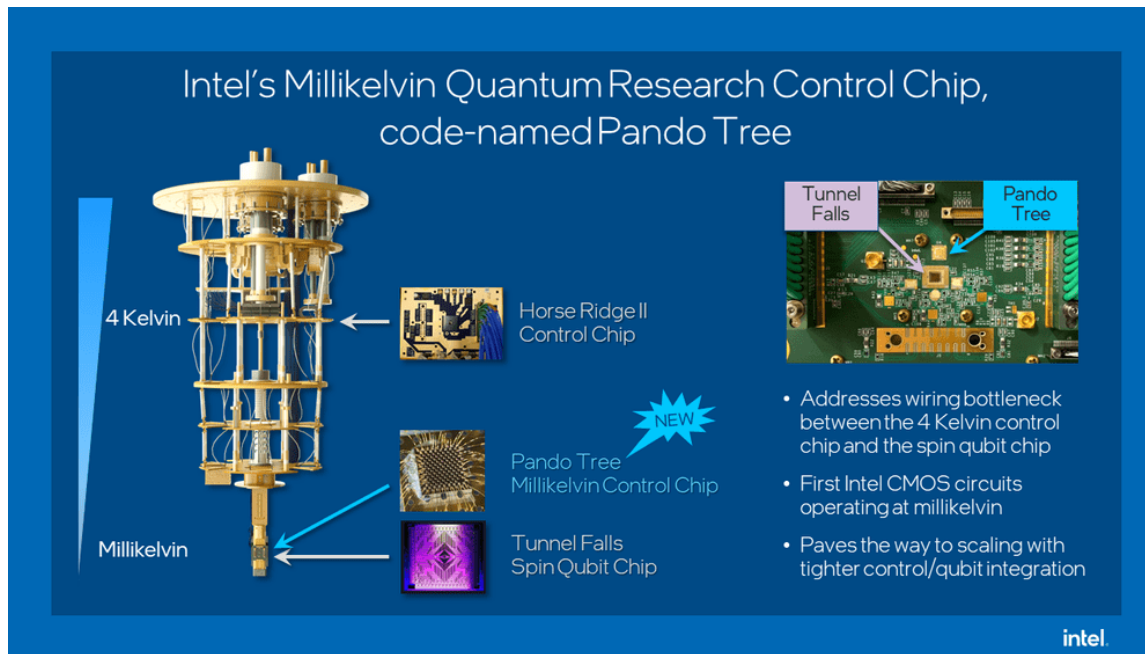
intel.



“Deploying traditional CMOS circuit capability at the millikelvin stage of the dilution refrigerator will enable quantum scaling to millions of qubits in the future.”

Intel's dual-chip system and qubit chip integration

- Horse Ridge II (4K) was introduced in 2020 - generates the necessary control voltages and communicates with Pando Tree through a single signal line and multiple digital control signals
- Pando Tree (mK temperatures), presented in 2024, serving as a demultiplexer, distributes these control signals to the qubits, significantly reducing the number of wires needed.

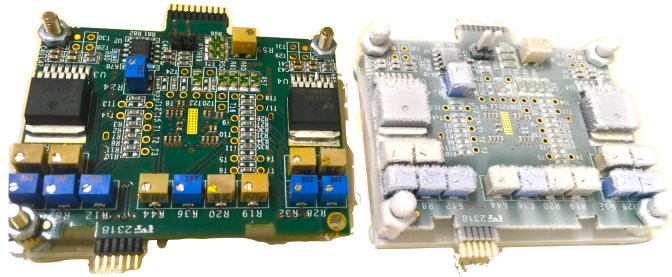


<https://thequantuminsider.com/2024/06/21/intel-debuts-new-chip-focused-on-addressing-quantum-computings-wiring-bottleneck/>

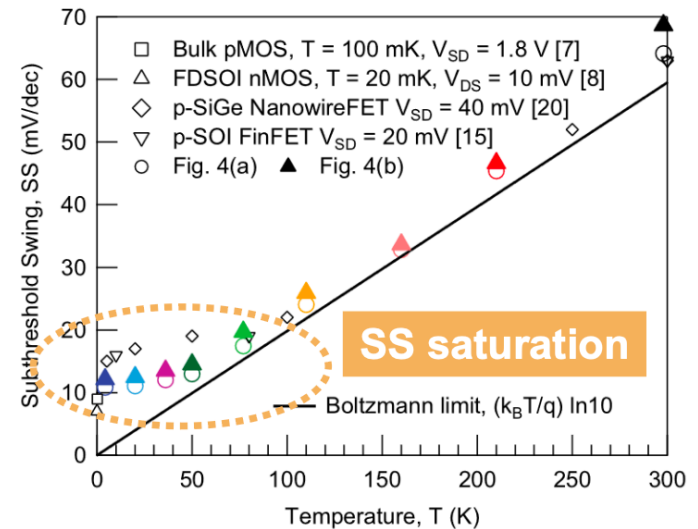
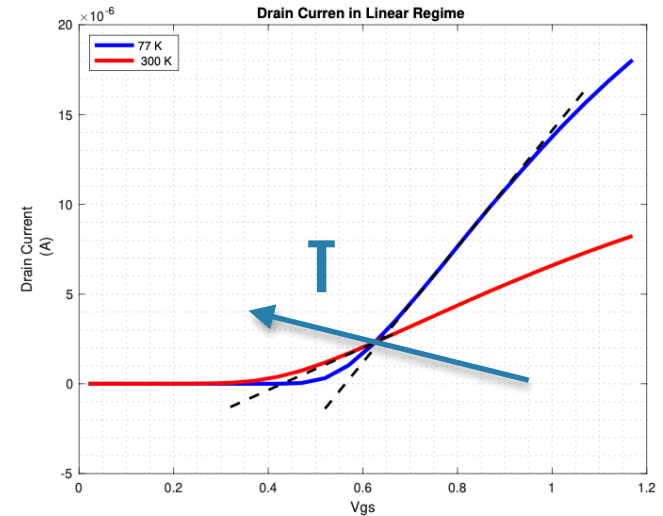
<https://community.intel.com/t5/Blogs/Tech-Innovation/Data-Center/Intel-s-Millikelvin-Quantum-Research-Control-Chip-Provides/post/1608558#:~:text=Pando Tree is a key,qubits operate at room temperature.>

“By operating in the same millikelvin stage as the qubit chip, Pando Tree can be co-packaged with the qubit chip. In the future, this will allow the millions of interconnect wires required between Pando Tree and the qubit chip to be implemented using the latest Intel Foundry Foveros 2.5D and 3D packaging technologies instead of the PCB traces currently being used.”

Operating CMOS at cryogenic temperature



- ▶ **Threshold voltage increases**
 - ◆ Compensated on SOI with backgate voltage (1)
- ▶ **Mismatch increases**
- ▶ **Increase of 1/f noise**
- ▶ **Higher carrier mobility**
- ▶ **Higher Transconductance**
- ▶ **Reduced Thermal Noise**
- ▶ **Steeper Subthreshold Swing (SS)**
 - ◆ Reduced leakage currents
 - ◆ Saturating at ~ 20 mV/dec for $T \lesssim 70$ K (2)



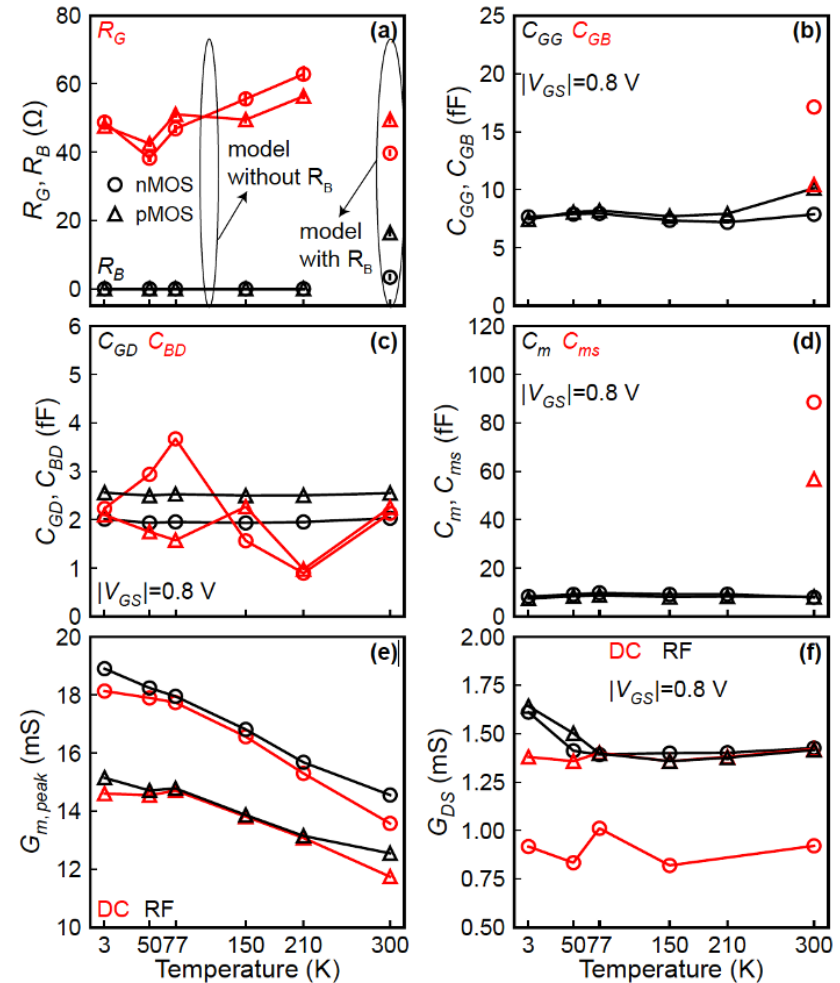
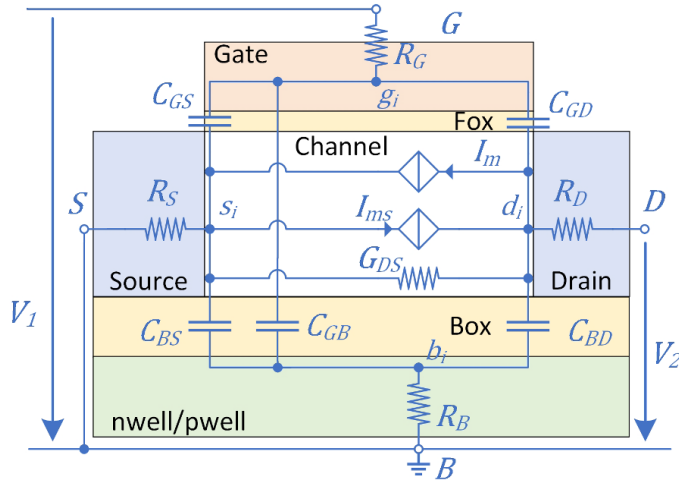
(1) B. Cardoso Paz et al., "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.

(2) A. Beckers, F. Jazaeri and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," in *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 276-279, Feb. 2020, doi: 10.1109/LED.2019.2963379.

Extensive modelling campaigns at EPFL

- CMOS 0.16 μm STMicroelectronics
- CMOS 40nm TSMC
- CMOS 28nm STMicroelectronics bulk/FDSOI
- CMOS 22nm FDSOI Global Foundries
- CMOS 16nm FinFET TSMC

RF Modelling of CMOS 22nm FDSOI



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Cryo-PDKs for GlobalFoundries nodes at Fermilab



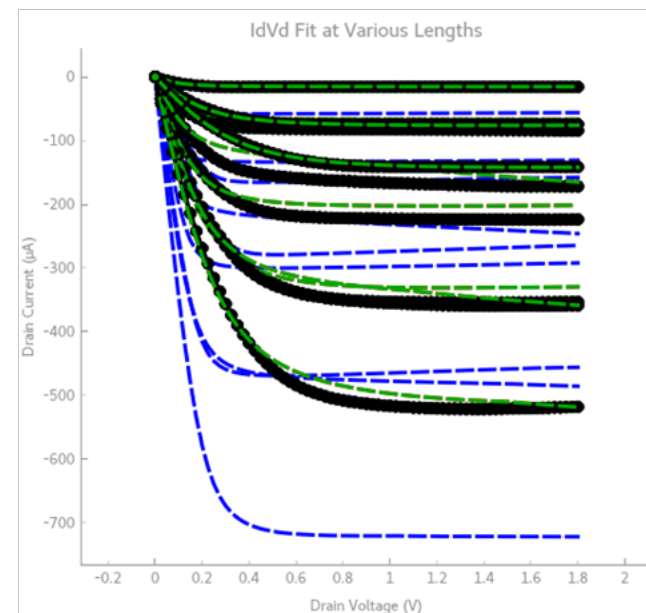
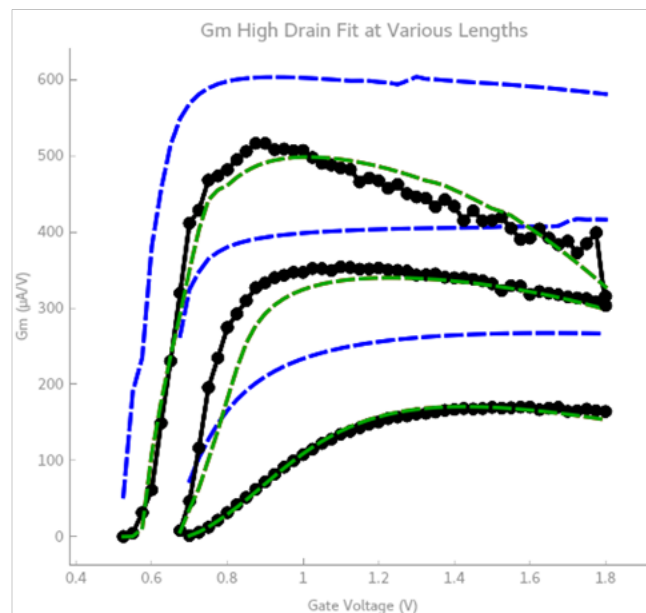
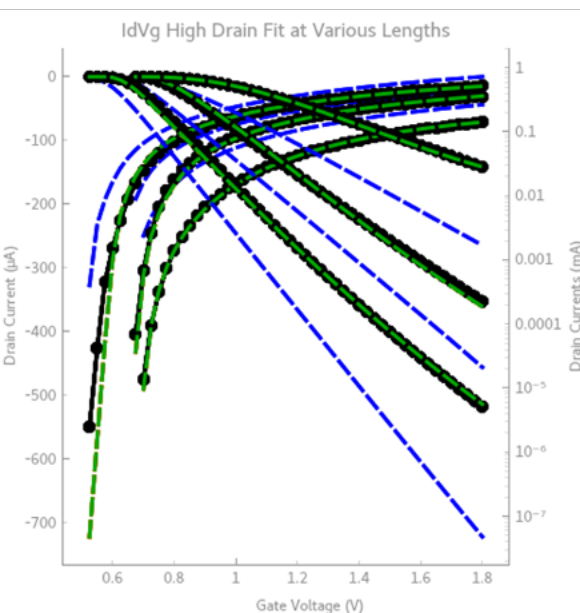
- Modelling of GF 22nm FDSOI and GF 28nm HV (bulk)
- PDK-compatible BSIM Independent Multi-Gate* for 4K
- Measurement and modelling of high voltage devices at 4K
- Measurements of transistors at 4K
- Development of simplified EKV model for analog design
- Low noise test structure measurements



* C. Hu et al., "BSIM-IMG: A Turnkey compact model for fully depleted technologies," 2012 IEEE International SOI Conference (SOI), Napa, CA, USA, 2012, pp. 1-24, doi: 10.1109/SOI.2012.6404352.

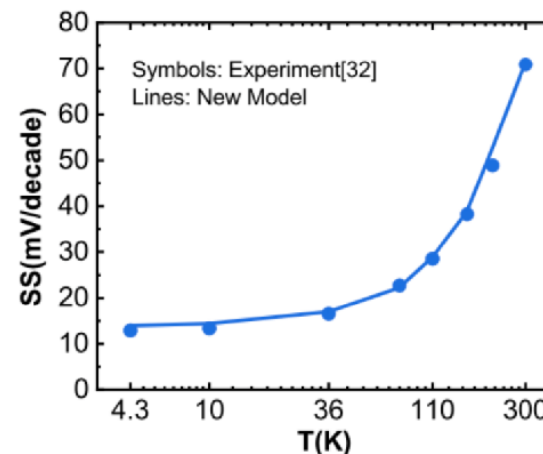
Fermilab: GF22nm FDSOI cryo-PDK development

- ❖ Developed at Fermilab in collaboration with Synopsys
- ❖ 22nm FDSOI cryo-PDK: isothermal BSIM-IMG (PDK distribution) model at 4K
 - ▶ E.g.: high drain length extraction (stage 5) (data, [foundry model simulated at cryo](#), [custom cryo models](#))



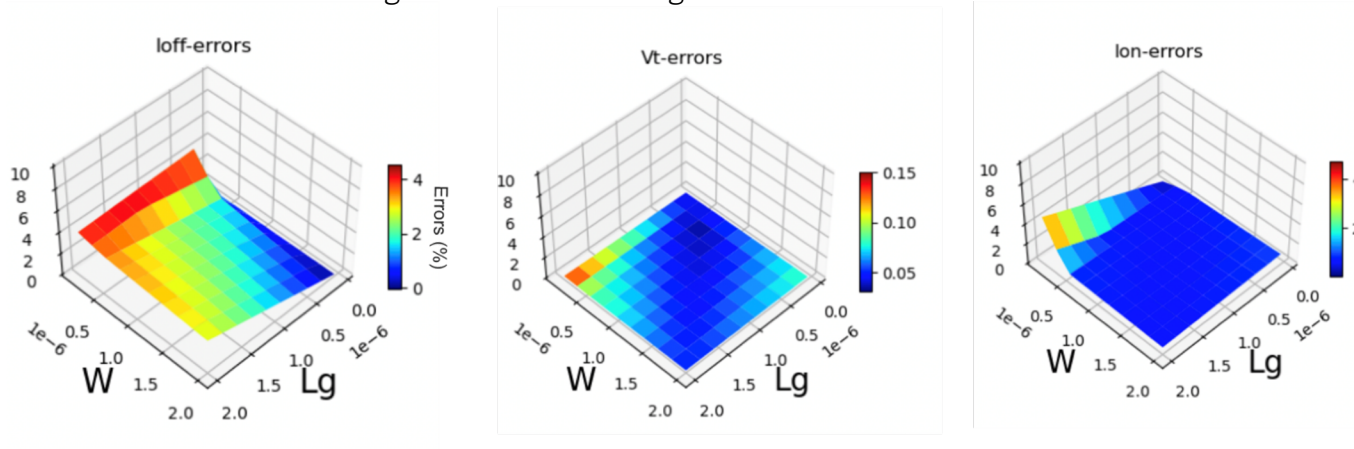
Workflows for parameter extraction and PDK development

- Take the 22nm PDK provided by global foundries for these devices and **re-extract** the parameters we think will change at cryo
- Keep a **basis in physics** by setting reasonable parameter ranges based on literature when applicable
- Change the input pdk:
 - BSIM-IMG 102.8 doesn't include effects like subthreshold slope saturation [14], we need to model that saturation by setting **temp=tnom** to the value where our **subthreshold slope saturates**
- **Isothermal** model
- We will then place these extracted values back into the PDK

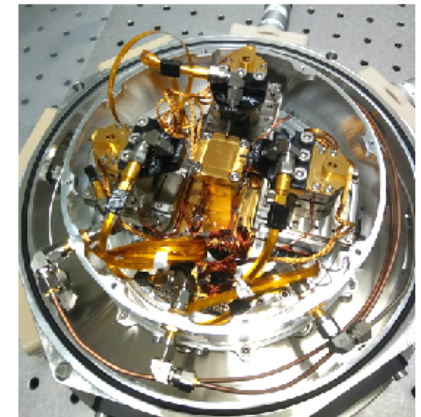
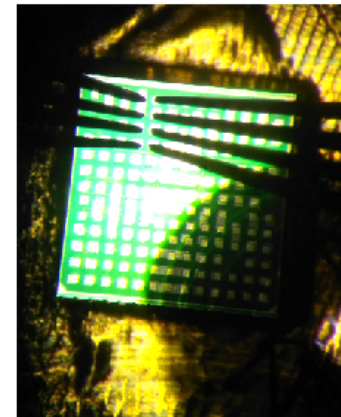
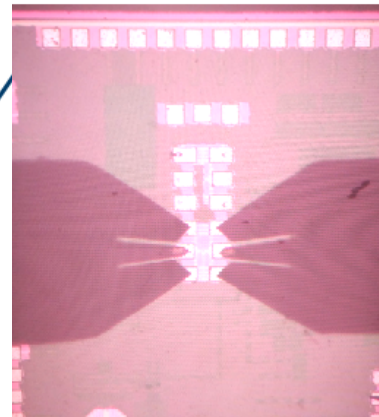
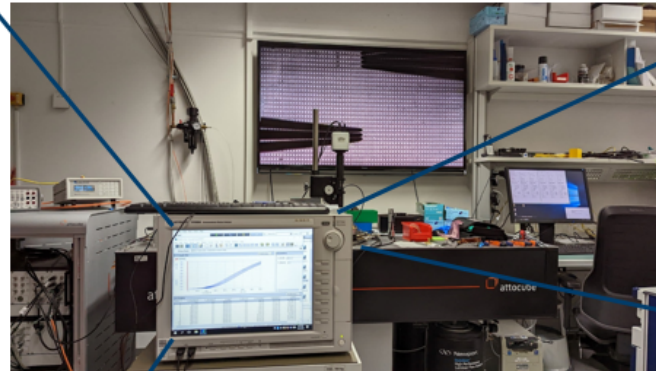
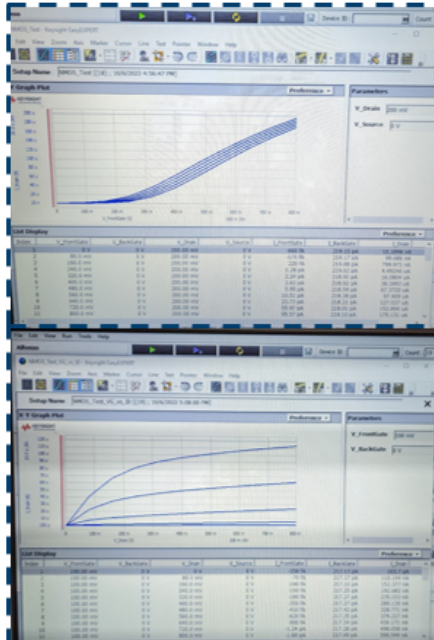


Subthreshold Slope Saturation as a function of Temperature [14]

Errors across figure of merit for all lengths and widths are well constrained



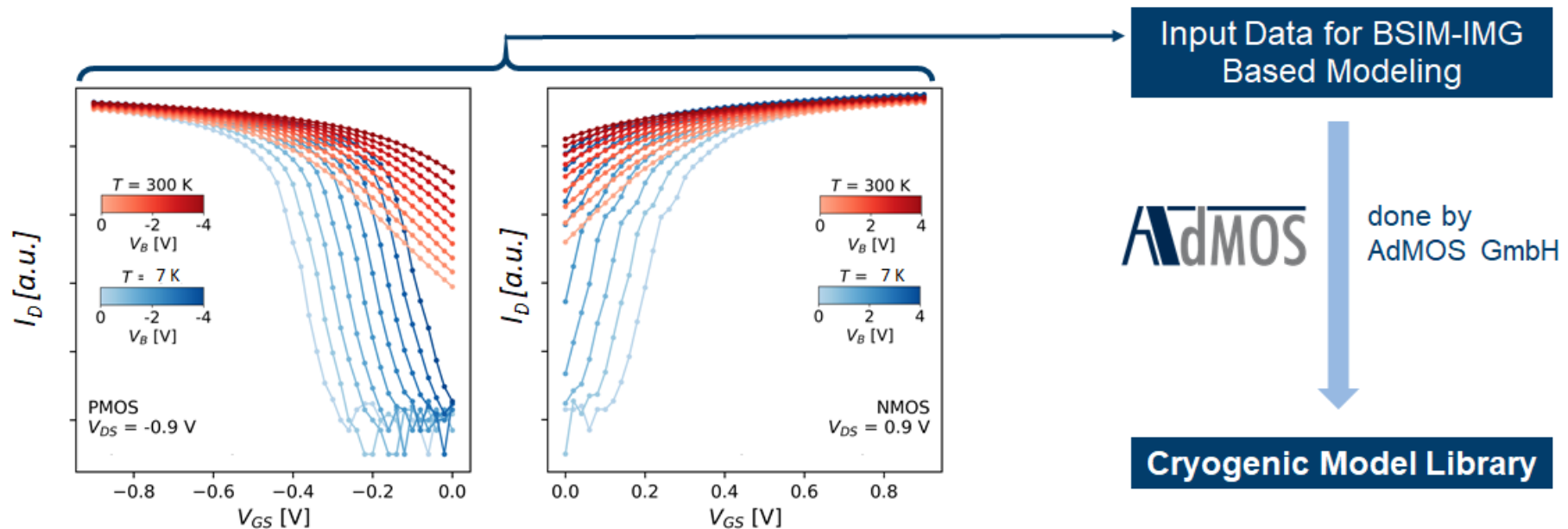
Cryogenic probe setup for RF/DC measurements at FZJ



- B1500A Semiconductor Device Analyser
- attoDRY800; down to 6K with needle probing station
- Accurate device models in simulations

[1] A. A. Artanov et al., "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures," in *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 900-904, March 2022, doi: 10.1109/TED.2021.3139563.

Workflows for parameter extraction and PDK development



Multiple geometries across different temperatures measured!

[1] Phanish Chava et al., Evaluation of Cryogenic Models for FDSOI CMOS Transistors Wolte 16.

GlobalFoundries 22nm FD SOI cryo-PDK



Semiwise, sureCore, and Cadence Showcase Breakthrough in Cryogenic CMOS Circuit Development for Quantum Computing and Energy-Efficient Data Centers

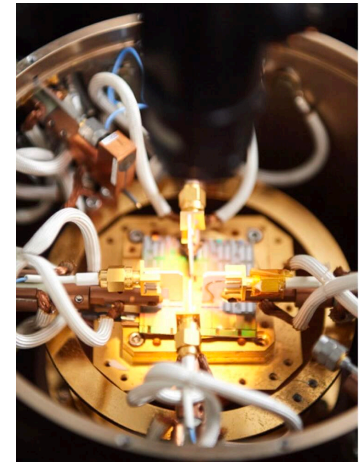
20 Jun 2024



Semiwise, sureCore, and Cadence have collaborated to overcome critical challenges in developing cryogenic CMOS circuits. (...) this collaboration springs from the Semiwise **Innovate UK project** “Development of CryoCMOS to Enable the Next Generation of Scalable Quantum Computers,”

Modification of transistor models on **GlobalFoundries 22FDX®** in the **Cadence® Spectre®** Simulation Platform, thereby enabling the process of analog, mixed-signal, and digital **circuit simulation and verification at cryogenic temperatures**

Production-worthy designs for cryogenic CMOS circuits by using cryogenic transistor measurements (...) in conjunction with a leading commercial TCAD simulator. This allowed us to create PDK-quality compact **transistor models that include corners and mismatch**



<https://www.semiconductorwise.com/press-releases>

https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr/2024/semiwise-surecore-and-cadence-showcase-breakthrough-in-cryogenic-cmos-circuit-development.html

measurement data was used by SemiWise to develop new transistor models including both Typical-Typical (TT) transistors as well as corners (SS, FF) that will enable reliable circuit design for use at 4K and 77K.

GlobalFoundries 22nm FD SOI cryo-PDK



Siemens collaborates with sureCore and Semiwise to pioneer quantum computing ready cryogenic semiconductor designs

The Siemens logo is centered in the slide. It features the word "SIEMENS" in a bold, white, sans-serif font, set against a solid teal rectangular background.

20 Dec 2023

Collaboration between Siemens, sureCore and Semiwise to develop cryogenic semiconductor designs capable of operating in extreme cold conditions required for quantum computing”

Using advanced analog/mixed-signal IC design technology from Siemens, Semiwise has developed **cryogenic CMOS circuit designs featuring cryogenic SPICE models** as well as **SPICE simulator technology** that can perform accurate analyses at cryogenic temperatures.

Semiwise is providing this intellectual property (IP), developed using Siemens’ Analog FastSPICE (AFS), to sureCore for the development of sureCore’s revolutionary line of CryoIP, which aims to enable the design of CryoCMOS control chips seen as crucial for unlocking the commercial potential for quantum computing.

sureCore is rapidly progressing towards its first CryoIP tapeout, leveraging **GlobalFoundries’ 22FDX® PDK.**

<https://newsroom.sw.siemens.com/en-US/siemens-eda-quantum-cryogenics/>

sureCore Cryo-IP for QC control chips



<https://www.sure-core.com/products-and-services/#cryoip-product>

sureCore is developing a range of **CryoIP™** suitable for operation at the extremely low temperature required for **Quantum Computing (QC)** applications.

By working closely with both industry partners and foundries, we plan to design and characterise **silicon IP capable of operation down to 4°K**

sureCore already has silicon-proven, ultra-low power, embedded memory IP that it will customise for this Cryo application and will be launched as its **CryoMem™** range. Using the knowledge gained from the development of **CryoMem**, sureCore plans to create a range of IP tailored for the **development of complete QC control electronics in Cryo-CMOS**. The company will offer a complete portfolio of this CryoIP for licensing by companies wishing to develop Cryogenic control ICs.

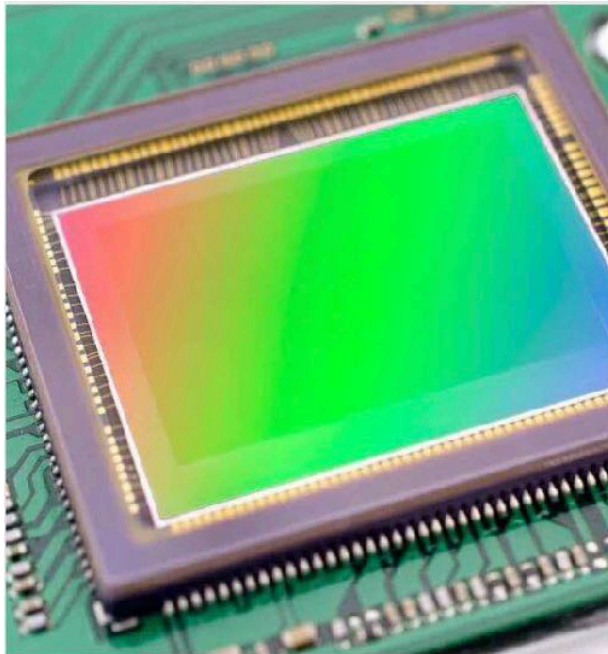
HIGHLIGHTS

- Specially Engineered CryoCMOS IP
- Characterised down to 4°K
- Minimal Power Dissipation
- Reduces Thermal Load
- Standard Cell Library Recharacterisation
- IP Portfolio for Cryo-ASIC's
- SRAM, ROM, Register file compilers
- ADCs, DACs & Temp sensors

MARKET APPLICATIONS:

- CryoASIC Design for Quantum Computers
- CryoASIC Design for High Performance Computing





Process Features for 90 nm ROICs

Specialized devices and structures to enable high resolution and sensitivity thermal imaging systems and sensor arrays.

- **Cryo models at 45 K, 77 K, 120 K, 150 K**
- Dual stack MiM caps with various configurations
- Tungsten filled through silicon vias, or TSV, for stacked die configuration
- Topside planarization with pixel contacts
- Stitching support for large format die
- Communication interfaces
- Rad-Tolerant 90 nm process baseline

****Main flow models were simulated at a minimum temperature of -40°C for a commercial environment and at 45K and between 77K and 150K for a cryogenic environment. ROIC flow models were simulated at a minimum temperature of -55°C for a military environment and between 77K to 150K for a cryogenic environment.**

Technology	RH90*	S90/S90LN	S130
Cryo Models	No	45K, 77K, 120K, 150K**	No

<https://www.skywatertechnology.com/cmos/>

SkyWater Establishes Cryogenic Lab, Utilizes FormFactor's Leading Tool for RTS Noise Detection in Read-Out Integrated Circuit Applications

21 Mar 2023

Public-private partnerships support SkyWater's leading-edge domestic capabilities and advancement of ROIC technology

Mitigating RTS noise is crucial to improving the image quality and performance for ROIC customers in various applications

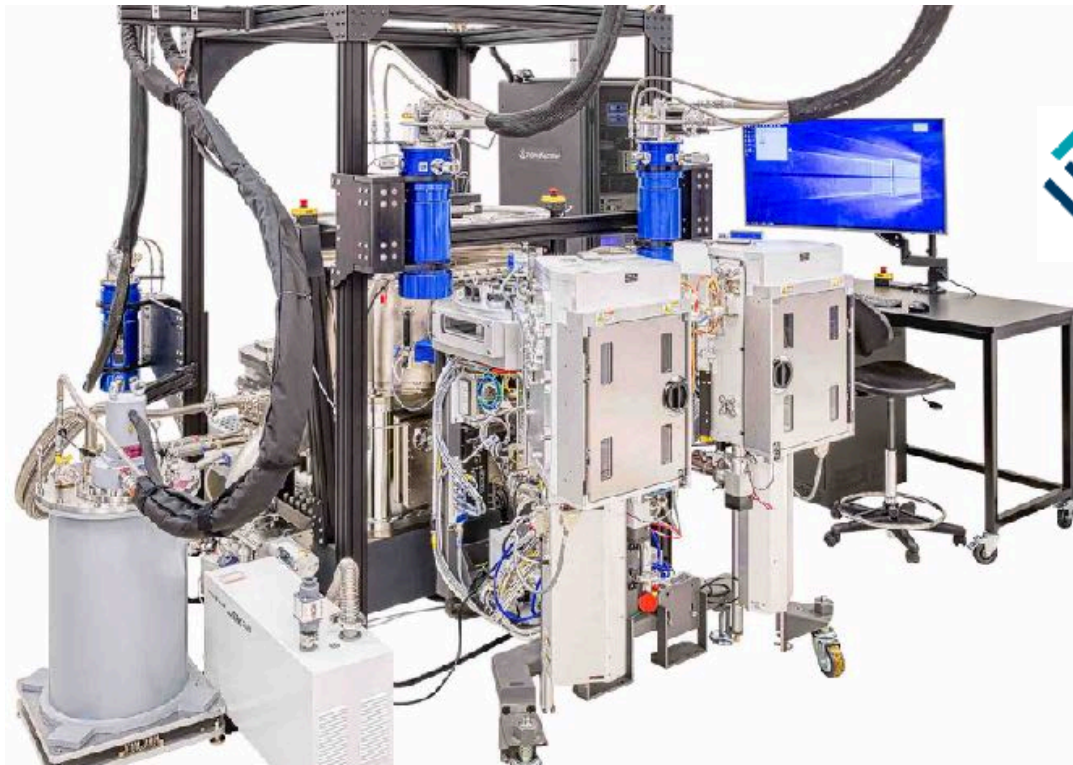
SkyWater's cryo lab utilizes FormFactor's leading **cryogenic probe system that enables precise **on-wafer measurements in extreme environments**. SkyWater partnered with the University of Tennessee at Chattanooga and Arizona State University's electrical engineering teams to develop test chips which are used to determine how much RTS noise exists for various transistor types and temperatures. From these measurements, enhancements are made for improved imaging.**



<https://www.skywatertechnology.com/skywater-establishes-cryogenic-lab-utilizes-formfactors-leading-tool-for-rts-noise-detection-in-read-out-integrated-circuit-applications/>

FormFactor cryogenic wafer testing

- Singulated die characterization at sub-50 millikelvin and high-throughput **wafer probing from sub 4K to 77K.**
- **Cryogenic** custom probes and **probe cards** for both DC and RF measurements (>20 GHz)
- Full scale wafers (150-200-300mm) down to 4 K using fully automated probe movement.



<https://www.formfactor.com/sales-service/cryogenic-test-services/?creative=691604908769&matchtype=b&network=g&device=c&adposition&keyword=cryogenic%20measurements>

Wafer Cryo-Probing station (77K) at INFN LNGS



- PAC200 Cryoprobe for 8" wafer measurements at 77K currently operating at INFN LNGS
- In operation since 2023 for the test of 1400 Silicon Photomultiplier wafers for Darkside-20K
- Turnaround 20 wafers per week (60% cool-down and warm-up, 40% measurement)

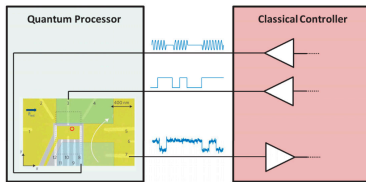
Pause.

Might be useful to set a new ground for this discussion,
reviewing some definitions used herein

“Deep Cryogenic” electronics for Quantum technologies

- ▶ Ongoing and boosted R&D in academia and industry for the development of novel quantum sensing and control electronics through the consolidation and scaling up of existing solutions or emerging process and integration technologies;
- ▶ provide advanced enabling infrastructures and key capabilities for the development of cryogenic electronics in order to solve “the wiring bottleneck” on quantum computers;
- ▶ cryogenic CMOS operating <4K and down to the mK will pave the way for scalability into the million qubit realm.

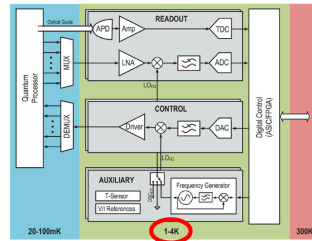
Classical Controller



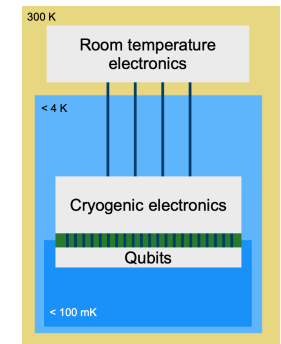
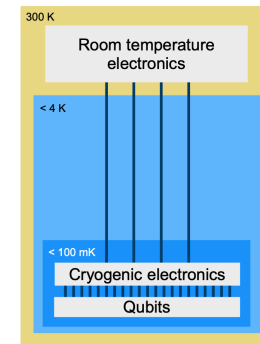
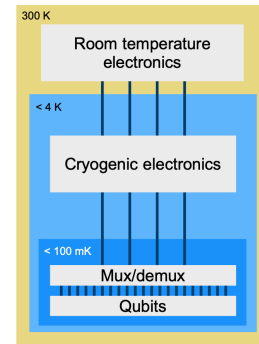
- Electronics to control and read-out the quantum processor mostly operated at room temperature (RT)
- Does not scale with the number of qubits

□ E. Charbon, ESSCIRC 2019.
 □ B. Patra, et al., JSSC, vol. 53, no. 1, 2018.

CMOS Integrated Controller



- More scalable approach by moving the control and read-out electronics closer to the qubits and operate it at cryogenic temperature (around 4 K)



C.ENZ, A. BECKERS and F. JAZAER, “MOSFET Compact Modeling down to Cryogenic Temperatures”

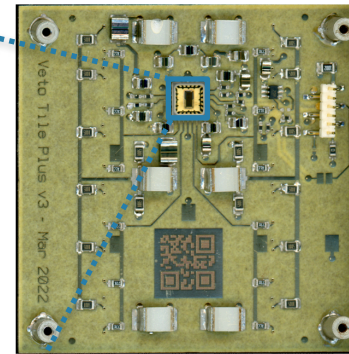
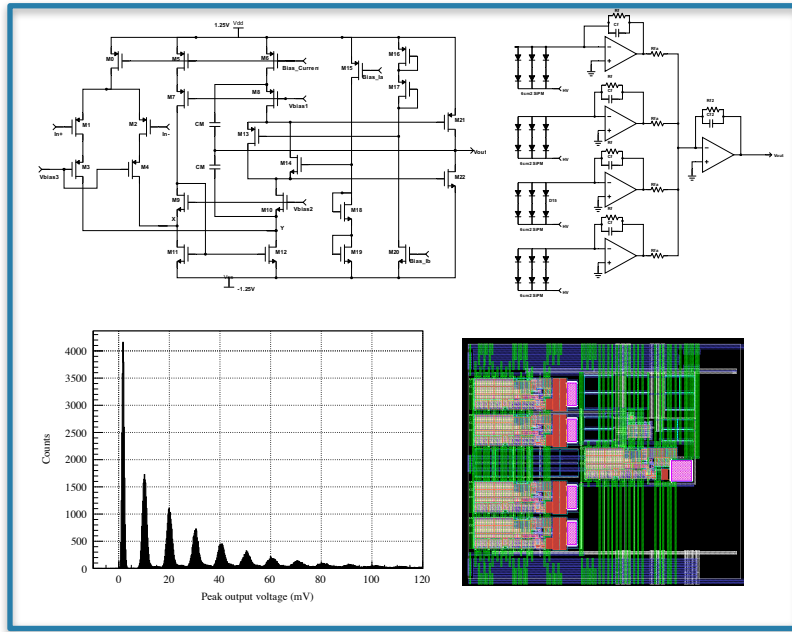
C. DEGENHARDT, “Cryogenic QUBIT Control – The Tyranny of numbers, self-heating and everything”

“Mild cryogenic” electronics e.g. Noble Liquid Detectors

- Rare-event search on astroparticles: neutrino physics and direct dark matter detection using Liquid Argon or Xenon;
- Single and dual-phase detectors employing (solid-state) photon sensors require front-end readout electronics operating at 165K (LXe) or 88K (LAr), e.g. Darkside-20K.

ASIC designed at INFN Torino for the Darkside-20K

VETO Detector (3200 chips). OPAMP schematics and summing scheme for the cold readout of a vTile with 24 FBK NUV-HD Cryo 1 cm² SiPMs. Histogram with pulsed laser and CAD layout.



Darkside-20K Veto Tile:

Arlon-55NT substrate, hosts 24 SiPMs on front, front end QFN-20 packaged ASIC electronics on back;



Darkside-20K Motherboard:

Sums signals from 16 vTiles organised in 4 quadrants - 4 differential analogue output channels.

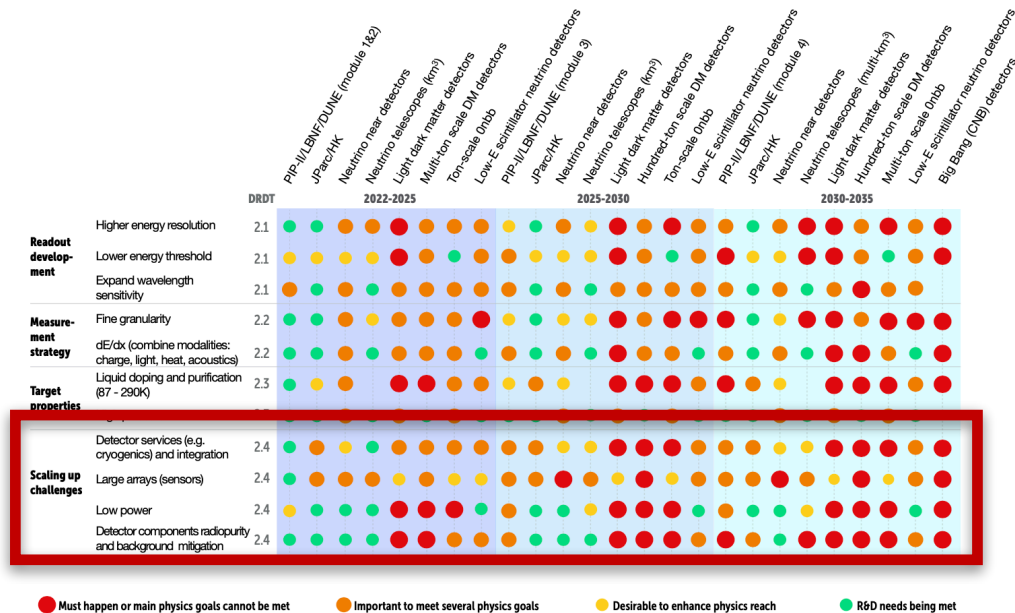
Need to commit to strong R&D programs for the development and deployment of new readout schemes suitable for future large-scale neutrino and dark matter detectors; today's solutions are not scalable.

Experiment	Type	Photon detector	Area (m ²)
nEXO	LXe	SiPMs (FBK [Ch2-18], Hamamatsu [Ch2-19]), digital 3D-SiPM	5
DARWIN	LXe	PMTs, SiPMs or Hybrids (SIGHT, ABALONE)	8
TAO	LSci	FBK SiPMs	10
DarkSide-20k	LAr	SiPMs (FBK NUV-HD triple-dopant)	30
ARGO	LAr	SiPM is baseline option	200
DUNE	LAr	Light guide or trap + SiPM	10-1000

Noble Liquid Detectors: future facilities with cold readout and scalable DSP

Future larger scale experiments will call for innovative **cold integrated readout electronics implementing digital signal processing** within the photosensor detection module.

“R&D on the 5-year horizon for greater integration include (...) dedicated ASIC design; 3D-vertical integration R&D; and development of lower-power, larger-area and lower-radioactivity photodetection modules.”



Scaling up with **cryogenic mixed-signal CMOS based photodetector technology.**

- DRDT 2.1 - Develop readout technology to increase spatial and energy resolution for liquid detectors → achieve readout of more **highly pixelated detectors** with greater **photon collection capabilities**.
- DRDT 2.2 - Advance noise reduction in liquid detectors to lower signal energy thresholds → future liquid detectors requires R&D to achieve **lower sensor and electronics noise**.
- DRDT 2.4 - Realise liquid detector **technologies scalable for integration in large systems** → detectors with sensor areas reaching 10, 100 and ultimately 1000 m².

The DRD7.4.a “Device modelling and Development of Cryogenic CMOS PDKs and IP”

- Target technologies: TSMC 28nm
- Parameter extraction down to 4K, corner temperatures: LXe, LAr, LHe
 - involvement of an industrial partner for cold-PDK design
 - Create infrastructures and tool competences for future in-house cold-PDK development
- Development of core mixed-signal CMOS Cold-IPs: ADCs, TDCs, DACs, LVDS transceivers, SPI, bandgaps,...
- Characterisation, documentation and repository of a Cold-IP Library
- Development of a small-scale (MPW) cold demonstrator chip:
 - Single-photon detector with excellent timing performance
 - Multi-channel/pixel CMOS mixed-signal IC
 - Exploring die/wafer-level integration techniques
 - Scalable, low-power and low-noise architectures

Project Name	Device modelling and Development of Cryogenic CMOS PDKs and IP (WP7.4a)
Project Description	Device modelling from selected CMOS technology nodes, development of “cold” Process Design Kits (PDKs), design and characterisation of mixed-signal CMOS IP blocks and demonstrator chips for photon detection in (LAr, LXe) noble liquid experiments, quantum computing interface and sensing.
Innovative/strategic vision	The aggregation of the international research teams will create the critical mass needed for the construction of infrastructures and tools, needed for device characterisation and modelling, towards the development of cold PDKs and cold-IP blocks. These will be made available to a wider community working towards the construction of frontier particle and photon cryogenic detectors.
Performance Target	cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K, cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip.
Milestones and Deliverables	D7.4a.1 (M9) Deliver a specification and requirements document for a full-chip demonstrator. M7.4a.2 (M18) Cold-PDK for TSMC28nm complete M7.4a.3 (M26) Tapeout of full-demonstrator chip D7.4a.4 (M38) Deliver a report of full-demonstrator silicon chip characterisation.
Multi-disciplinary, cross-WP content	The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for operation at cryogenic temperatures, will pave the way for the development of cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs for DRD2 and DRD5.



Fermilab: 65nm cryo models and IPs

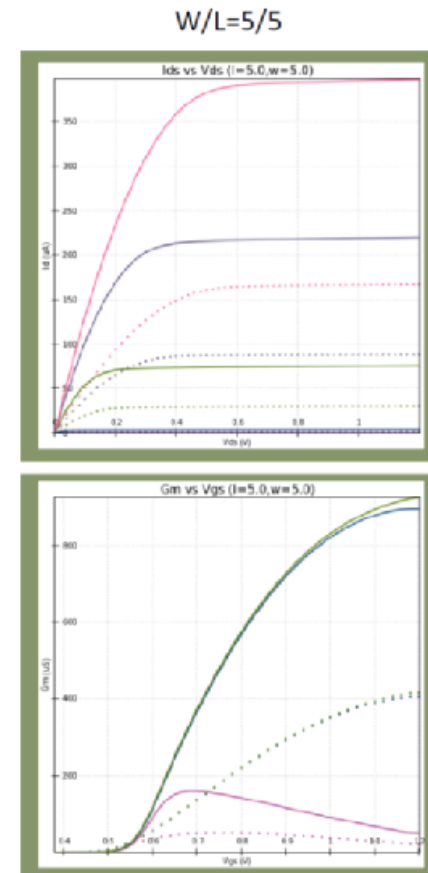
Creation of cryogenic CMOS models (T=-189C) by vendor based on test structures and data collected by FNAL, SMU, BNL groups.

- Isothermal (valid for T=25C and T=-189C only)
- Flicker noise parameters were verified with low temperature data in this release.
- Supports the following simulation **corners**: tt, ss, ff, sf, fs and **mismatch**.
- Mismatch variations are from the original foundry model

65nm IPs

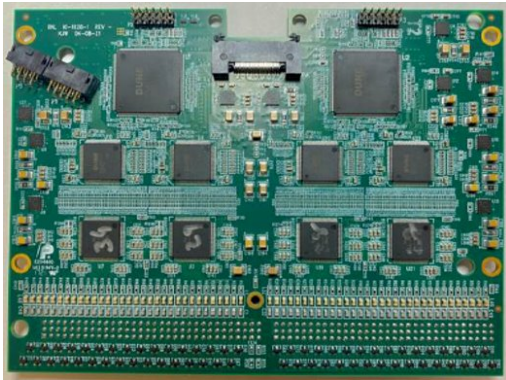
LVDS Tx and Rx, POR, Bandgap, level shifters, IOs, etc.

Others developed in collaboration with LBNL, BNL, SMU (**COLDATA**, **COLDADC**)



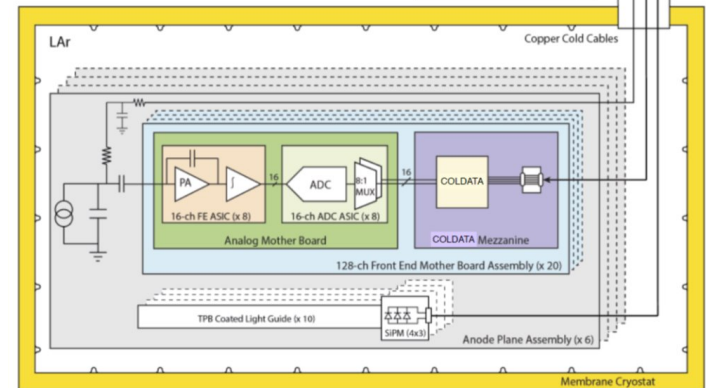
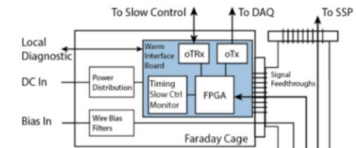
Cold ASICs for DUNE

- ❖ 16-channel front-end ASICs for amplification and pulse shaping (LArASIC - BNL);
- ❖ 16-channel 12-bit ADC ASICs operating at 2 MHz (ColdADC – LBNL+FNAL+BNL);
- ❖ 64-channel control and communications ASICs (COLDATA – FNAL+SMU)



ASIC	Quantity
Front End (LArASIC)	24000
ADC (COLDADC)	24000
Data Concentrator (COLDATA)	6000

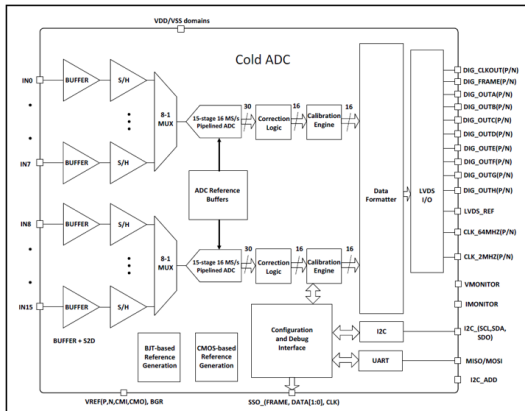
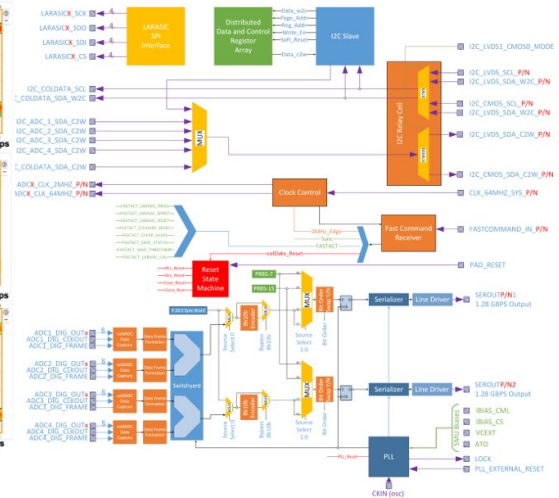
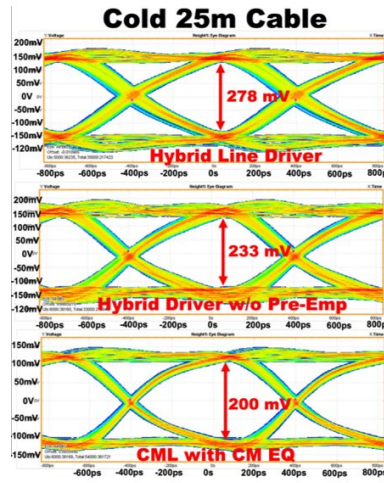
- ❖ Current working on:
 - ▶ SiPh for readout and power delivery
 - ▶ Cryo dSiPM for large area coverage
 - ▶ Coordinating with other institutes for pixelated readout schemes with >100M channels (<100μW/channel) (e.g. Qpix)



Cold ASICs for DUNE

COLDATA (FNAL, SMU)

- data concentrator and communicator that interfaces with electronics outside the cryostat. Each COLDATA services 4 LArASIC/ColdADC pairs (64 input channels)
- Concentrates data from 64 front end channels into two 1.25 GHz serial lines.
- provides clock generation and control, slow and fast command response, and reset control for the Front-End Motherboard



MEASURED RESULTS

	290 K	77 K	Units
CMOS Technology	65	65	nm
Number of Channels	16	16	
Channel Sampling Rate	2	2	MS/s
ADC Resolution	12 or 14	12 or 14	bits
Full-Scale Range	3.0	3.0	V-ppdiff
Noise (input referred)	207	130	μ V-rms
DNL (after dielectric absorption correction)	-0.3 / 0.4	-0.4 / 0.3	LSB (12-bit)
INL (after dielectric absorption correction)	-0.8 / 0.7	-0.7 / 0.6	LSB (12-bit)
Channel-to-Channel Crosstalk	0.35	< 0.06	%
SNDR	70.5	72.9	dB
SFDR	82.6	82.1	dB
ENOB	11.4	11.8	bits
Power Dissipation	371	332	mW
Die Area	52.4	52.4	mm ²

COLDADC (LBNL, FNAL, BNL)

- 65nm CMOS
- Two 15-stage pipeline ADCs operating at 16MHz
- Digital calibration with automatic calibration
- For both single ended and differential input signals
- 11.8b ENOB at 77K

Grace, C., et al. "ColdADC_p2: A 16-channel cryogenic ADC ASIC for the deep underground neutrino experiment." *IEEE Transactions on Nuclear Science* 69.1 (2021): 105-112.

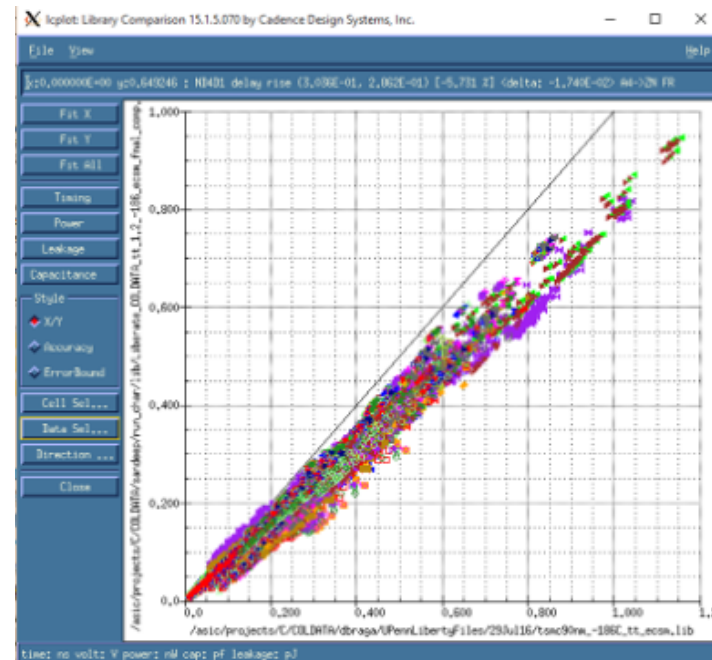


Fermilab: 65nm cryo-models and Digital IPs

Custom Standard Cells Digital Library (L=90nm)

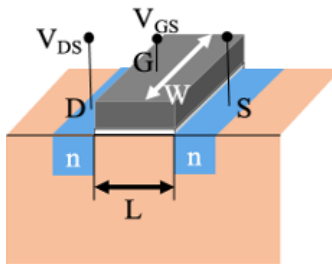
- L=90nm to reduce hot carrier effects (pMOS also increased to maintain balance)
- ~230 cells (4 or 5 different drive strengths per logic gate)
- Inherently slower than 60nm library (30% slower)
- 9-track
- Area penalty of 10 to 20%
- DRC clean
- Layout, schematic and abstract views

STA library characterization: timing and power libraries



Type	Sub-type	Cells
Combinatorial	Simple Logic	INV, BUFF, BUFT, ND, NR, AN, OR, XNR, XOR
	Complex Logic	AO, OA, AOI, IAO, IOA, OAI, IND, INR, MUX
Storage	Latch	Latch LH (Latch with High Enable), LN (Latch with Low Enable)
	Flip-Flop	DF (D Flip-flop), DFK (synchronized set/reset D Flip-Flop), DFN (negative clock trigger D Flip-Flop)
Special	Delay cell	DEL
	Clock Buffer	CKB, CKN
	Clock And	CKND2, CKAN2
	Clock XOR	CKXOR2
	Adder	FA1 (1-Bit Full Adder), HA1 (1-Bit Half Adder)
	Antenna Diode	ANTENNA
	Tie-high / Tie-low Cell	TIEH, TIEL
	Filler Cell for Core	FILL
Decoupling Cell	DCAP, DCAP4, DCAP8, DCAP16, DCAP32, DCAP64	

Parameter extraction of CMOS 180nm technologies at KEK



Characterisation of TSMC 180nm and Silterra 180nm nodes

Methods

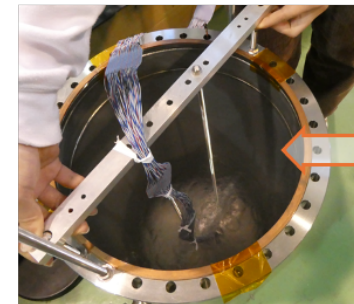
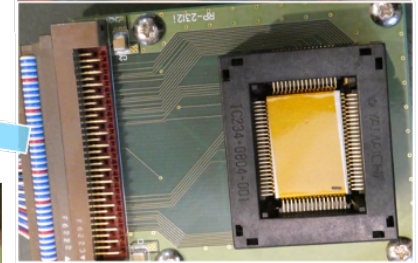
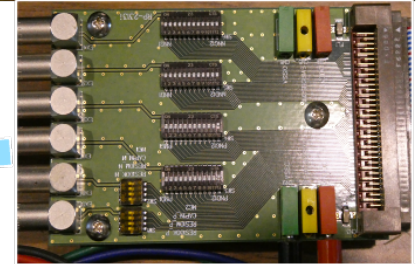
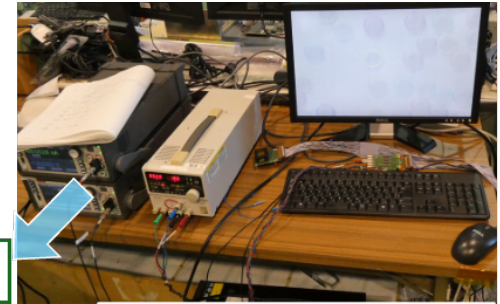
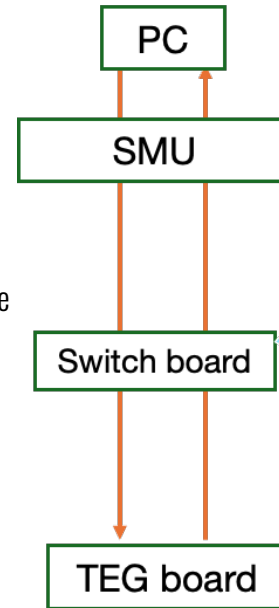
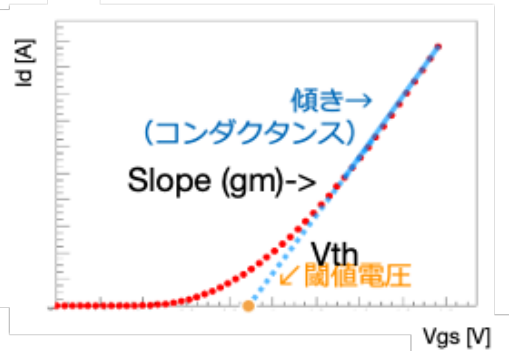
- V_{ds} : fixed at 1.8V
- V_{gs} : sweep between 0 to 1.8V with 50 steps

NMOS/PMOS with different channel lengths and widths

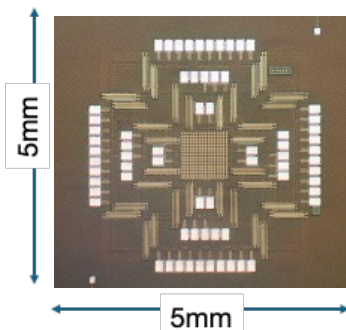
L [um]	W [um]
10	10
10	0.22
5	5
5	0.44
2	2
0.72	0.88
0.36	5
0.36	0.44
0.36	0.22
0.18	10
0.18	0.44
0.18	0.22

Id-Vgs characteristics

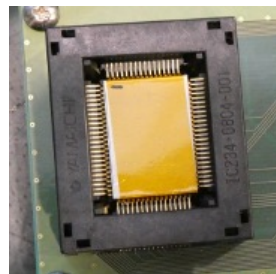
- Slope: line fitting with linear region
- Threshold voltage (V_{th}): extrapolate with linear line



TEG chip was placed in LN2 (77 K) dewar.



PCMTEG



After packaging

Low Temperature Readout System (LTARS)

LTARS2018_K06B

(silterra 180 nm process CMOS)

- Working properly at room temperature.
- Degraded performances (V_{th} shift) at LAr temperature.



LTARS2020

(silterra 180 nm process CMOS)

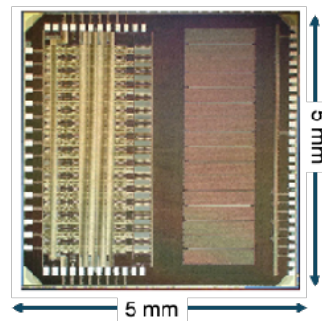
- On-chip bias circuit based on the feedback principle compensates the threshold shift.
 - ▶ Performances at room temperature and LAr temperature satisfied the requirements.



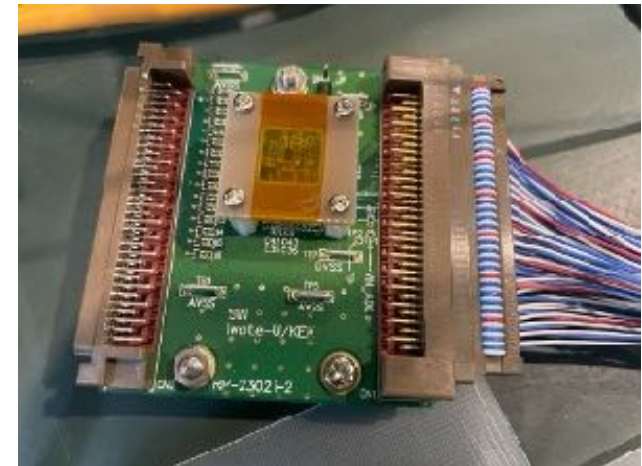
LTARS16A

(TSMC 180 nm process CMOS)

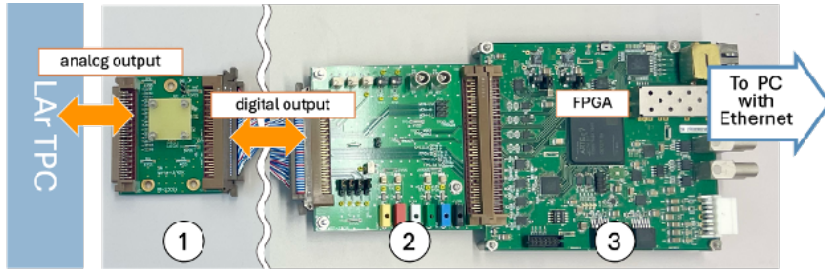
- AD conversion in ASIC for reducing noise during data-transmission with long cables.
- Readout 4000 samples at 2.5MS/s, corresponds to 1m drift length at 1.6 mm/ μ s drift velocity)
- Switchable trigger mode (external or internal)
- Two operating modes (trigger/continuous readout mode)
- Two outputs from High-Gain and Low-Gain paths



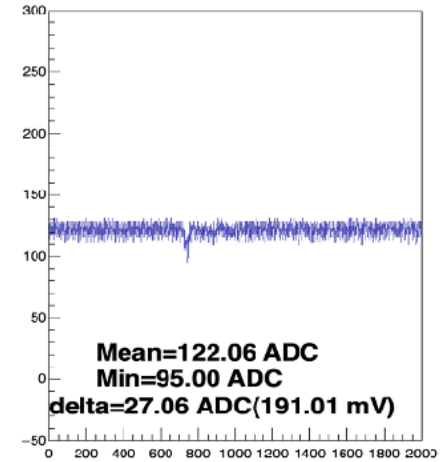
Parameter	High Gain (HG)	Low Gain (LG)
Peaking Time	1 μ s (Fast), 4 μ s (Slow)	
Gain	10 mV/fC	0.5 mV/fC
Dynamic Range	± 80 fC	± 1600 fC
ENC	$< 3000 e^-$	$< 62500 e^-$



Test or the LTARS16A on a TPC

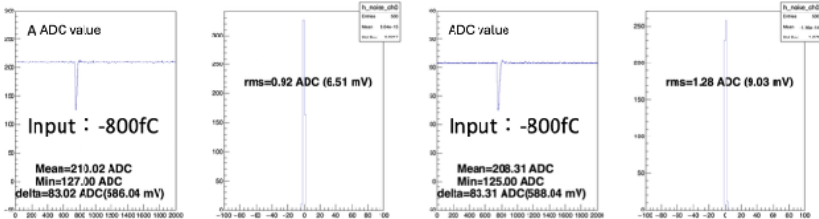
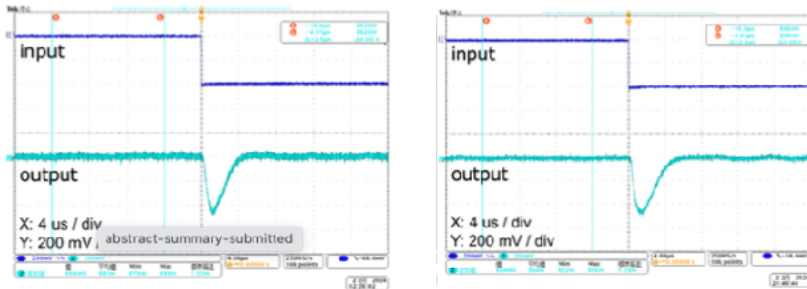


- TPC is filled with gas argon.
- ^{241}Am (alpha source) is set under the anode pad.



Room temperature

LN₂ temperature



- ① LTARS16A board
- ② Power supplies and parameter tuning board
- ③ Custom FPGA board for DAQ



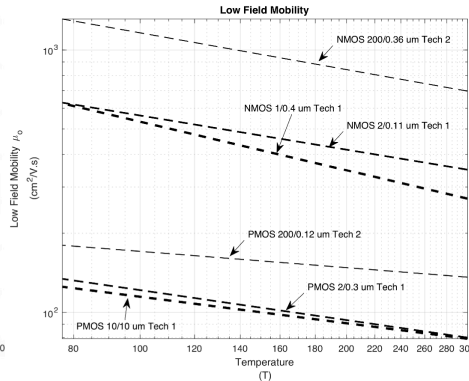
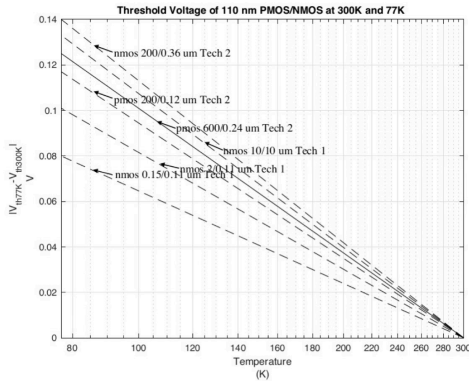
Poster at this Workshop:
Ayumi Morita: Development of Low Temperature Electronics for LAr-TPC

https://indico.cern.ch/event/1381495/contributions/5988522/attachments/2869339/5161340/TWEP2024_poster_morita.pdf

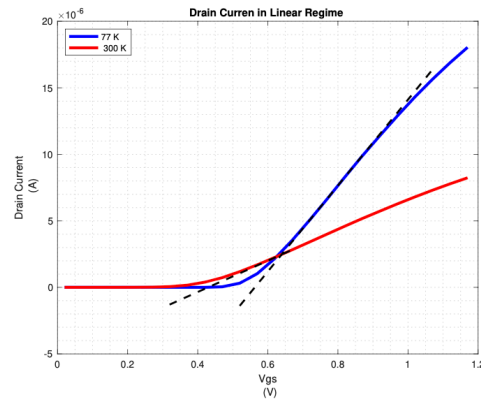
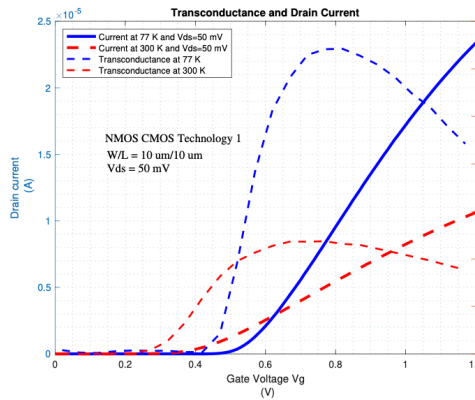
Parameter extraction of CMOS 110nm technologies at INFN



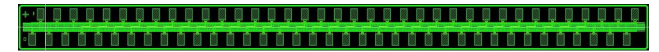
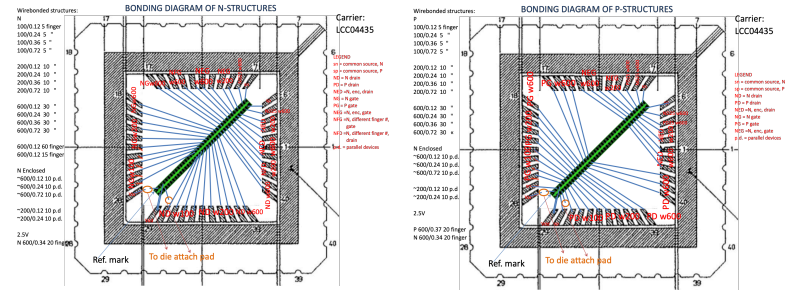
- UMC110nm test chip by PSI and Uni. Bergamo
- LF11is PCMTEG structures by the foundry
- Both tested at INFN Torino at RT and 77K
- Extraction of DC parameters for PMOS and NMOS with different geometries



Threshold voltage (left) and low-field mobility (right) of two CMOS 110nm nodes at temperature corners (300K, 77K)

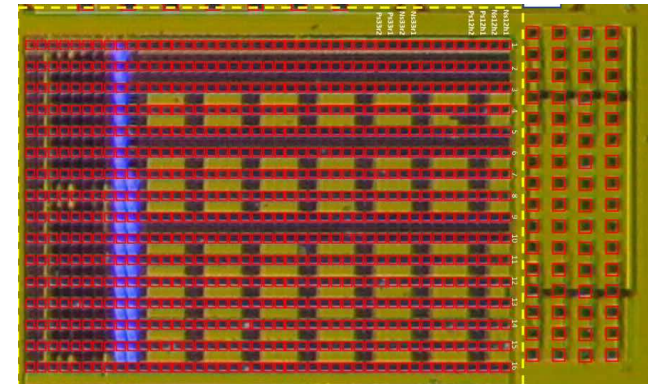


Drain current and transconductance at RT and 77K, Vth is extracted with a linear interpolation of the Ids curve



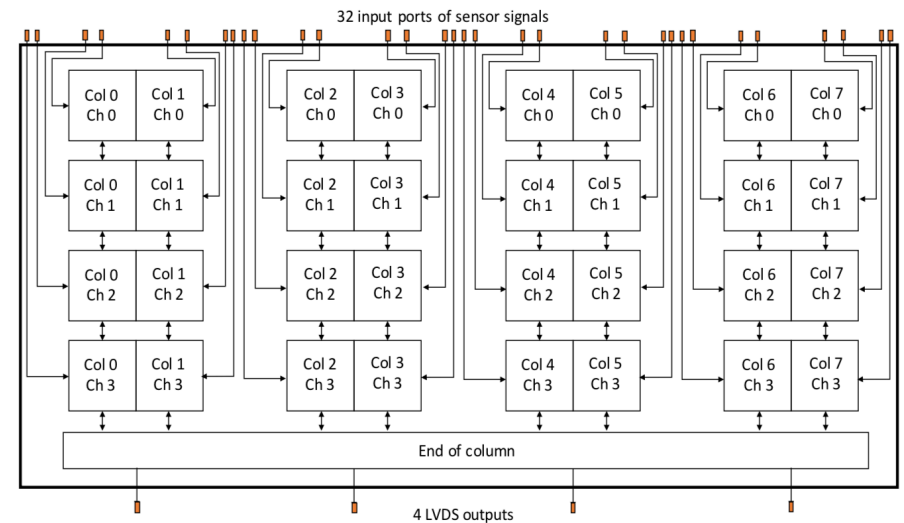
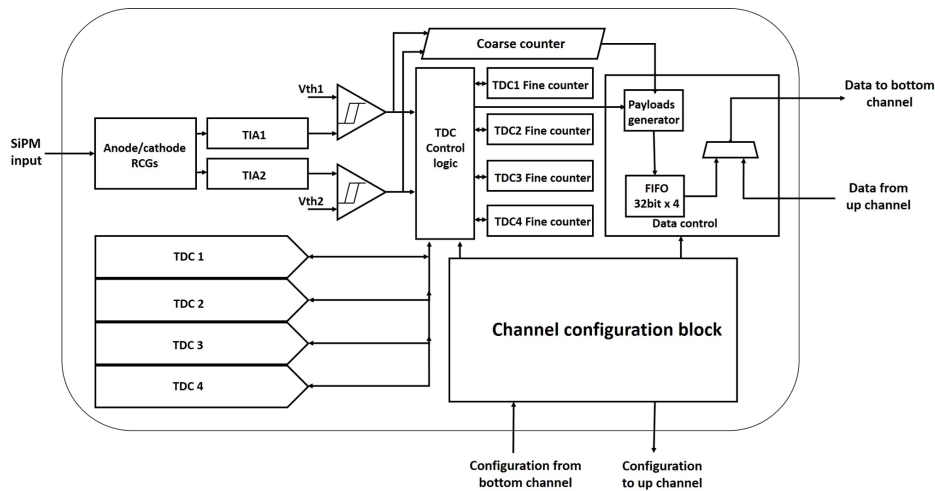
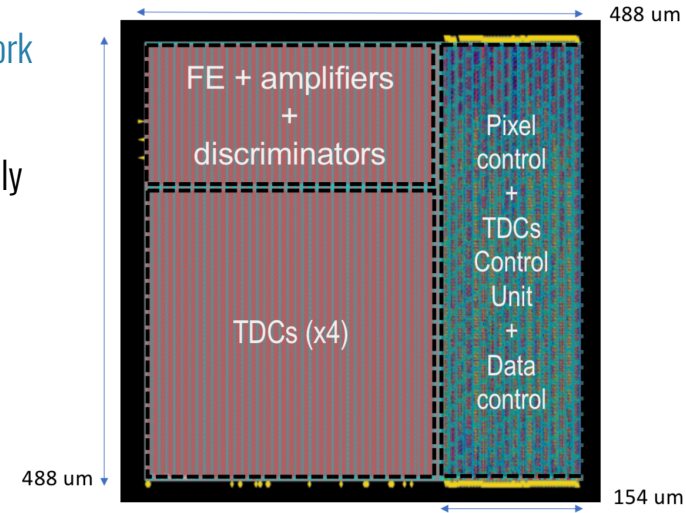
Total Ionizing Dose Effects on CMOS Devices in a 110 nm Technology

Elisa Riceputi*, Massimo Manghisoni*, Valerio Re*, Luigi Gaioni*, Roberto Dinapoli* and Aldo Mozzanica*
 *Università di Bergamo, Dipartimento di Ingegneria e Scienze Applicate, Viale Marconi 5, 24044, Dalmine (BG), Italy
 †Paul Scherrer Institut, 5232 Villigen PSI, Switzerland



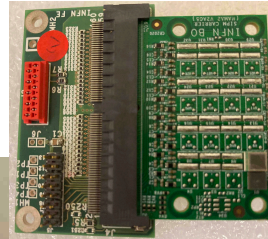
ALCOR ASIC for SiPM readout at low temperature

- 32-pixel matrix mixed signal ASIC (CMOS UMC 110nm) developed by INFN in the framework of Darkside-20K (DM direct detection with LAr), optimised for operation at 77K
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O
- Single-photon time tagging mode or time and charge measurement
- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- 4 LVDS TX data links, SPI configuration, operation up to 320 MHz (TDC binning 50 ps)

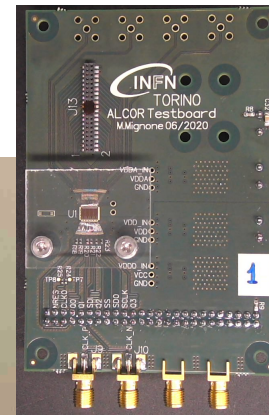


The Cold Test Setup

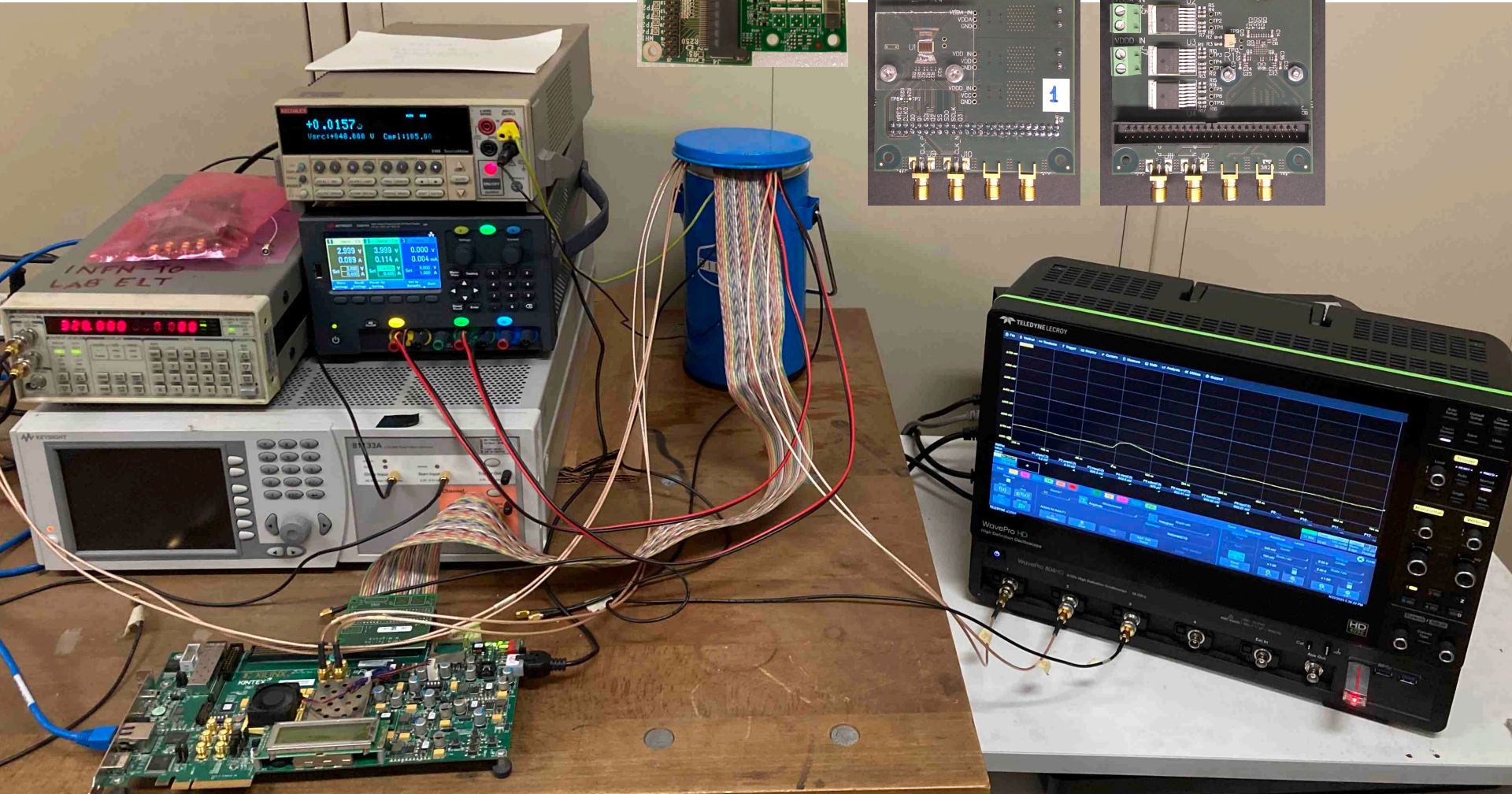
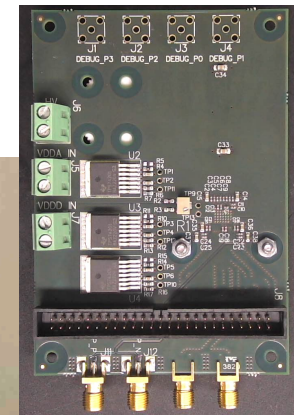
SiPM Carrier



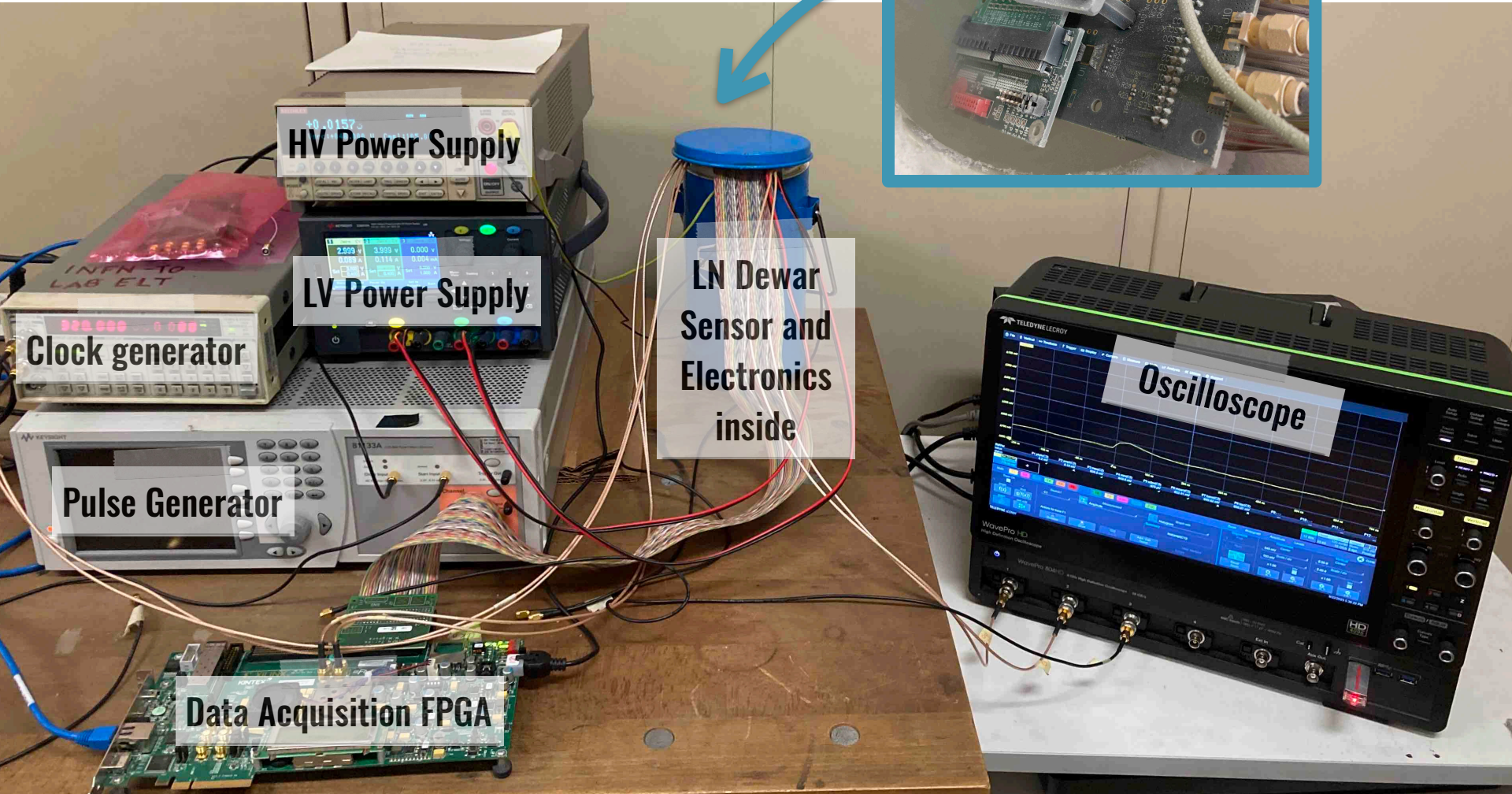
ALCOR FEB (f)



ALCOR FEB (b)



The Cold Test Setup



HV Power Supply

LV Power Supply

Clock generator

Pulse Generator

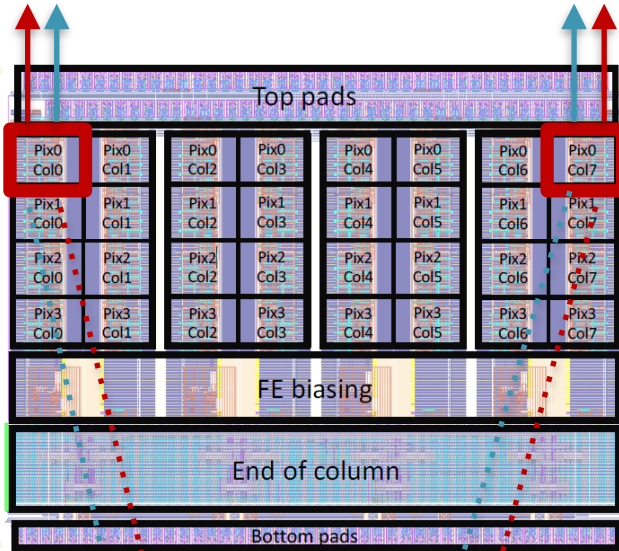
Data Acquisition FPGA

LN Dewar
Sensor and
Electronics
inside

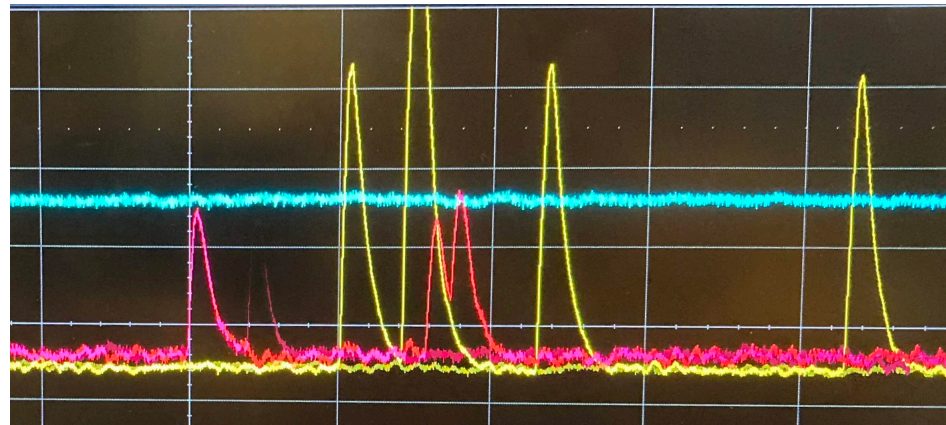
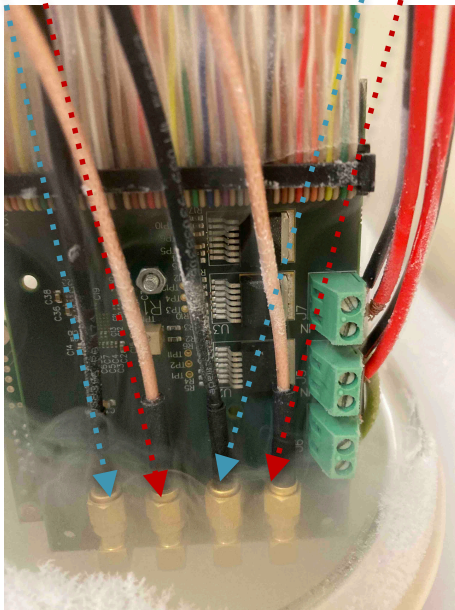
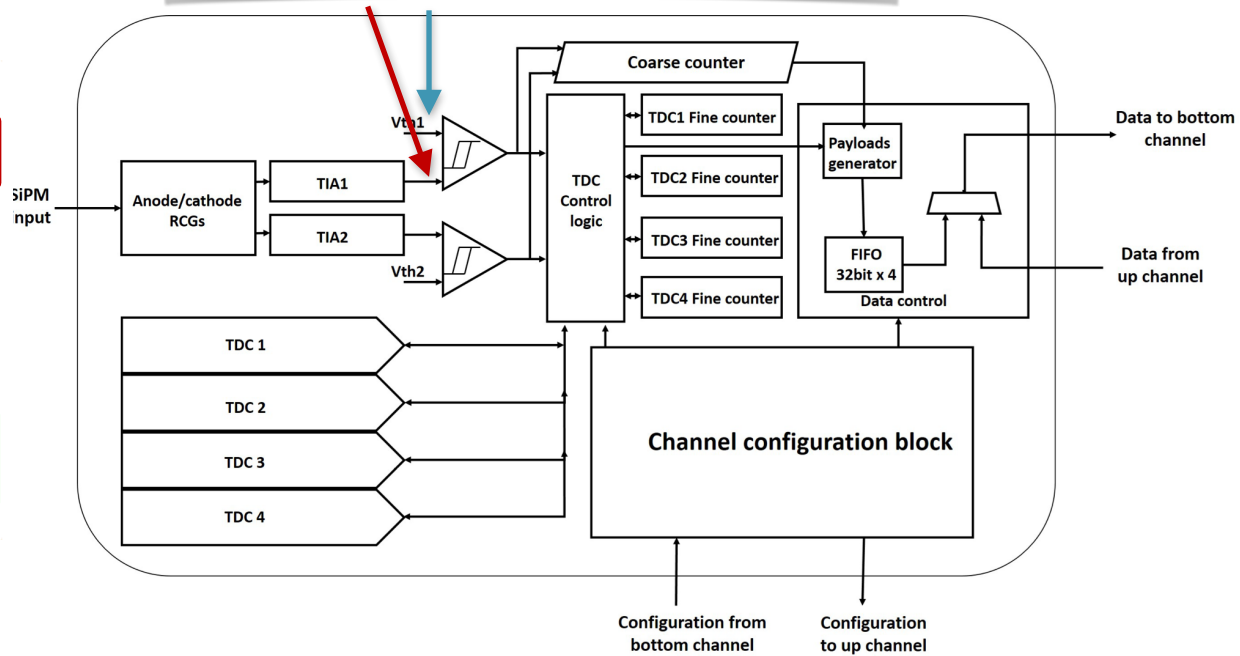
Oscilloscope

ALCOR ASIC

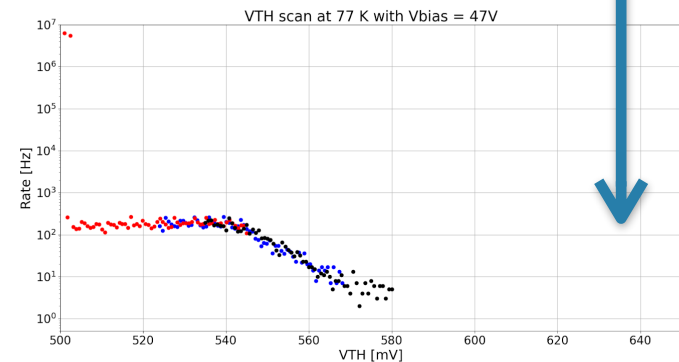
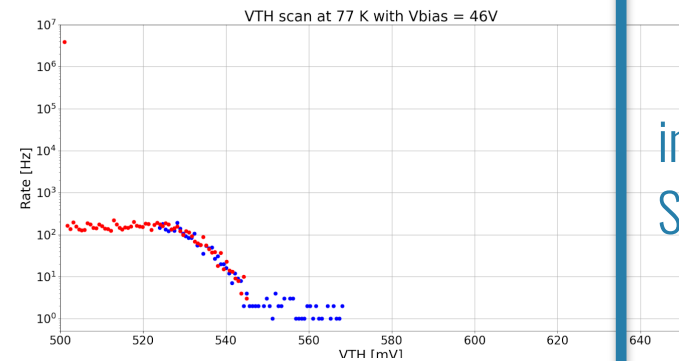
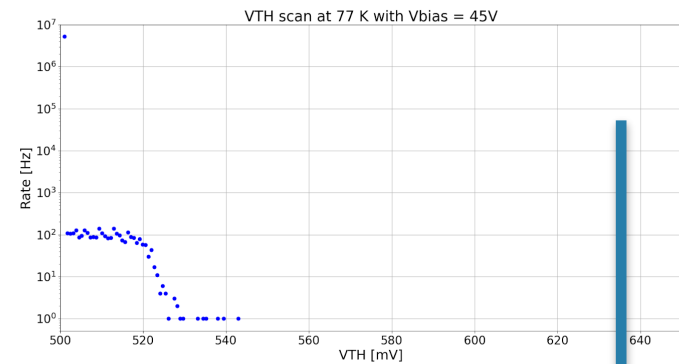
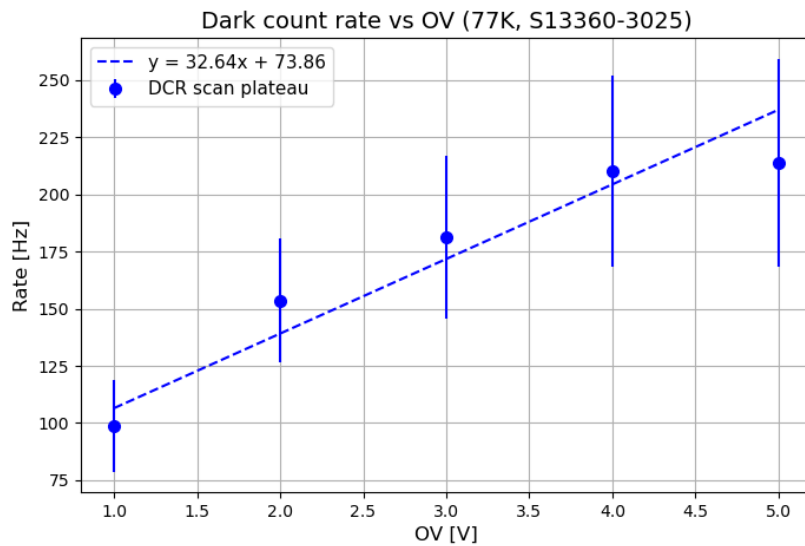
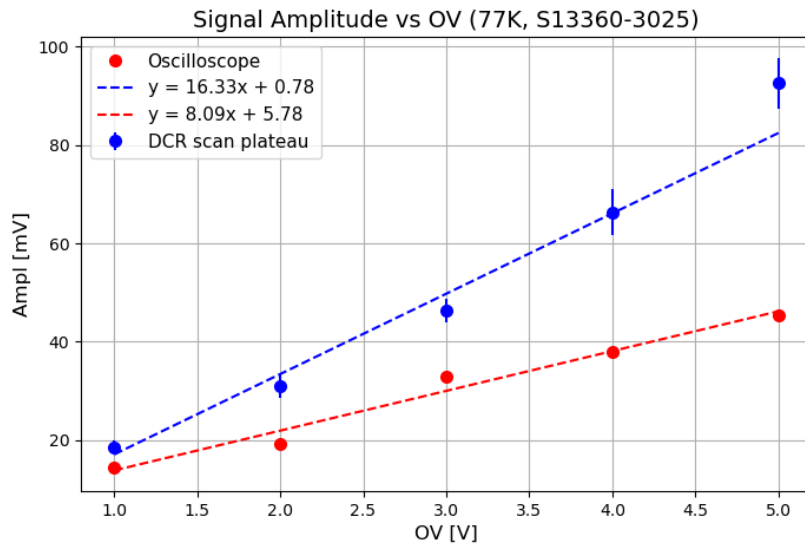
Pixel floorplan and Architecture



Amplifier Output and Threshold voltage are available as debug outputs for Pixel 0 and Pixel 28



Dark Count Rate (DCR) and signal amplitude studies at 77K



increasing
SiPM bias

London Low Temperature Laboratory at RHUL

- Setting up operations down to ULT at London Low Temperature Laboratory - cryostats reaching 100 microKelvin
- first ASIC operations at 1K expected soon. Currently using available setups for measurements at 4K (e.g. Darkside-20K VETO readout ASIC shown before)

London Low Temperature Laboratory



- The Low Temperature Laboratory at RHUL was founded in 1986 as part of a reorganisation of the University of London, with a purpose-built laboratory space of 130 m². The facilities have expanded over the years with a diversification of its activities.
- The facilities of LLTL include four microkelvin platforms, with distinctive sample environments, with additional dilution refrigerators for millikelvin physics. It is supported by a helium liquefier, mechanical and electrical workshops.

London Low Temperature Laboratory

Research at the frontier near absolute zero.
Quantum Technologies and Quantum Materials.

The infrastructure of the London Low Temperature Laboratory (LLTL) supports research on Quantum Science and Technology into the microkelvin regime. It is a founder member and access-giving site of the European Microkelvin Platform (EMP), which is funded as a European Advanced Infrastructure.

Main research objectives are currently:

- Topological superconductivity/superfluidity.
- Advancing measurement capabilities with quantum sensors.
- Cryogen-free microkelvin platforms.
- Cavity optomechanics with superfluid ⁴He.
- Realizing high entangled states of quantum matter:
 - supersolid; quantum spin liquid.
- Quantum technology for fundamental physics.



The London Low Temperature Laboratory is an access facility of the European Microkelvin Platform



Semiconductors at Cryogenic Temperatures

A. K. JONSCHER

1964

Andrzej Karol Jonscher was a Polish-British physicist at Chelsea College and, in 1987, became Emeritus Professor at the Royal Holloway, University of London.

An outlook to the development and use of cryogenic CMOS electronics for particle physics

- ❖ CMOS Process Design Kits typically valid down to 233K (-40°C), although [models scale relatively well down to 77K](#). This was verified with VDSM bulk and FDSOI technology nodes.
- ❖ [Cryo-CMOS PDKs](#) are fundamental for the development of complex mixed-signal cryo-ASICs allowing for innovative detector architecture and concepts, data transfer, readout and control.
- ❖ Future R&D on electronics for HEP exploring low temperature effects will certainly require infrastructures for [device parameter extraction and modelling](#) and development of cryo-PDKs.
- ❖ The [sweet spot around LN boiling temperature](#) (where we get the best of the MOSFET characteristics with still no saturation effects) opens promising prospects on the development of innovative readout concepts both for [neutrino and dark matter detectors with noble liquids](#) and, in general, for charged particle and photon [detectors operating at 77K](#).
- ❖ The growing interest on the use of CMOS for Quantum Computing and Quantum Sensing ~~could~~ shall open new opportunities for [collaborative efforts with selected silicon foundries and CAD/EDA houses](#) on the PDK development and optimisation of CMOS sensors and processes for operation at cryogenic temperatures.

Fundamental contributions from several people

Davide Braga at Fermilab (US)

Dennis Nielinger and Patrick Vliex at FZJ (DE)

Edoardo Charbon at EPFL (CH)

Tetsuichi Kishishita at KEK (JP)



Manuel Rolo (INFN)

Thank you for your time!