A test bench for the qualification of the GRAiNITA prototype

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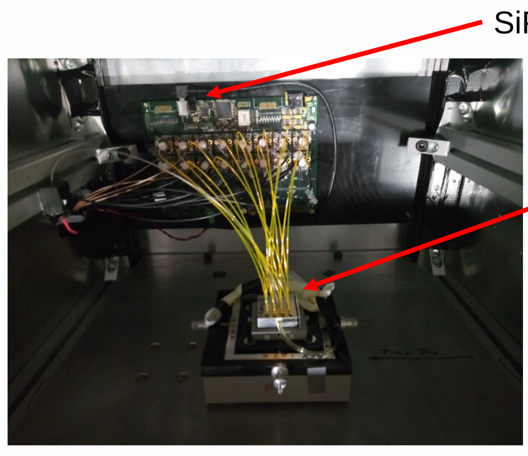
Abstract

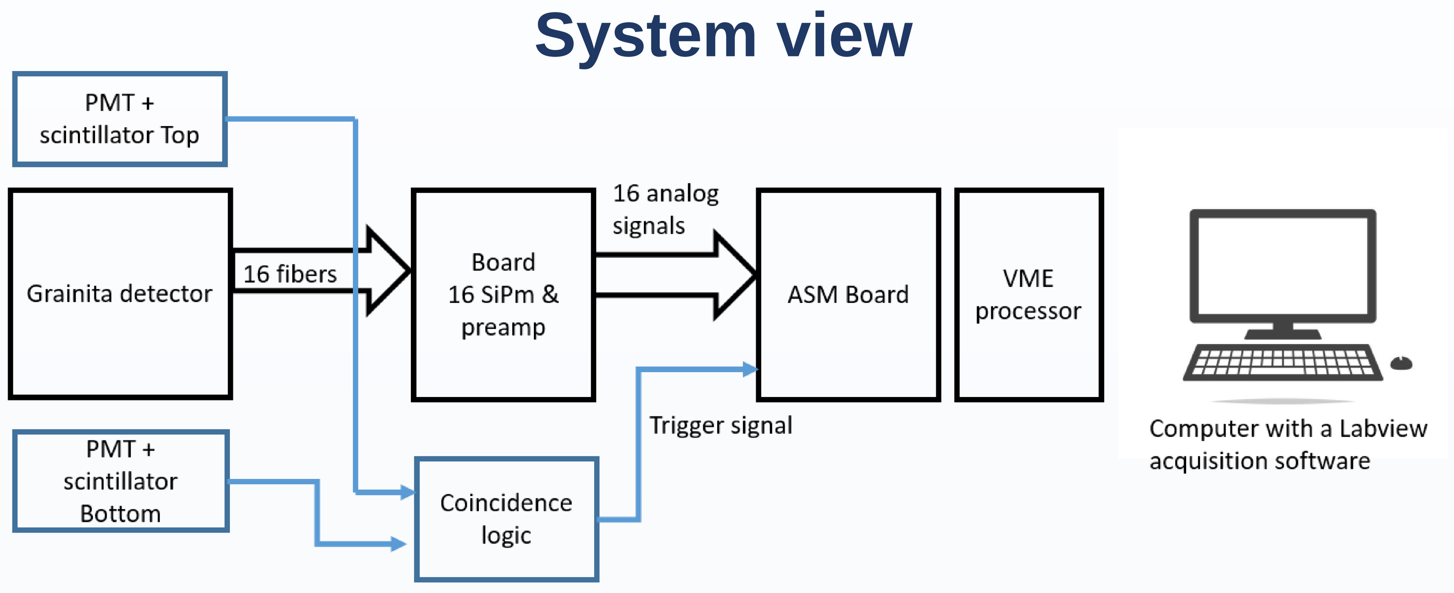
The GRAiNITA prototype has been developed as a first step toward the development of a next-generation calorimeter for FCC-ee. To evaluate GRAiNITA performance, a special test bench was built. The principle consists in tracking the particles that pass through the prototype to check the response of the prototype as a function of the region traversed. Wavelength-shifting fibres capture the light emitted when particles travel through the crystal and transmit it to silicon photomultiplier (SiPM) detectors. A fast acquisition system is used to count the individual photoelectron(PE). An off-line analysis allows one to correlate the tracks with the deposited energy.

The main topic of this poster is the processing of SiPM signals by timestamping each individual scintillation photon. The proposed test bench is capable of handling 16 channels in parallel.

The results of this analysis will be used to test and possibly implement a pulse shape discrimination in the next version of the prototype.

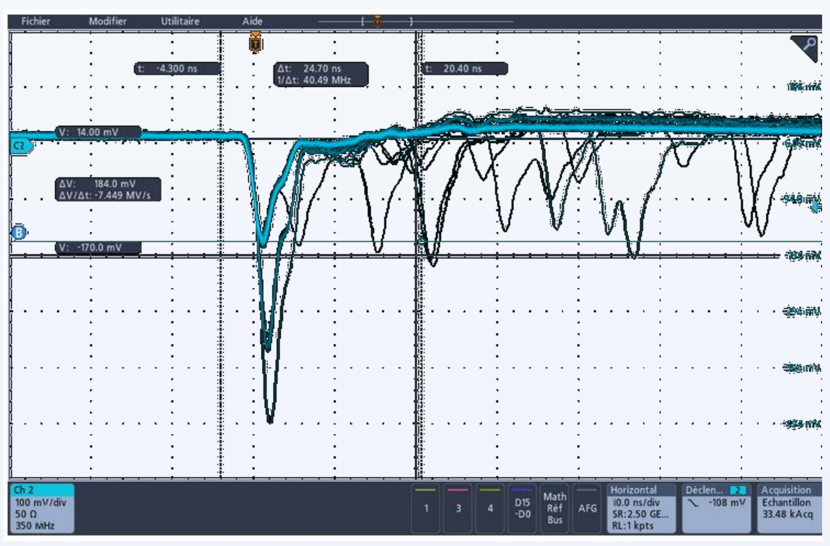


System view



1. Light is generated by the interaction of incoming particles with the GRAiNITA prototype. It is a box of 2.8 x 2.8 x 6 cm, containing 180 g of $ZnWO_4$.
2. Light is converted to an analog signal by SiPMs and is shaped by a first stage of preamplifiers.
3. The analog to digital conversion is performed by the DRS4 chip and has two processing paths :
   - 2 comparators/channels
   - A capacitive array associated with an ADC
4. The digital processing is done in a dedicated FPGA.
5. Acquisition is based on a VME bus and a Labview software.

Signal to be processed



Input signal :One Photon-Electron gives, after the pre-amplifiers, a 8 ns pulse with a 170 mV amplitude.

The scintillation of $ZnWO_4$ in response to the passage of an electron of 1 GeV gives thousands of PE. The decay of the signal follows exponential laws with several times constants. For example, $ZnWO_4$ has at least 3 components in the µs range (25 µs, 4.4 µs and 0.4 µs). Their precise determination is the aim of this project as their relative ratio are expected to change with the particle type.

If the case of the test of faster scintillating times like BGO we used the integration method and a fast sampling by the DRS4 in this board.

The electronics design

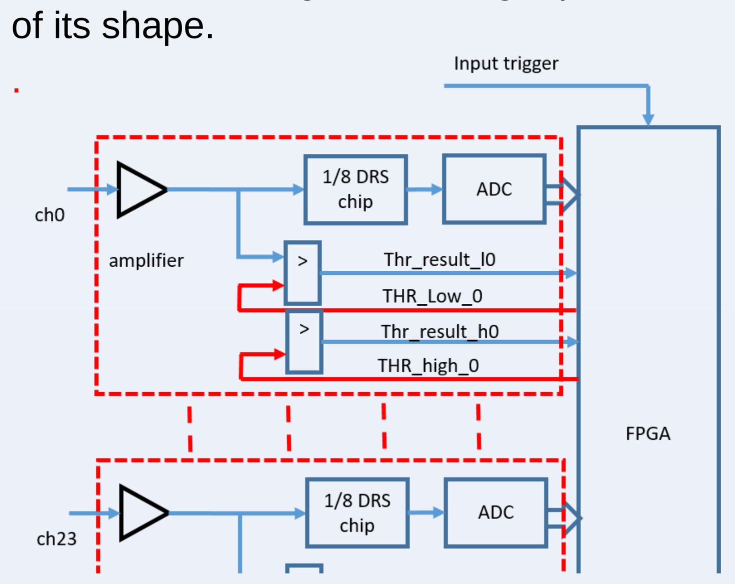
The ASM board, which has been designed for a medical application experiment, is used to digitize and process the input signals. It has been modified to cope with the constrains of the test bench.

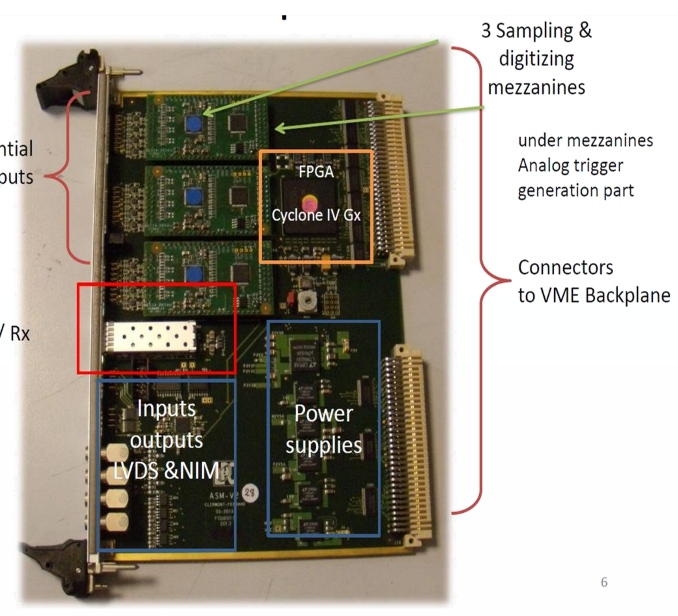
It is a homemade design based on a FPGA (Altera Cyclone 4 GX) for the digital processing associated with 4 DRS4 ASICs (designed by PSI). It allows to sample up to 24 channels at 4 GHz. The data is stored in a 1024 capacitor array and the converted to digital by 12 bits ADCs. The board use the standard VME format. The data is sent to the acquisition PC with the VME 64 block transfer.

The board houses 2 comparators per input channels. Each threshold level can be individually configured by a 12 bit DAC controlled by the LabVIEW software.

These comparators allows to count individual photons and timestamp them which a 4.1 ns precision. The threshold level is determined by performing a threshold scan. This step is automatically done by the software.

In the meanwhile, the DRS4 acquire the first 1 us of the signal allowing a precise study of its shape.

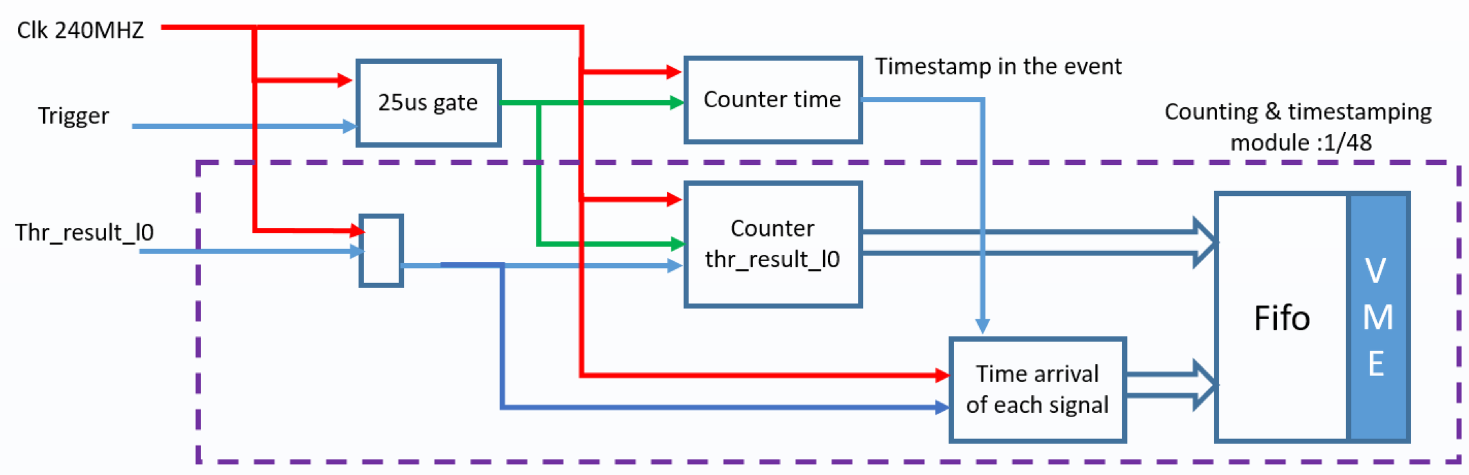




ASM Specifications		
	Number of channels	24
DRS4	Sampling frequency	1GHZ to 4GHz
	Dynamic range	600 mV
	Sampling depth	1024 samples
ADC	Number of bits	12 bits
	Sampling Rate (Per Second)	40 MHz
comparators	2 by channel	48 in total
	Number of bits	12 bits
DAC	lsb	0,8 mV

Firmware implementation

The trigger is generated by the coincidence between two external scintillators in order to be able to select particles which cross the GRAiNITA prototype. Its logic is based on NIM elements.



The reception of the trigger starts a 25 µs gate in which all the PE time-of-arrivals are recorded :
- The gate and the counter use a 240 MHz clock (4.16 ns resolution)
- Timestamps are stored with the PE number in a 5k event FIFO
- This module is implemented for each of the 48 comparators (24 channels x 2)
- Data is sent to the acquisition PC using the VME bus
- The trigger timestamp and tagging allows to synchronise the events of the full acquisition system

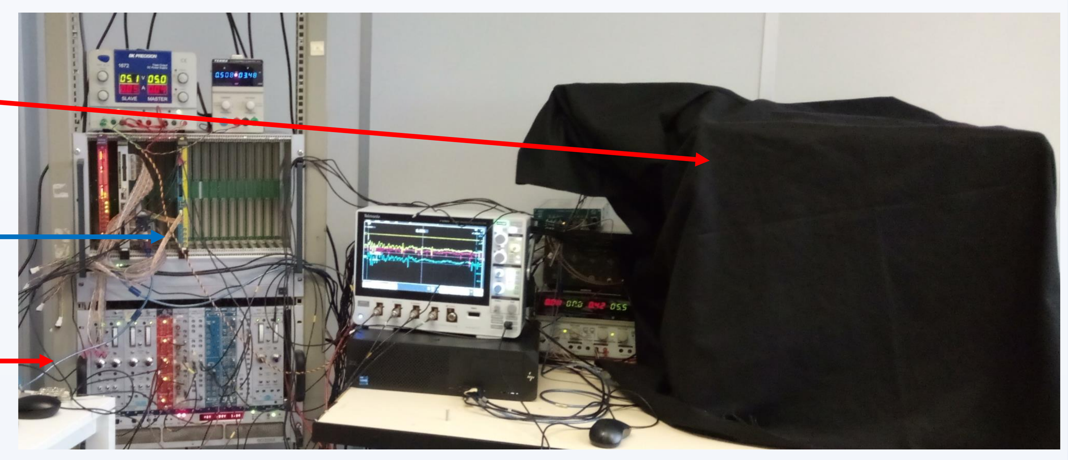
First result

Test bench

Black box housing Granita prototype

VME crate with the ASM board and the processor board

NIME crate for trigger logic



The system has been validated using a LED pulser connected to the SiPMs. It allows to send a 25µs signal in order to emulate the scintillation light emitted by the prototype. The processing has been checked by connecting an oscilloscope in parallel to the ASM boards.

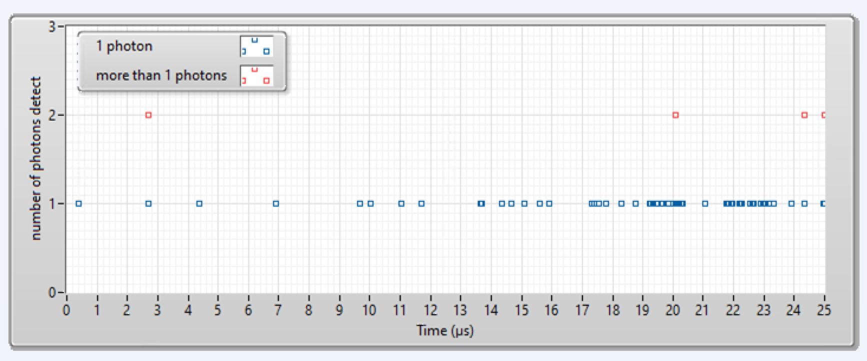
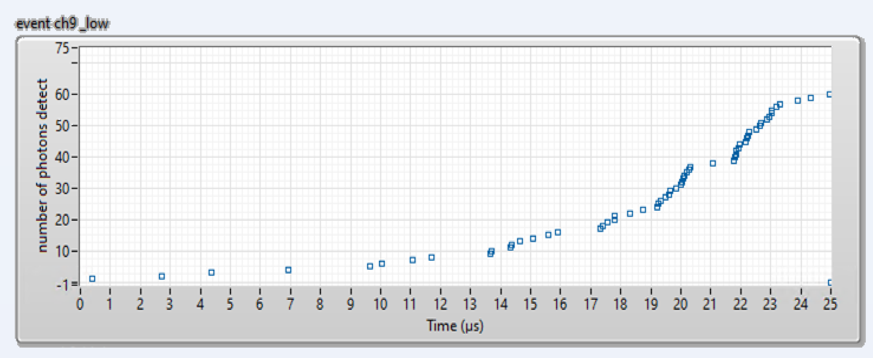


Figure 1 : PE time-of arrival recorded on one channel for both comparators. One has been set at the 1 PE level (blue) and the second one at the 2 PE level to detect pile-ups (red).

Figure 2 : Cumulative plot of the number of detected PE versus the time-of-arrival.



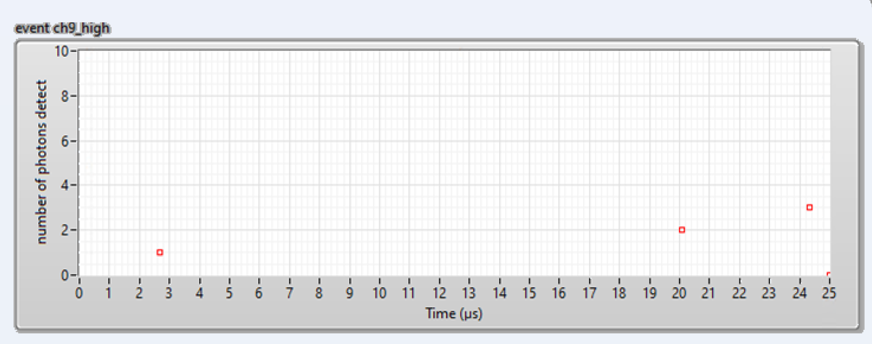


Figure 3 : Cumulative plot counting the number of pile-up event (comparator 2 triggered)

Next Steps and Conclusion

We designed a test bench able to precisely determine the timing of each scintillation photon generated by a crystal. It is based on the ASM board and the DRS4 ASIC. Its performance has been checked using a LED pulser and an oscilloscope.

The next step is to test the GRAiNITA prototype with this system. A first step will use cosmic muons before moving to radioactive sources. A test beam is foreseen this autumn.

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