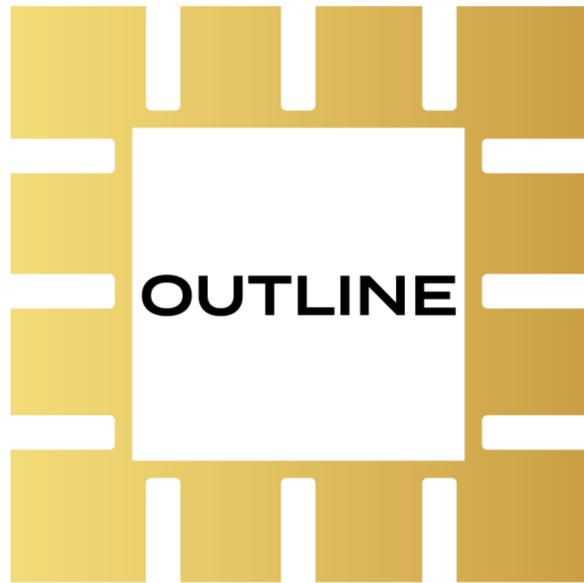
# Optimizing ESD Protection for Thin-Oxide Transistors in the Latest Semiconductor Processes

TWEPP – October 2024

Wouter Faelens, Sofics




- Introduction
  - Electrostatic Discharge
  - Impact for IC industry
- Advanced CMOS / FinFET nodes
- Local clamp approach
- Conclusions

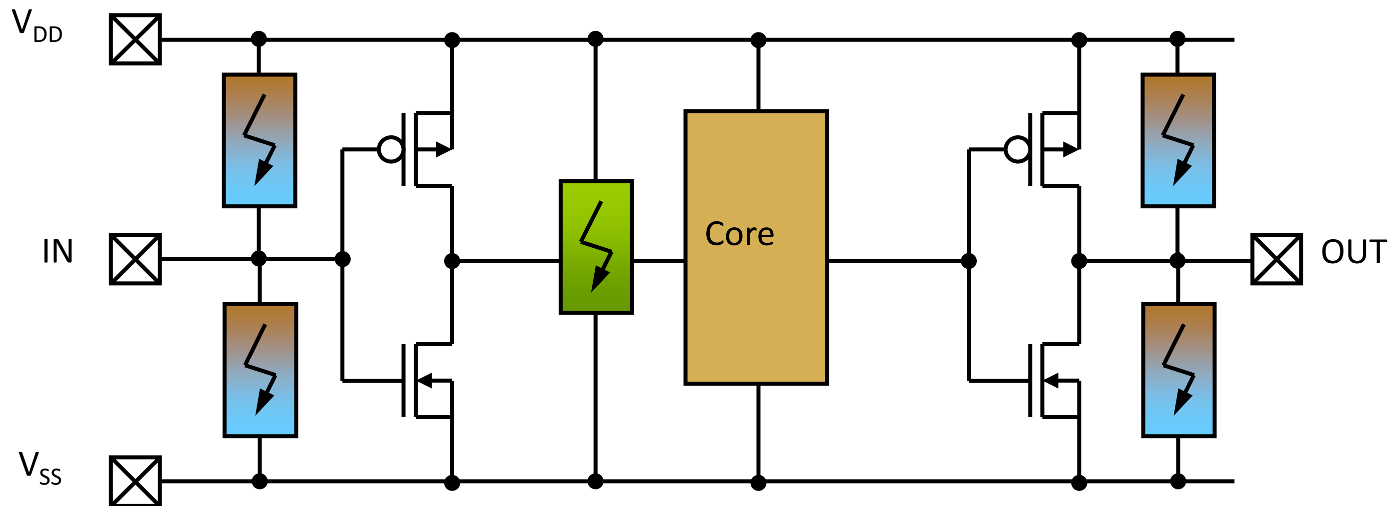
# What is ElectroStatic Discharge (ESD)

- What is Electrostatic Discharge (‘ESD’)?
  - The sudden discharge of a charged body
    - Short time (<1us)
    - Short rise time (<10ns)
    - High current levels (1-10A)
      - and beyond...
  - Tribo-electric and induced charging
- Damages caused by
  - Charged human
  - Charged machinery/robotic
  - Charged IC’s

| Description | Typical voltage (V) |
|---|---|
| Person walking over carpet | 15.000 |
| Person working at a table | 800 |
| Circuits after removing protective foil | 20.000 |

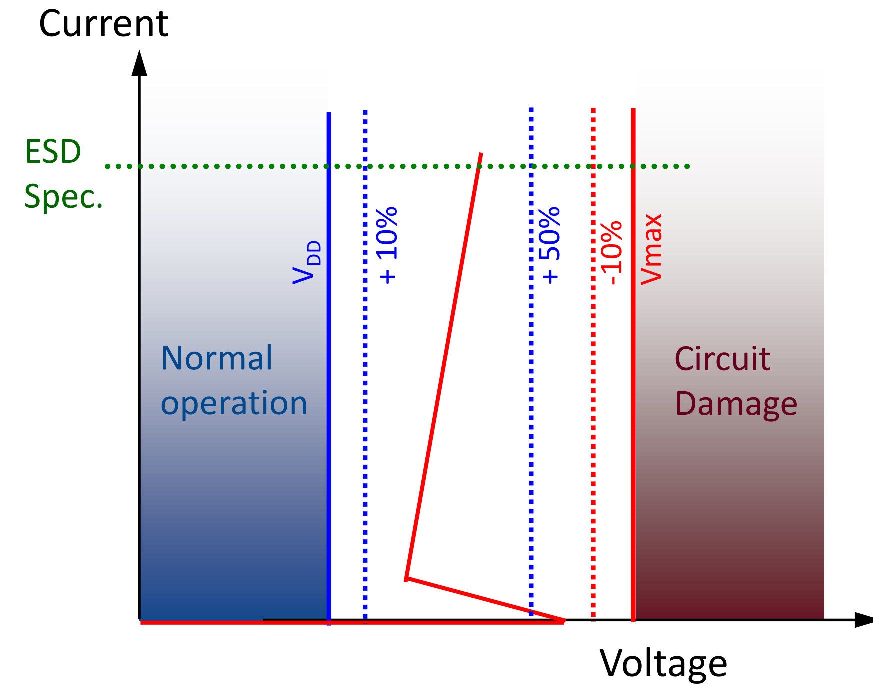
# Solution: on-chip ESD protection

- On-chip ESD protection
  - ESD clamp/diode devices at IO interfaces, power pads
  - Different concepts are used in the industry



# Solution: Design window

- Requirements for ESD protection switches
  - Protecting during ESD
    - **Effective** clamping voltage to safe value
    - $V_{max}$ defined by sensitive element:
      - Core
      - GOX
      - MOS devices
  - Minimal impact on circuit performance
    - Leakage
    - Capacitance



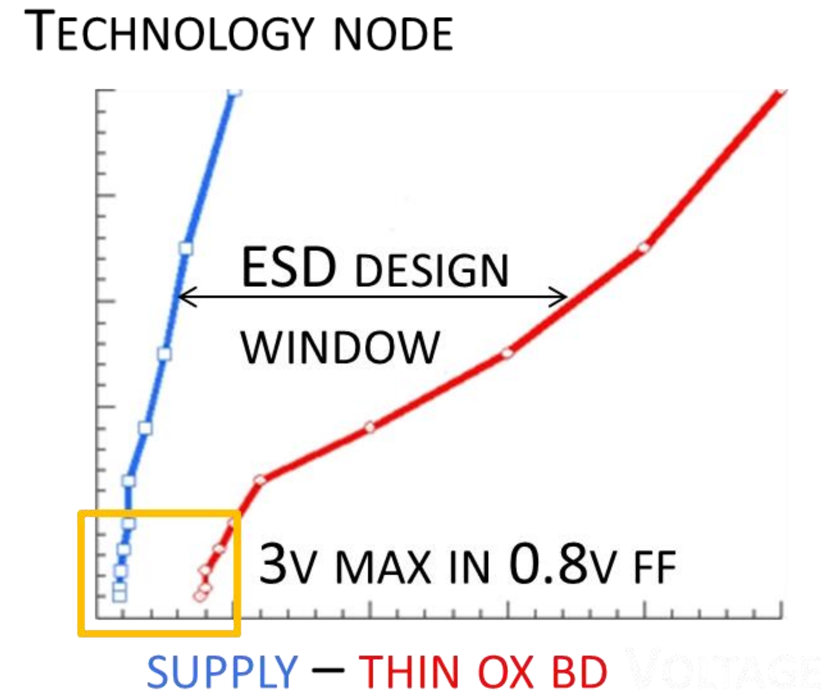
- Introduction
- **Advanced CMOS / FinFET nodes**
  - **Sensitive circuits**
  - Design complexity
  - Cost
  - CDM
  - Traditional ESD approach no longer effective
- Local clamp approach
- Conclusions

# Challenges for on-chip ESD protection for advanced nodes

- Many challenges for advanced CMOS and FinFET designs
  - Advanced circuits **fail easily** under ESD stress – smaller ESD design window
  - **Traditional ESD solutions** are **no longer effective**
  - Increased **design complexity**
  - **Cost of failure** is very high
  - **CDM challenge** for large size SoC's
  - ESD complexity rising with many different IP sources

# ESD Design Margin evaporates for advanced CMOS

- Drastic reduction in failure voltage
  - Transient breakdown of gate oxides
  - Burn-out of output drivers
  - Core failure voltage
- 16nm FinFET – core transistor
  - Vmax 25% lower compared to 28nm
  - Vmax 33% lower compared to 90nm
- 7nm FinFET – core transistor
  - Vmax 35% lower compared to 28nm
  - Vmax 57% lower compared to 90nm



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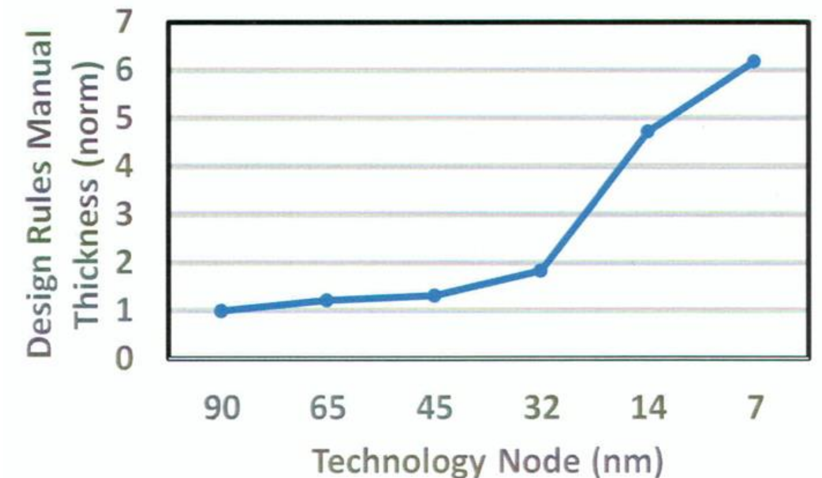
# Increased design complexity

- FinFET design complexity
  - Number of design rules increased drastically
  - Complexity of the rules increased
  - Mentor Graphics:
    - "Required processing power for verification doubled compared to 28nm"
  - Design time increased a lot

**Sofics experience**

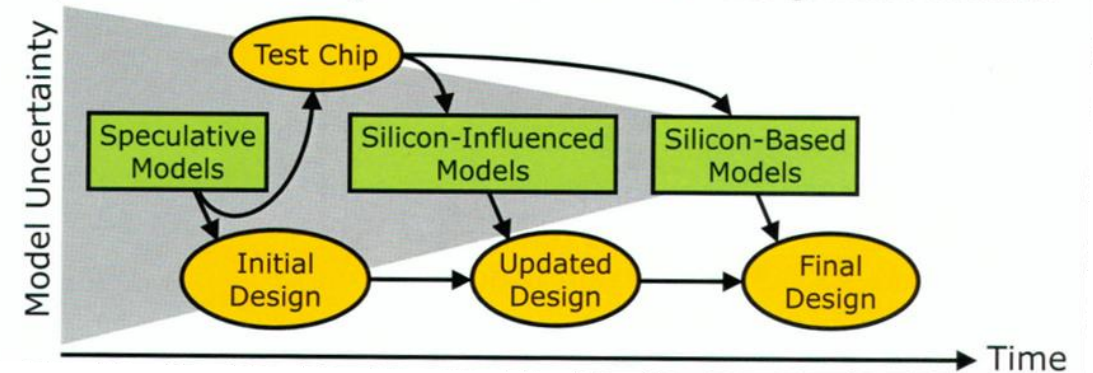
| Design time | 28nm | 16nm |
|---|---|---|
| Optimized ESD | 1 day | 2 weeks |

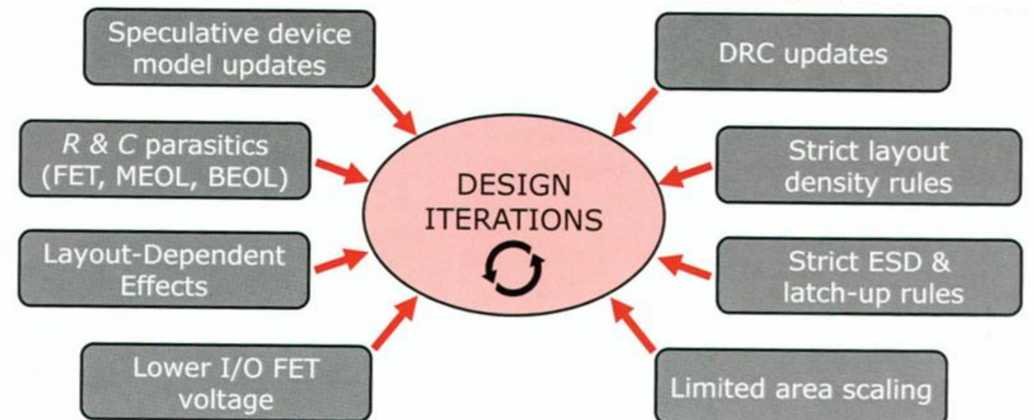



Jonathan E. Proesel,
IBM T.J. Watson Research center
@ ISSCC 2020

# Increased design complexity

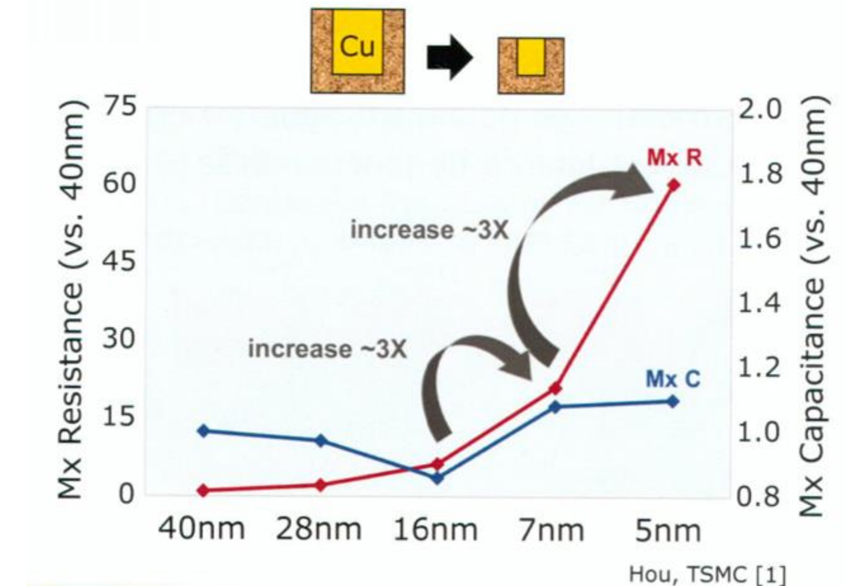
- TSMC @ ISSCC 2020
  - Uncertainty at design stage
    - “Process at tape out ever more immature in each new node”
    - “Design concurrently developed with technology to shorten time to market”
  - Pre/post layout simulation gaps
    - “Accept **more iterations** in each new node”
  - More restrictive layout
    - “1000s of DRCs, many very tough to pass, always getting more restrictive”
    - Density checks



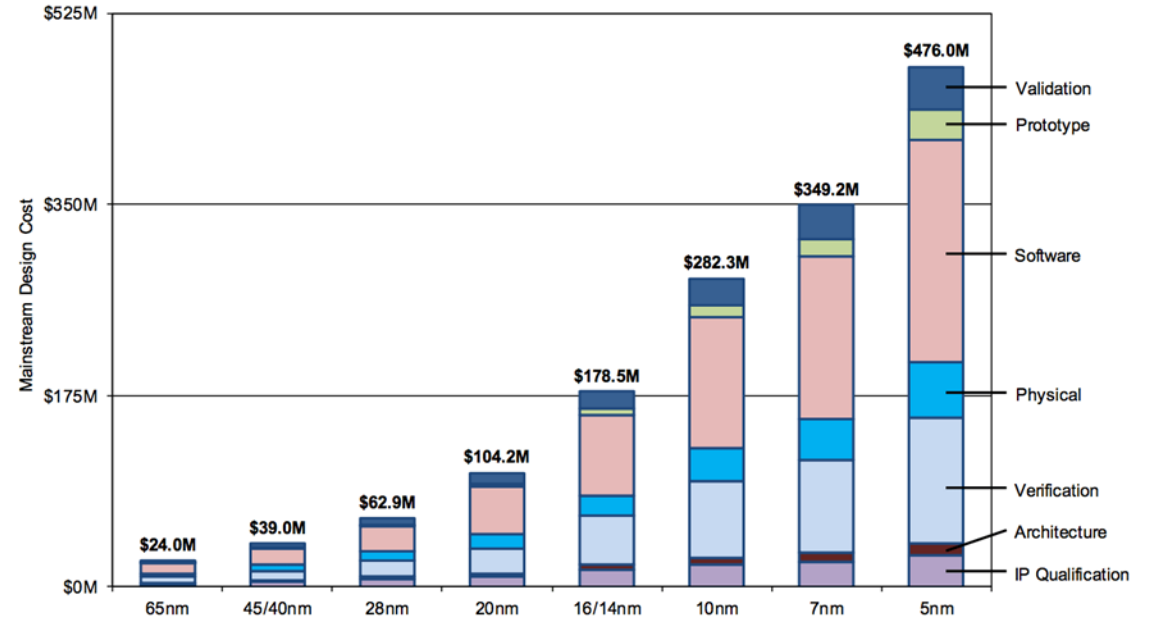
# Increased design complexity - metallization

- RC parasitics of interconnects
  - 2 groups of metallization
    - Local Metals get thinner: R increases!
    - Top metal thickness remains
  - TSMC @ ISSCC 2020
    - “Resistance is arguably THE defining agony of FinFET era design”
    - “Capacitance-only post-layout simulation virtually useless”



# Cost of failure

- IC design is expensive
  - Mask cost rising quickly
    - 'first time right...' requirement
    - Multiple million $ to resolve the problem (new full mask set).



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  - **CDM**
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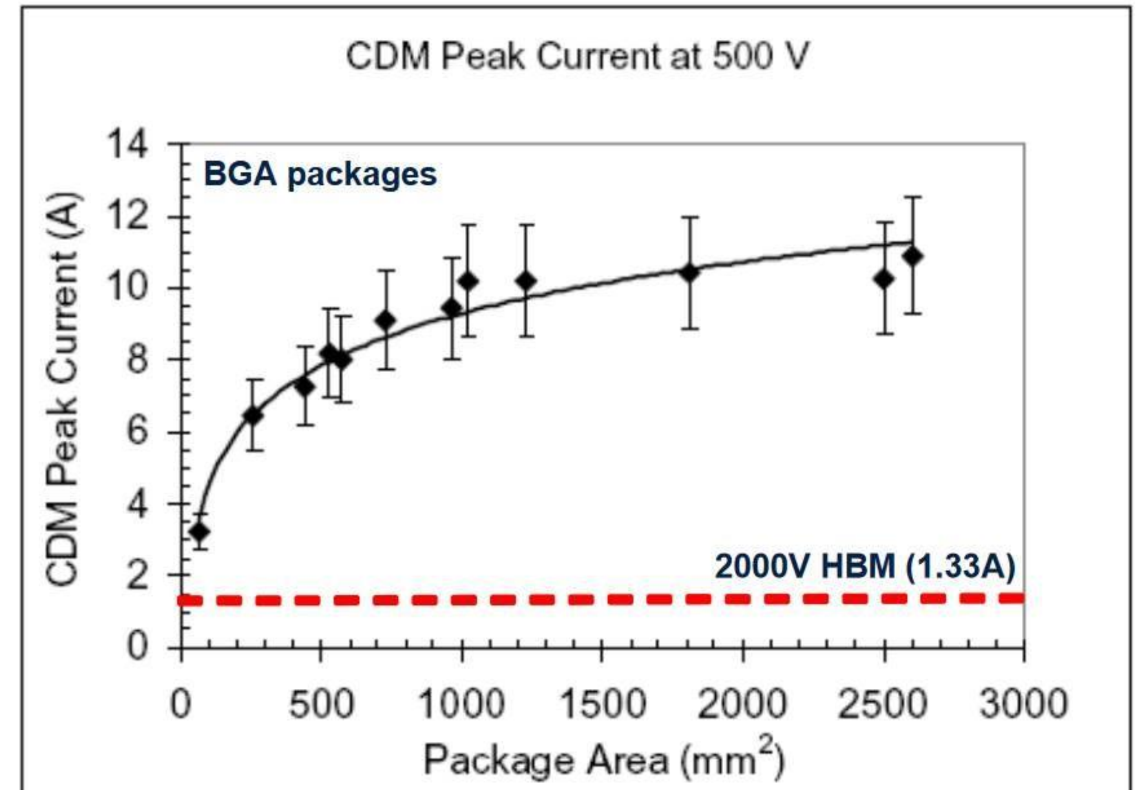
# FinFET SoC's are frequently large, complex chips

- CDM challenge
  - CDM peak current depends on chip/package size
  - Large chip means higher peak current during CDM stress
- Example:
  - ESD solution proven for 4 A peak current
  - Integrated in small (100mm²) chip:
    - pass 500V CDM
  - Same ESD/IO integrated in large chip:
    - Fail 500V CDM
    - Pass 250V CDM



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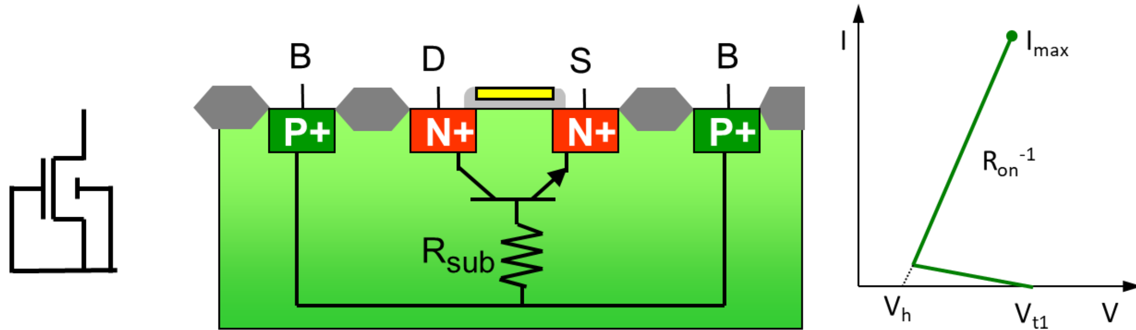
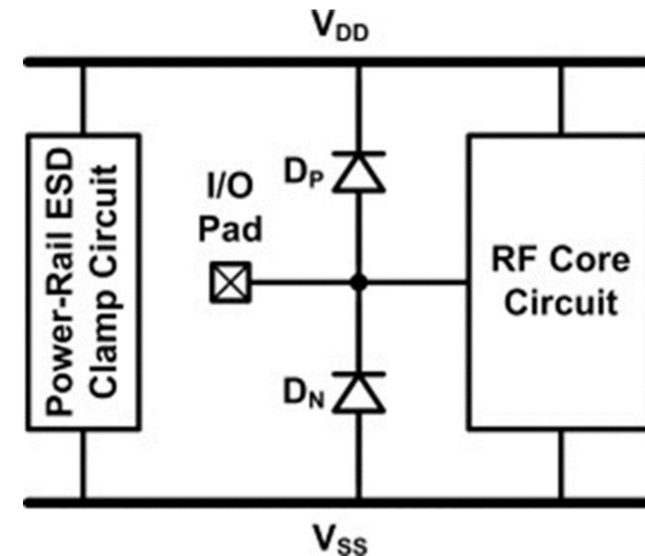
# Traditional I/O ESD solutions

- ggNMOS or self-protective driver
  - Perfect solution in **mature** CMOS
  - Integrated in drivers
  - Diodes integrated

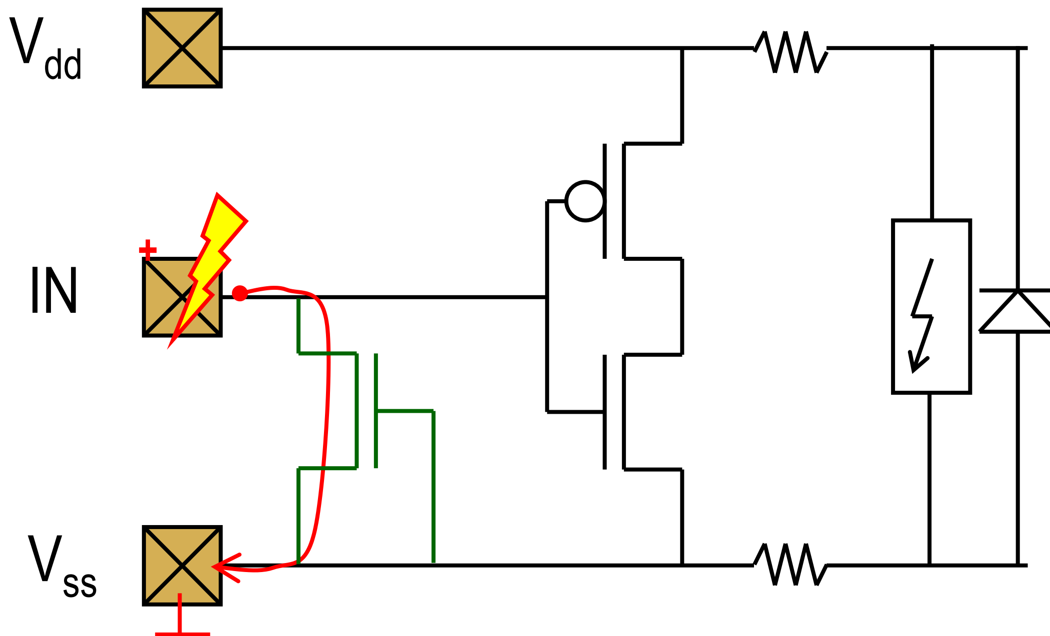


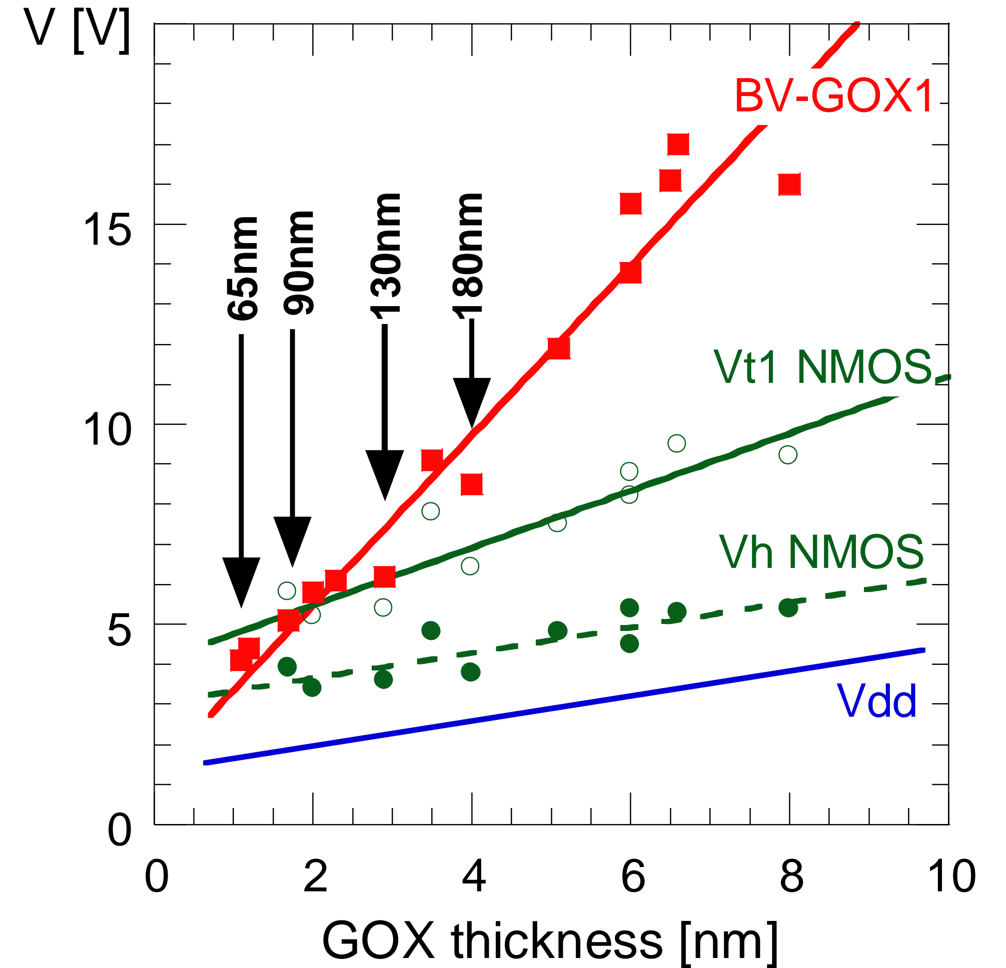

- Diode based I/O protection
  - Simple concept
  - Good characteristics (leak, cap)
  - Small area



# But: ggNMOS clamp cannot protect thin oxide below 65nm

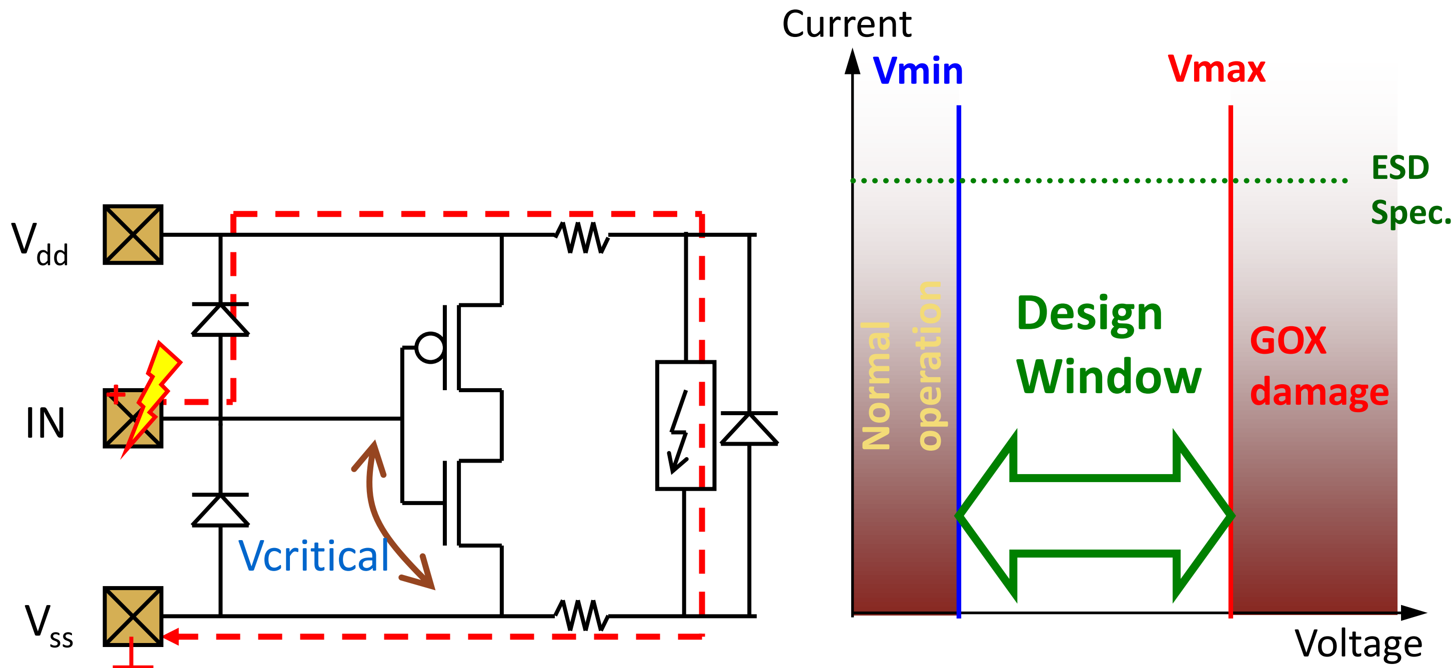
- Technology scaling obsoletes traditional protection approaches

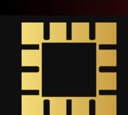


# Dual diode solution

- Protection using diode up and power clamp
  - Voltage drop over diode, bus, Power clamp
  - Requirement: Total voltage drop below Vcritical



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# Dual diode: Influence of bus resistance

- IV curves of all elements in the current path

*Diode*

I

V

*Resistance of Vdd bus line*

I

V

*Power Clamp*

I

V

$V_{dd}$

IN

$V_{ss}$

I

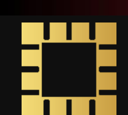
ESD Spec.

GOX damage

Vmin

Vmax

V



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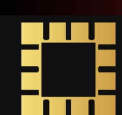

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- IV curves of all elements in the current path

Diode

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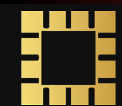

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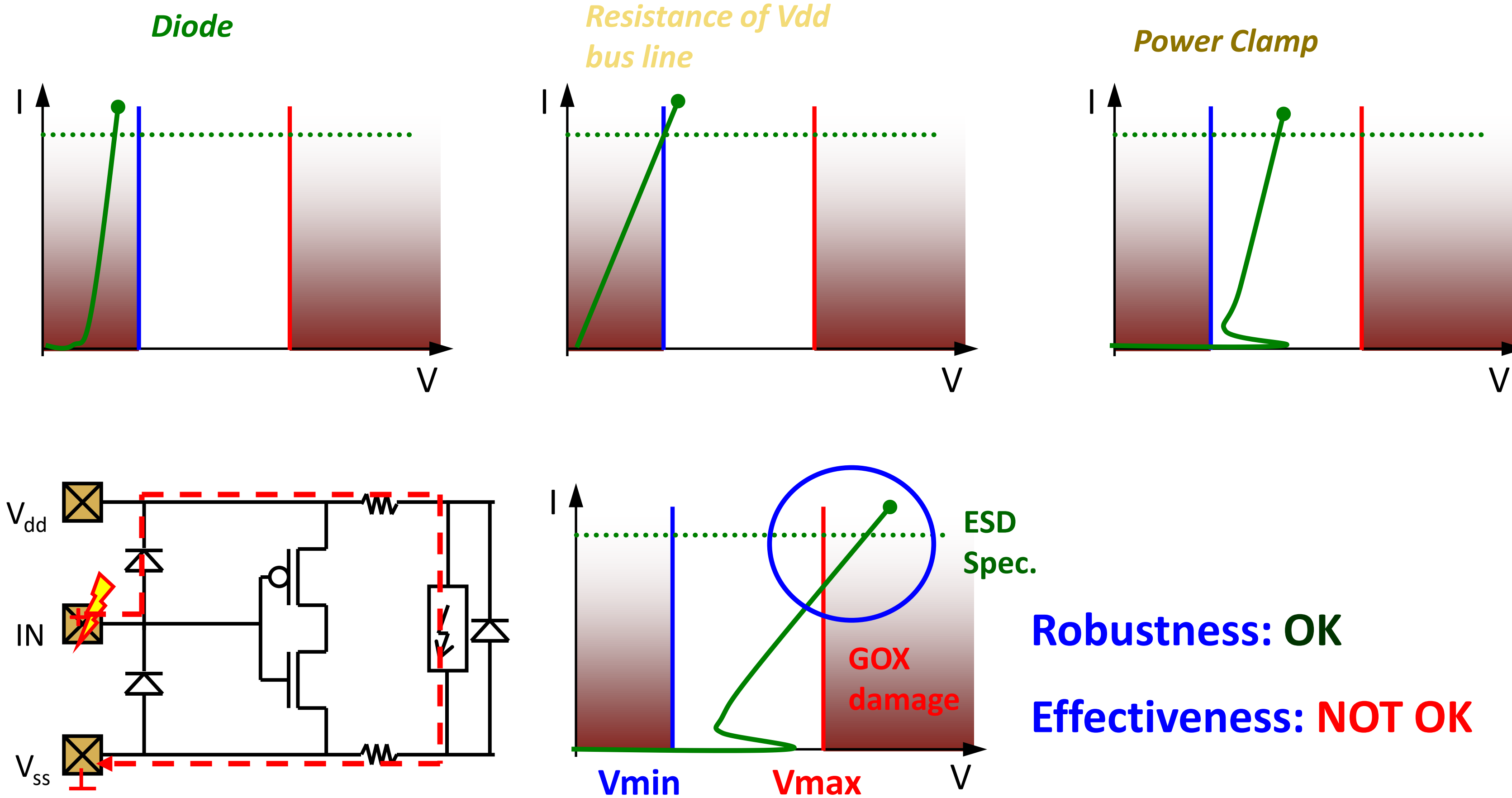
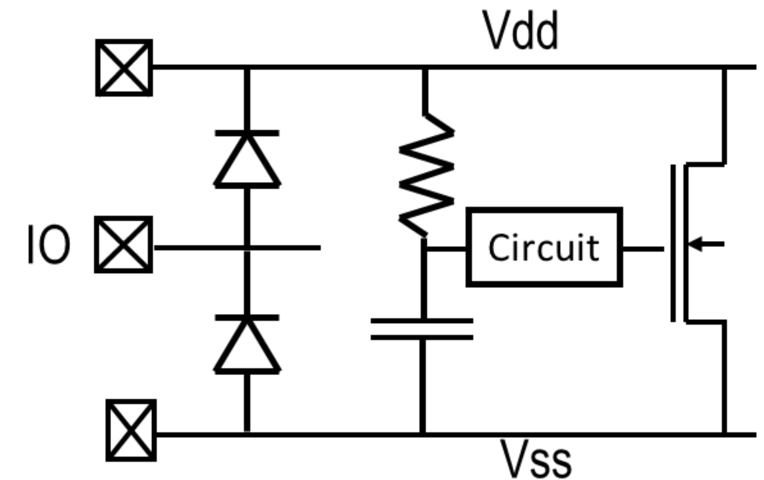
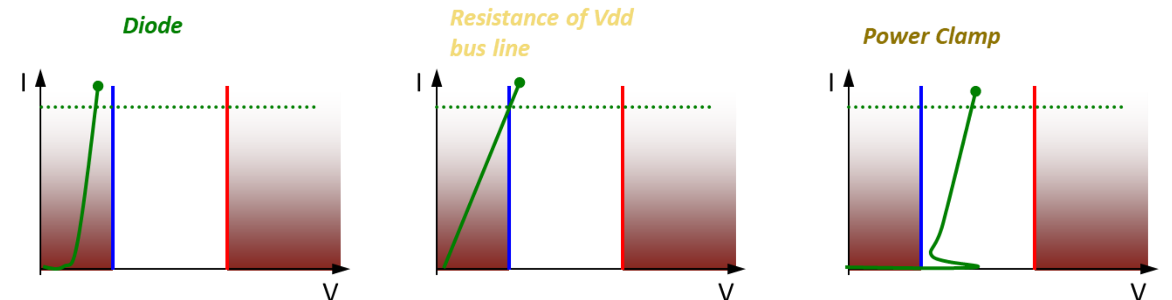


# Traditional diode based approach gets worse too

- ESD performance of diodes reduced
  - 35mA/um up to 65nm
  - 25mA/um in 40nm
  - 20mA/um in 28nm, 16nm
- 'Solution'?
  - Diode scaling required
    - But capacitive loading increases
  - Reduced distance between VDD – IO pads
  - Larger power / rail clamps



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  - **Traditional ESD solutions** are **no longer effective**
  - Increased **design complexity**
  - ESD complexity rising with many different IP sources
  - **Cost of failure** is very high
  - **CDM challenge** for large size SoC's

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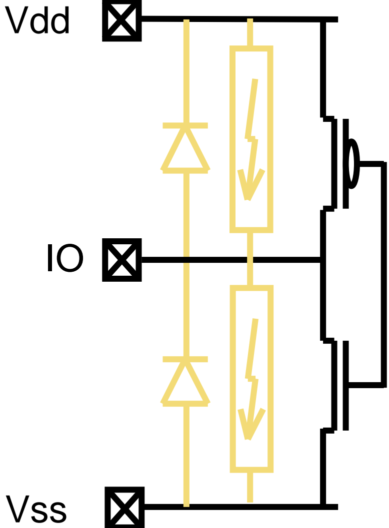
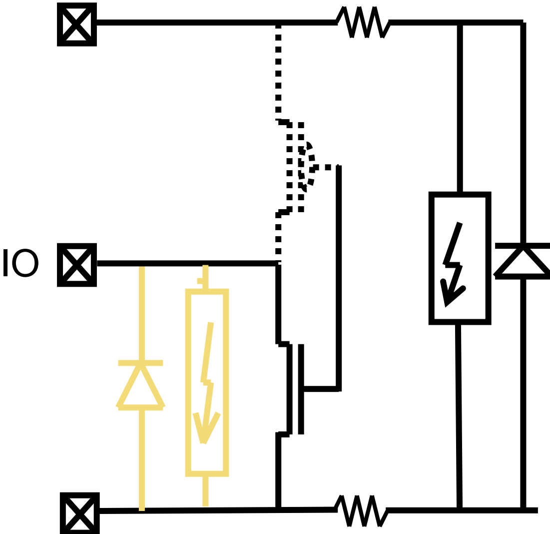
- Introduction
- Advanced CMOS / FinFET nodes
- **Local clamp approach**
  - **Principle**
  - **Examples from Sofics**
    - **Low leakage, capacitance, ESD levels, …**
- Conclusions

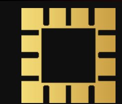
# Local ESD protection at I/O

- Full local protection
  - ☺ Safe local clamping
  - ☺ Bus resistance is NOT critical
  - ☹ Larger area (needed for every I/O pin)
  - ☹ Possibly higher capacitance




- Semi local protection
  - ☺ Safe local clamping
  - ☺ Bus resistance is LESS critical
  - ☺ Open drain circuits
  - ☹ Larger area
  - ☹ Higher capacitance



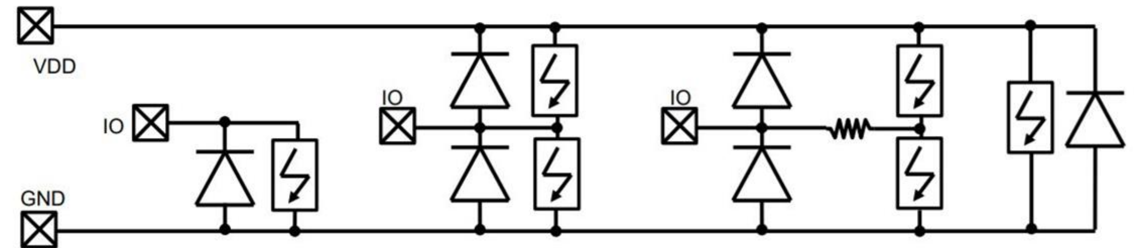



# Decade of cooperation CERN – Sofics

- I/O libraries for 1.2V, 0.9V
- Projects
  - 2013 – TSMC 65nm ESD
  - 2015 – TSMC 130nm ESD
  - 2016 – IBM/GF 130nm ESD
  - 2020 – TSMC 28nm ESD
  - 2021 – TSMC 28nm I/O
- Focus
  - Without thick oxide transistors
  - Low leakage ESD protection cells
  - Small area
  - Over-voltage tolerant option
  - Low capacitance local clamp (<200fF, <130fF options)

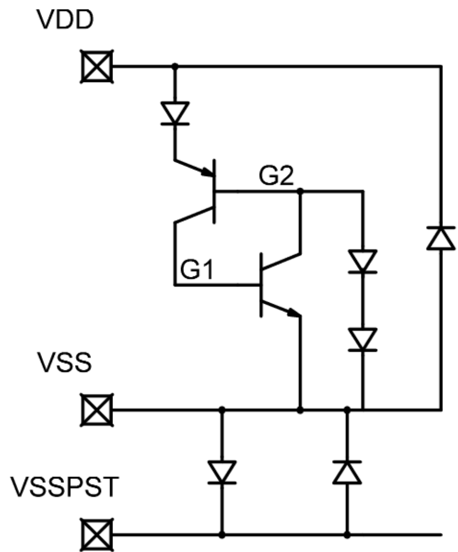
# Decade of cooperation CERN – Sofics

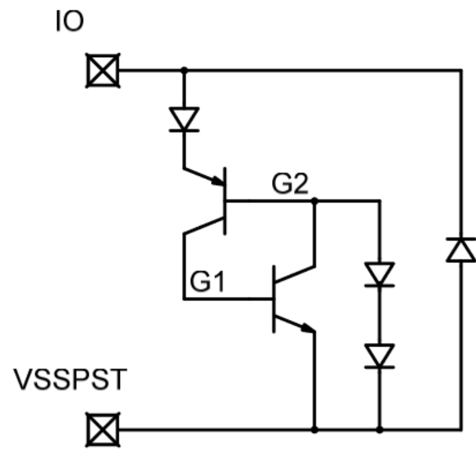
- Library contents
  - 1.2V Power/GND
  - 1.2V Analog I/O versions
    - Full local ESD protection
    - Integrated CDM secondary protection
    - Over-voltage tolerant ESD protection
  - Power cut cell
    - Separate 1.2V / TSMC GPIO sections

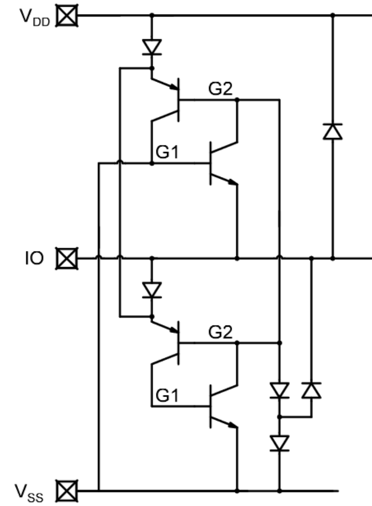


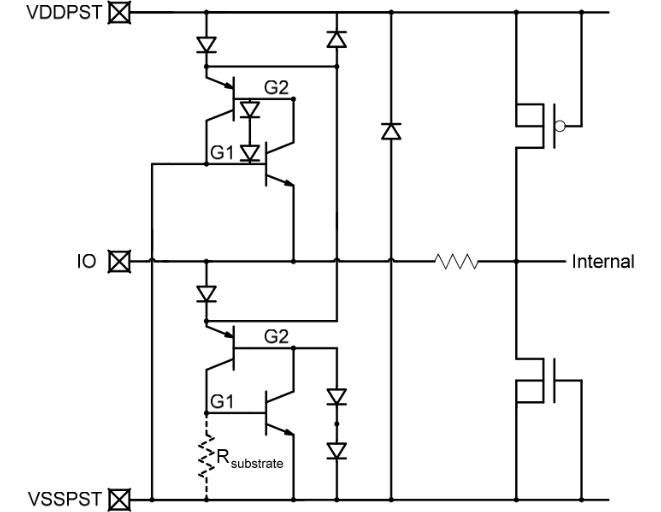
# 1.2V pads

- Power and ground
- Overvoltage tolerant IO
- Full local I/O protection
- Full local I/O protection + CDM



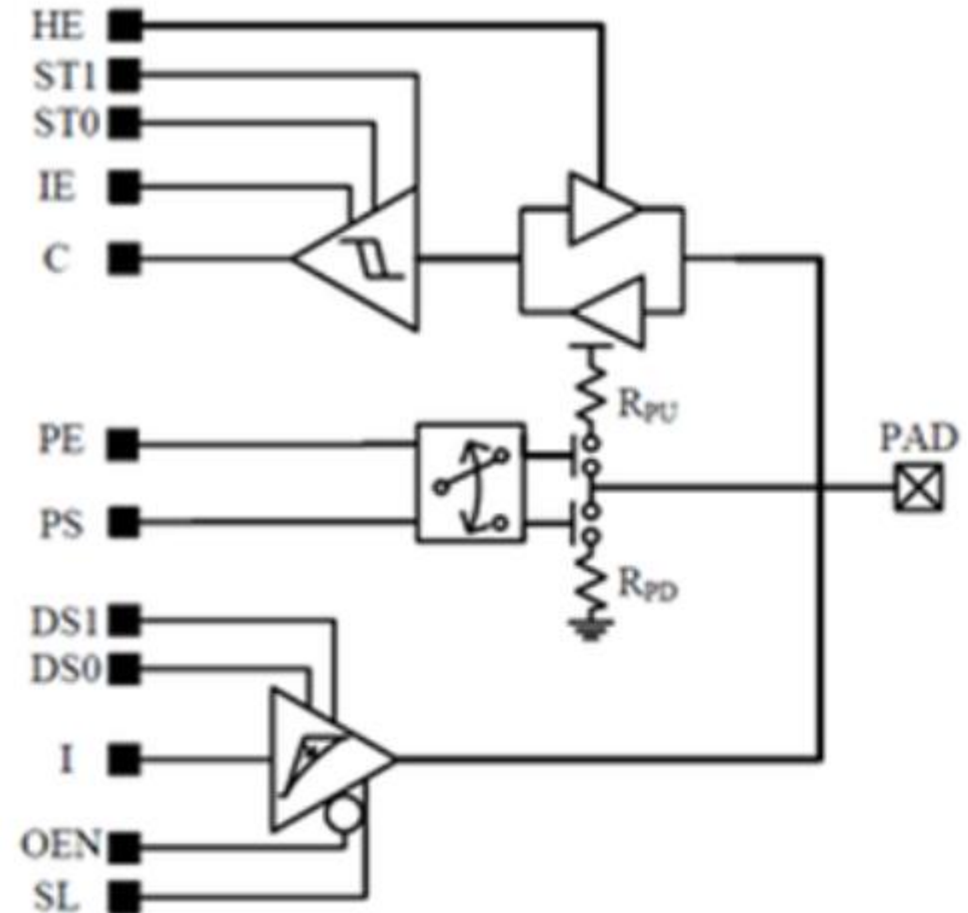



# TSMC 28nm 1.2V I/O based on 0.9V thin oxide devices

- 1.2V GPIO
  - Only thin-gate, 0.9V devices.
- Supported features
  - Programmable drive strength
  - Input/output enable
  - Pull select, pull enable
  - Compatible with TSMC I/O ring
  - Integrated 2kV HBM ESD
  - Bias circuit shared over I/Os

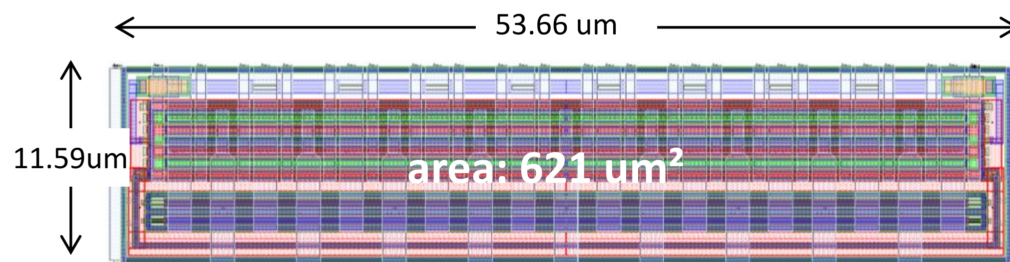


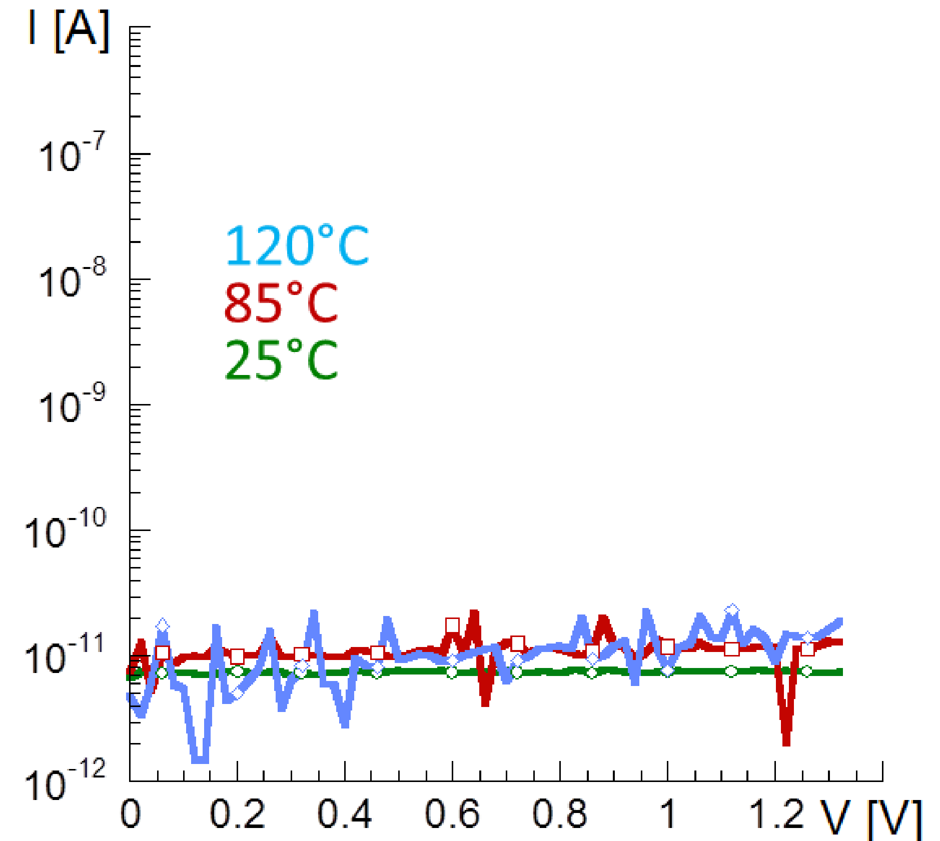
# Local ESD protection: examples

- High-speed I/O
  - <15fF cap
  - TSMC N22
- Ultra low leakage
  - <20pA
  - TSMC N40
- Overvoltage tolerant
  - 1.8V protection without thick oxides
  - TSMC N28
- High ESD robustness
  - 8kV HBM (5.33A ESD current)
  - Smaller footprint
  - TSMC N22

# Analog I/O with ultra-low leakage

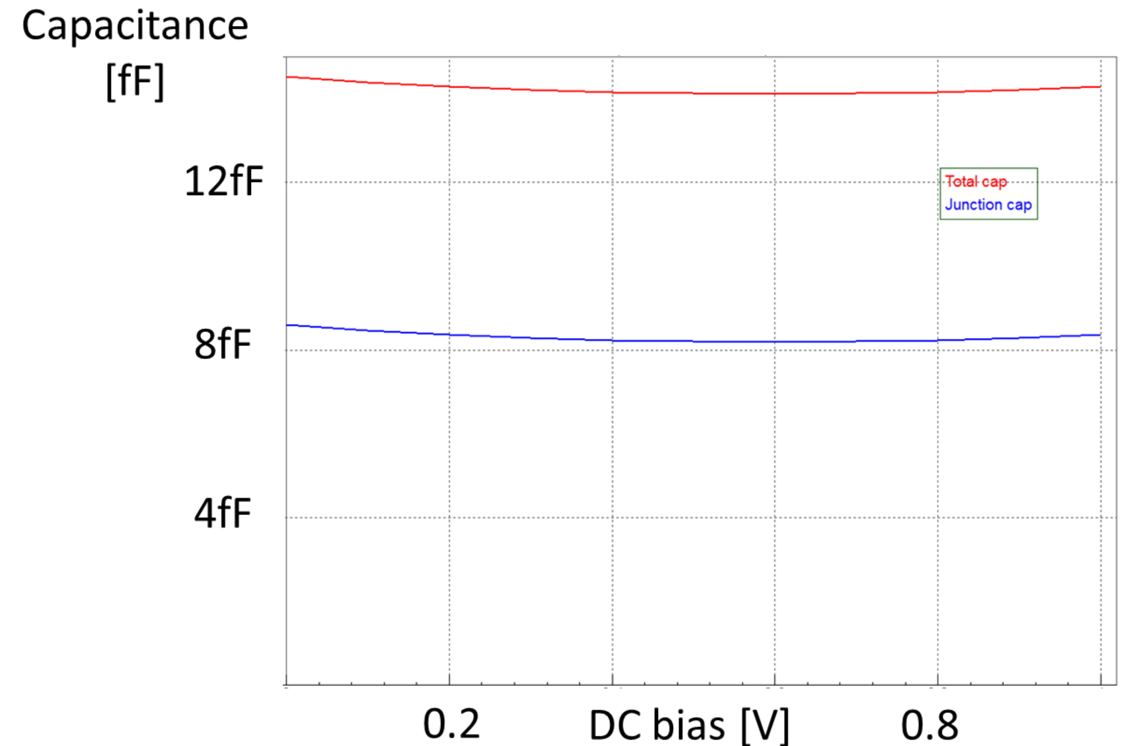
- Bluetooth – TSMC 40nm
  - ESD >5kV HBM
  - High Q factor, low capacitance
    - 177fF total capacitance
  - Low leakage:
    - 20pA at 1.2V accross temperature
    - Compare: 100nA at RT – conventional



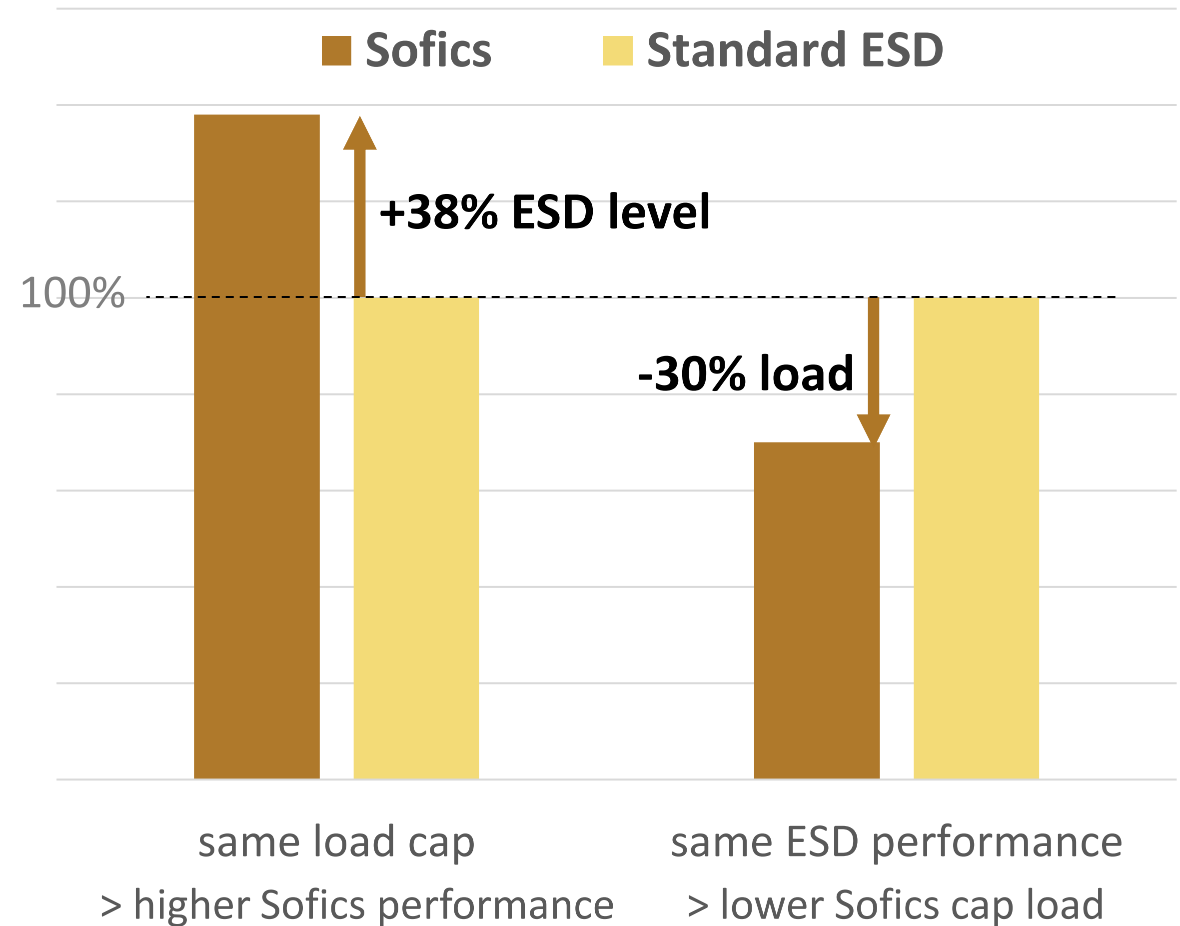
# High-speed I/O with ultra-low capacitance

- Silicon photonics – 22nm
  - Parasitic capacitance
    - Junction
    - Metal connections
  - Across DC bias at input



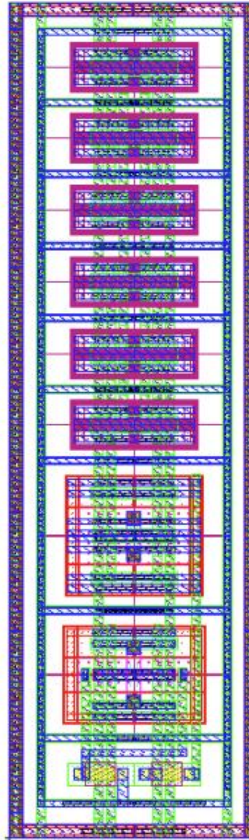
# Low-capacitance interfaces (FinFET case)

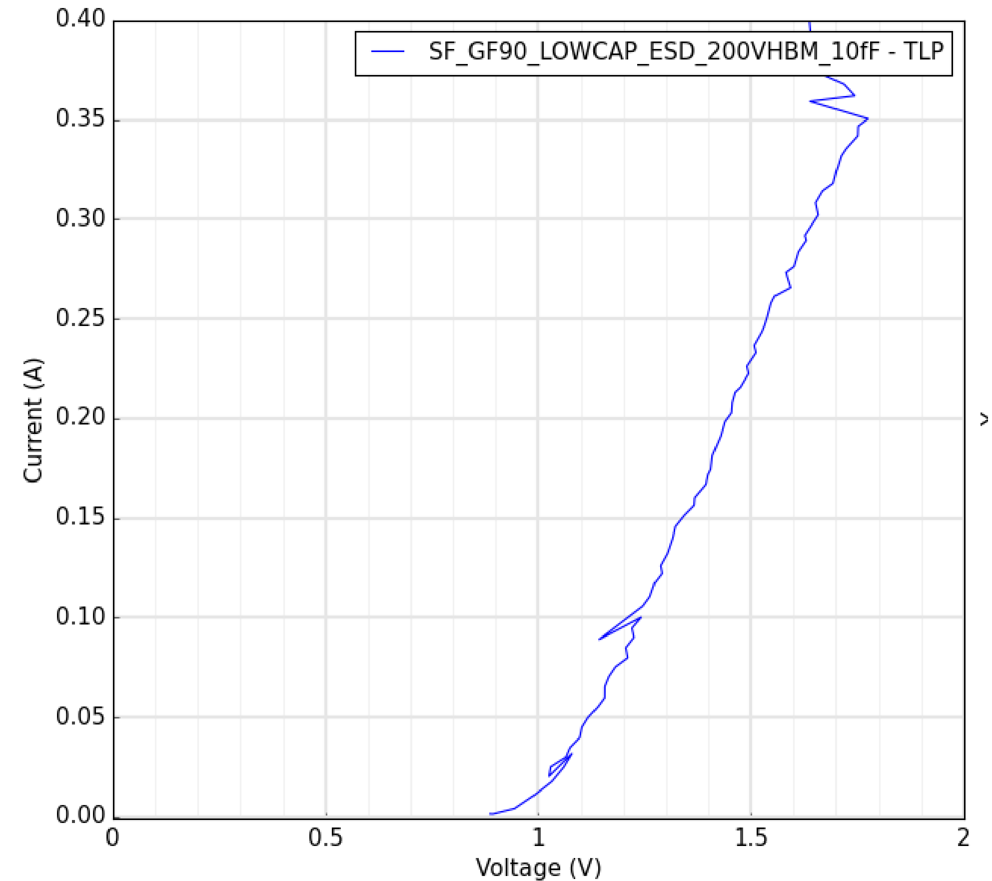
- Solution for:
  - High-speed interfaces
  - High frequency interfaces
- Typical specs:
  - Low RC
    - No input resistor
    - Low capacitive load
  - Protection of core interface
    - Narrow ESD design window



# Sofics ESD concept for very high-speed I/O

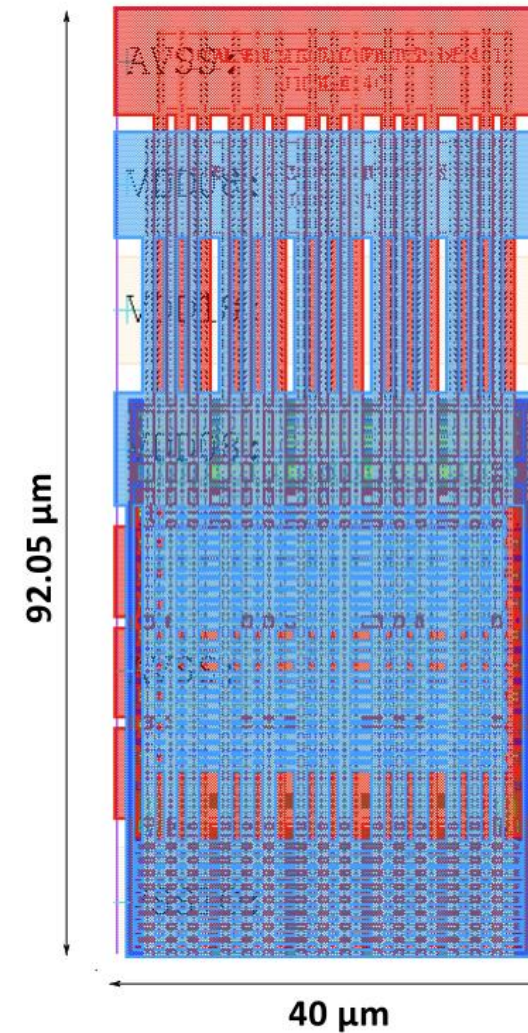
- Full local clamp – 2.5V reference
  - SiGe BiCMOS
  - Parasitic cap at I/O: ~7fF
  - ESD up to 500V HBM
  - I/O runs at max 1.0V
  - Area: 412 µm²
    - 11.02um x 37.30um





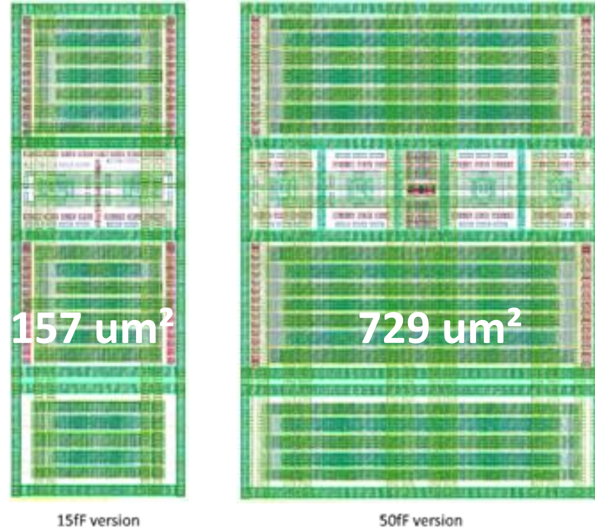
# Area efficient – high robustness solutions

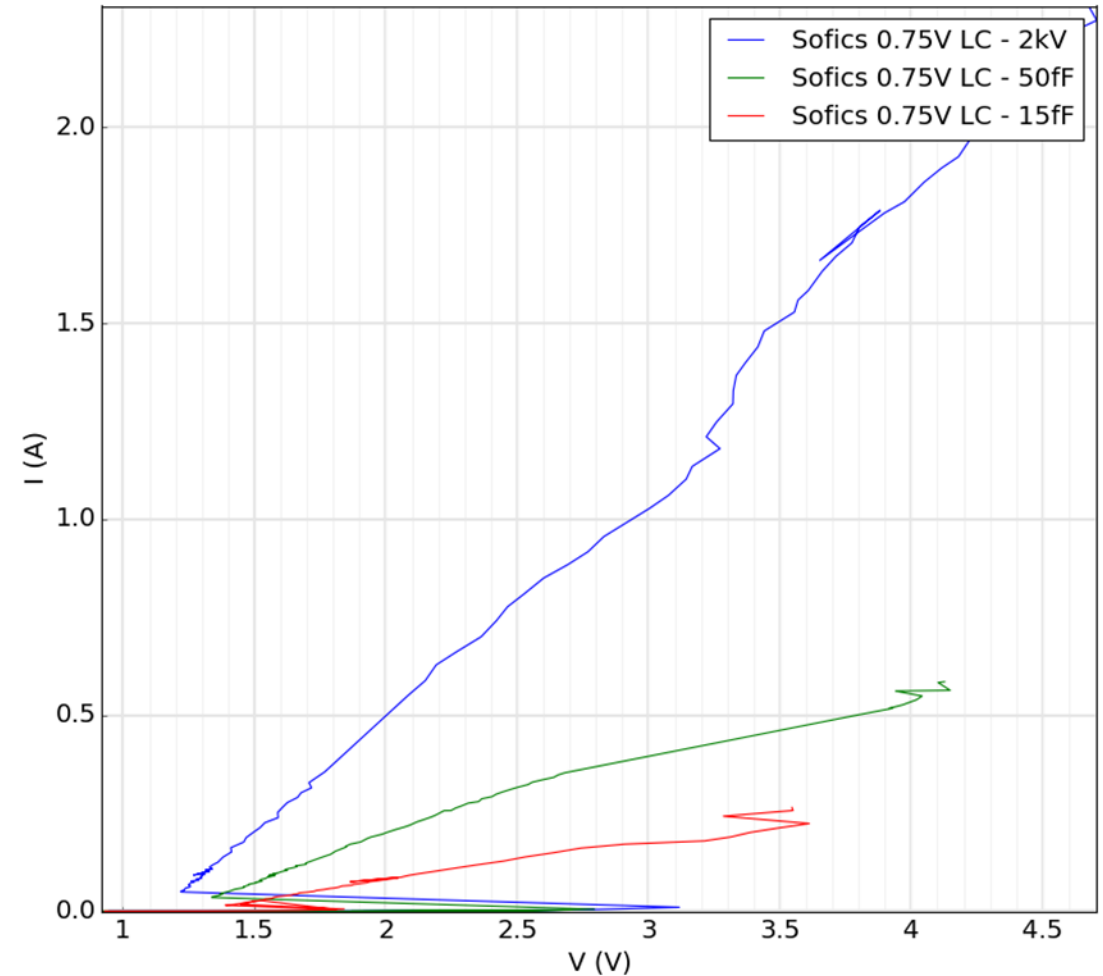
- TSMC 22nm ULL
  - 0.8V power clamp
    - 8kV HBM in 3682 um² area
    - Vt1 = 2.5V, Vh = 1.2V, Ron = 0.8 Ohm
  - 1.8V power clamp
    - 8kV HBM in 3086 um² area
    - Vt1 = 3.8V, Vh = 2.8V, Ron = 0.8 Ohm
  - 3.3V power clamp
    - 8kV HBM in 4935 um² area
    - Vt1 = 6.6V, Vh = 3.9V, Ron = 0.4 Ohm
    - 8kV IEC I/O available in 4770 um² area



# Enabling thin oxide gates in the I/O – 7n FinFET silicon proven

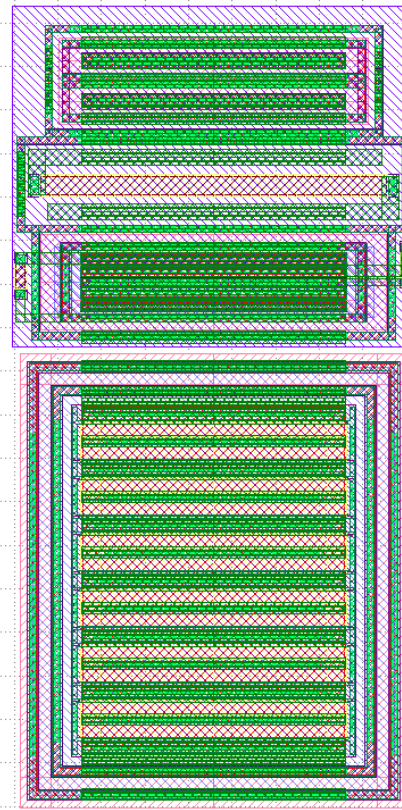
- Sensitive “core interfaces”
- ESD robustness as needed
  - 2kV HBM – thin oxide interface
  - 400/150V HBM – 50/15fF cap



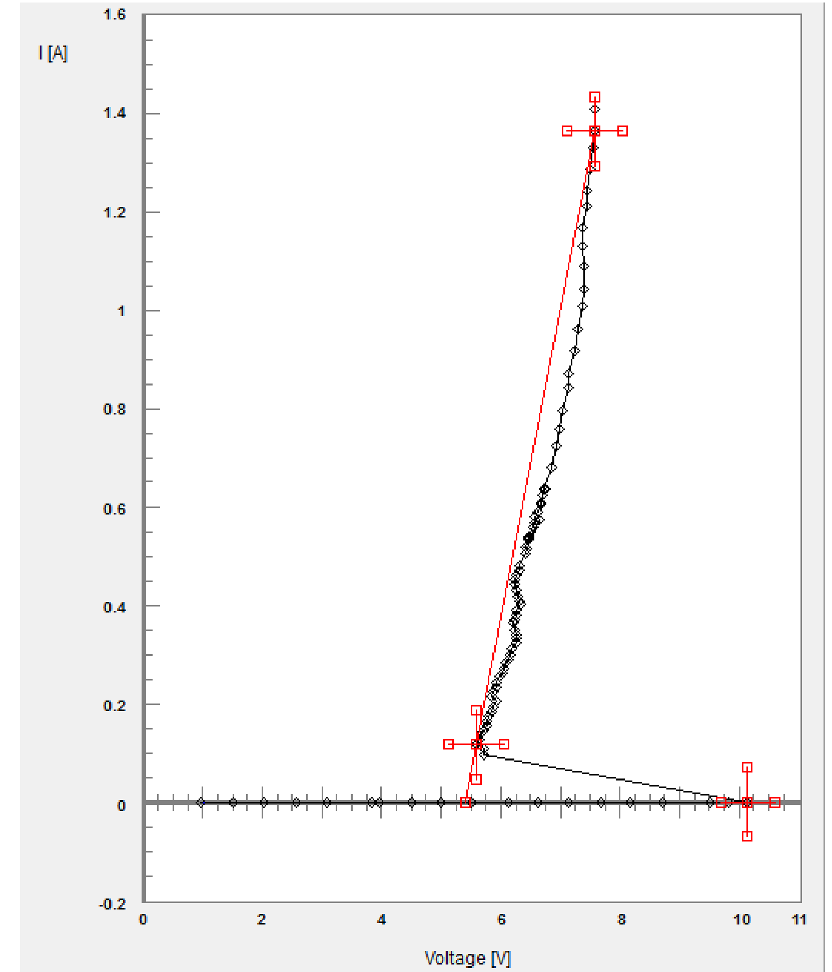



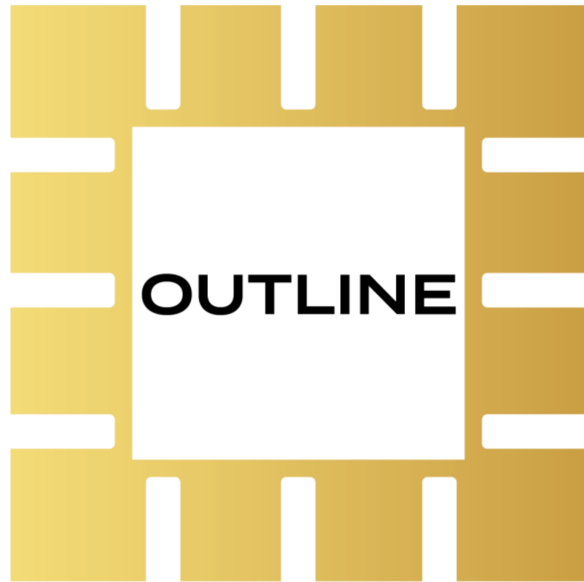
# 5V tolerant solutions

- 110nm CMOS
  - 2kV HBM, 4300um²
    - Vh > 5V, Vt1 ~10V
    - Leakage: 2pA
  - 9kV HBM, 6000um²
    - Vh = 2V, Vt1 = 6.5V
    - Leakage: 115pA



2kV version



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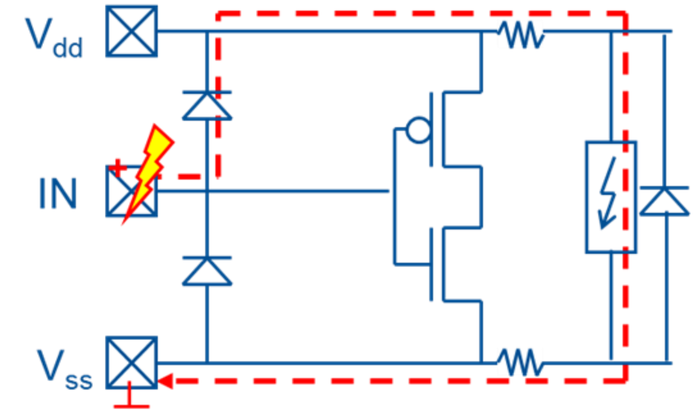
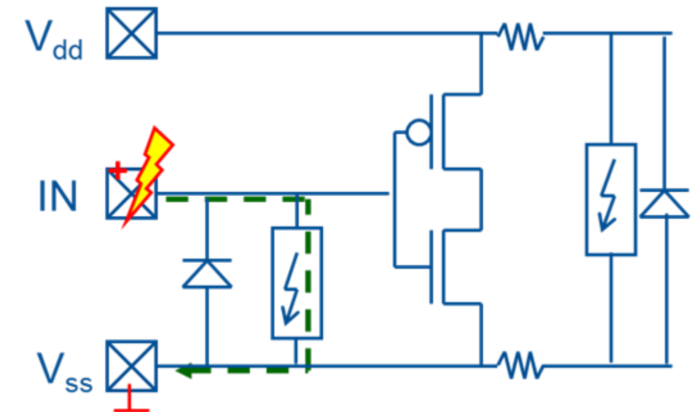
- Advanced CMOS / FinFET nodes
- Local clamp approach
- **Conclusions**

# Conclusions

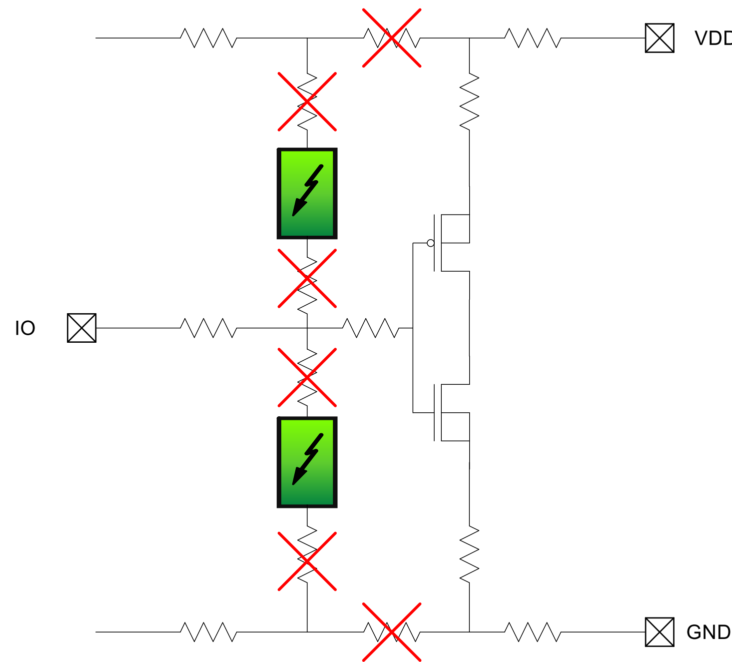
- Conventional ESD protection
  - Dual diode approach
  - Not optimal for advanced CMOS/FinFET
- Solution: (Semi) Local clamp
  - Proprietary ESD-on-SCR devices
  - Reduced influence of bus resistance
  - Reduced clamping voltage
  - Optimize every analog I/O separately.

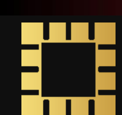


# Extra: Good practice

- Avoid bus resistance between victim circuit and clamp
- Avoid resistance between clamp and busses



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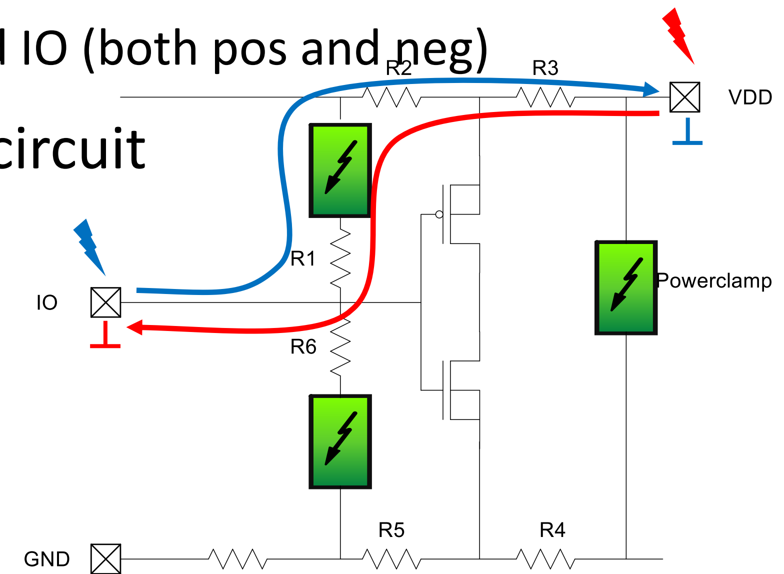
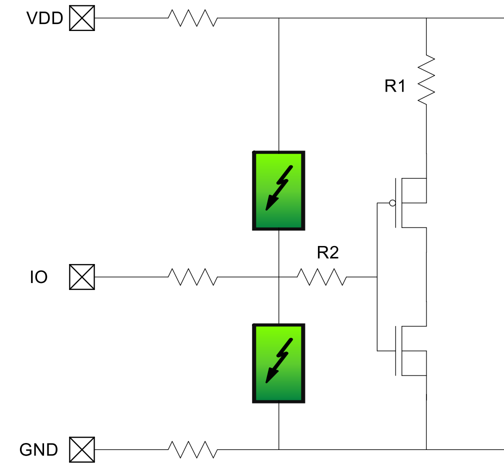
# Extra: bus resistance

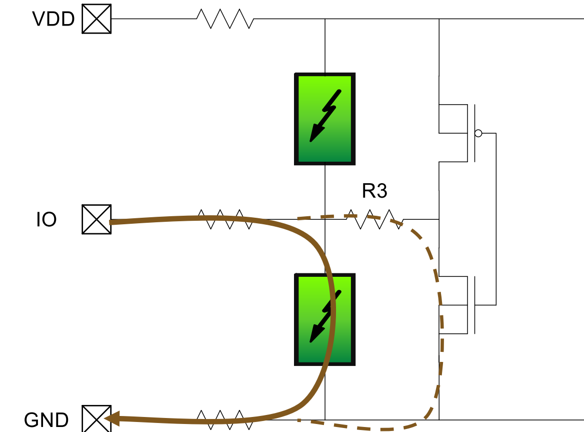
- Bus resistance is not always problematic
- If resistance is not part of the ESD path it will not determine stress case
- Resistance in ESD current path for local protection at IO
  - Is bad when it increases voltage drop over circuit
    - R1 and R2 are problematic for stress between VDD and IO (both pos and neg)
  - Has no influence when not causing voltage over circuit
    - Can limit total current
    - R3 is no problem

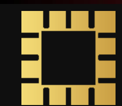


# Extra: Metal resistance – influence on design window

- Resistance at input gate will typically not make a difference
  - Resistance only builds up voltage if current runs through it
  - R1 and R2 don't change design window
- Resistance at output can be beneficial if some current flows through
  - Often current is very small so large resistor would be necessary to build up voltage
  - R3 can improve design window
    - Driver must conduct some ESD current => has to be robust



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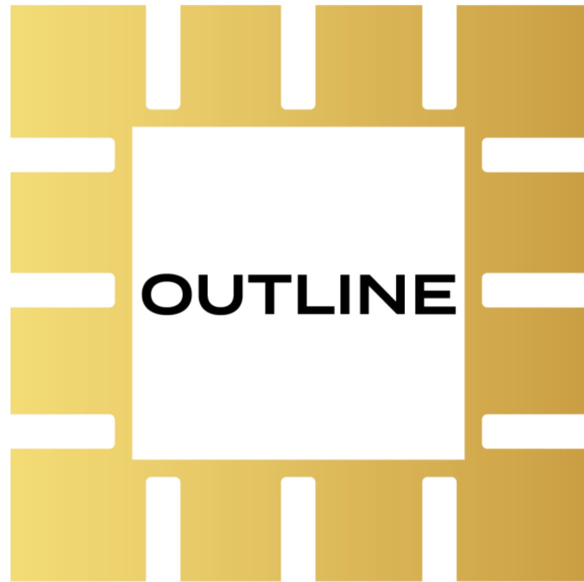


- Introduction
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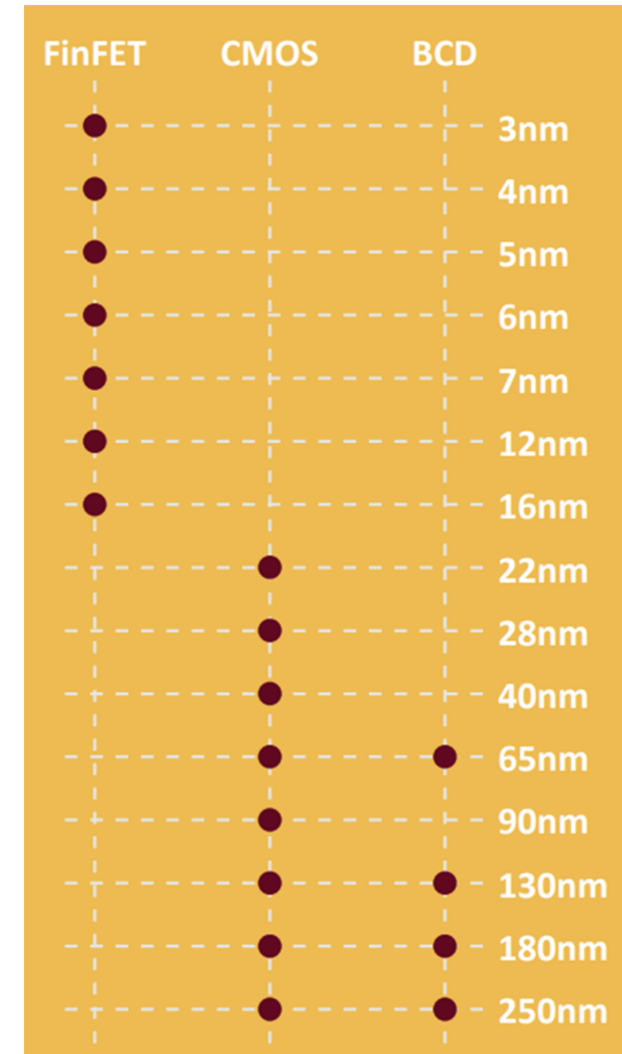
- **About Sofics**

# Solutions beyond Foundry Libraries for (Bi)CMOS, FF, GAA

- ESD protection solutions
  - RF
  - High-speed
  - Low power
  - Over-voltage tolerant
  - Small area
  - Extreme/IEC robustness
  - + EOS
  - + EOS + EMC
- Specialty I/O circuits
  - Over-voltage
  - Multi-voltage
  - Chiplets
  - Core transistor I/Os
  - Rad-hard
  - High-speed
  - RF
  - +EOS

# Sofics' IP is proven on 50+ processes

- CMOS
  - Mature: 0.5um to 180nm
  - Mainstream: 130nm to 65nm
  - Advanced: 40nm to 22nm
- FinFET and GAA technology
  - 16nm to 3nm – 2nm (on-going test chip)
- BCD technology
  - 250nm to 55nm
- BiCMOS technology



# 100+ customers across the globe and application space

# Just a few Sofics IP applications…

## Internet of Things, wearables

15+ customers

Battery-less processors

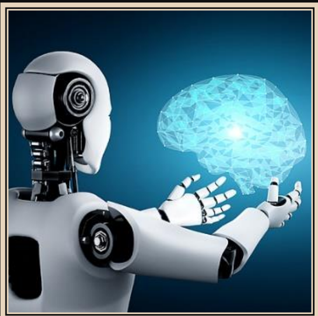
Health monitoring

## Automotive

15+ customers

LIN, CAN

Car keys



## Artificial Intelligence

5+ customers

Data processing – compute

Inference

## Medical

5+ customers

Hearing aids

Imaging (endo/arhtroscopy)

## Space

5+ customers

Radiation hardness

CERN – particle research

## Datacenter and wireless

40+ customers

Silicon-photonics interfaces

40% of Bluetooth market

# More about us...

- Get more information
  - Sofics website
  - Blog
- Stay informed
  - Follow us on LinkedIn
- Connect in person
  - Ehsan Fallah
  - Bart Keppens

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