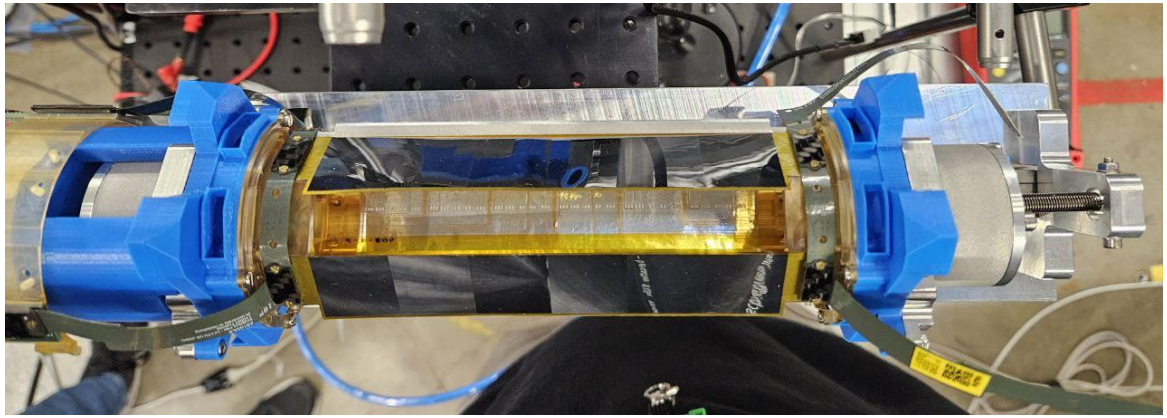
University of Zurich[UZH]

Physik-Institut

Production and Qualification of the Mu3e Vertex Detector

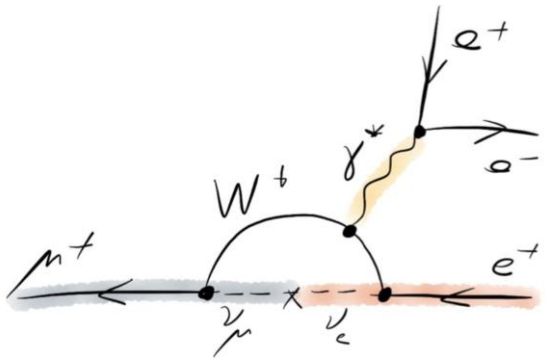


Thomas Christian Senger

On behalf of the Mu3e collaboration

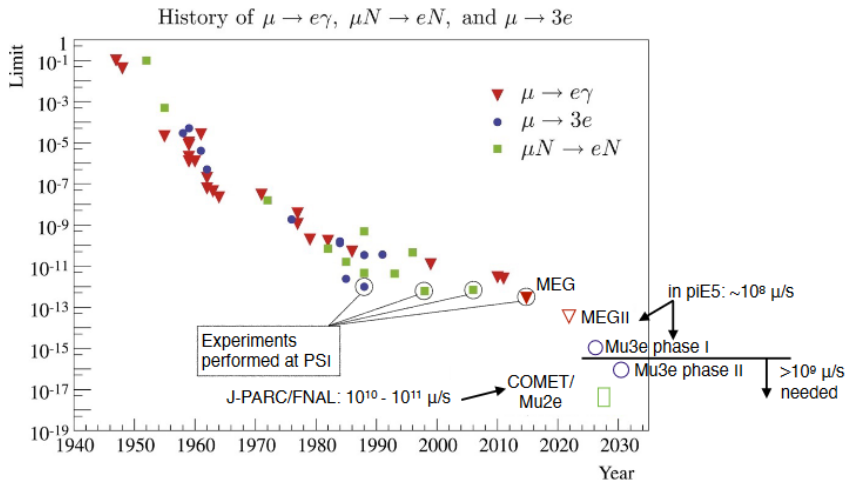
Probing the standard model with Mu3e

- Mu3e is a high-precision experiment at Paul Scherrer Institut (PSI) in Switzerland
- Search for the Charged LFV decay $\mu \rightarrow eee$
  - Highly suppressed in the SM BR($< 10^{-54}$)
    - Via neutrino mixing
  - Best current upper limit $\mu \rightarrow eee \approx 10^{-12}$ @90%C.L. from SINDRUM in 1988



Standard model decay via neutrino mixing

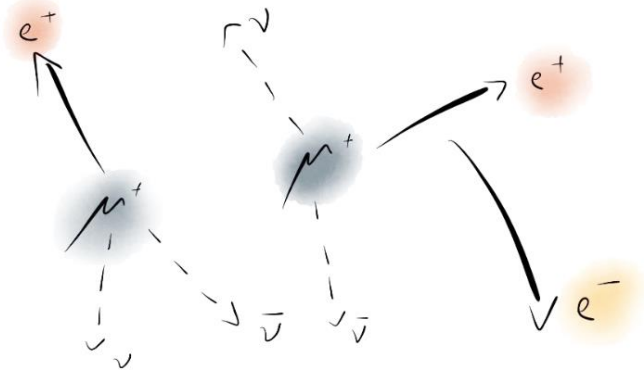
- **Goal of Mu3e**
  - Improve limit by 3 to 4 orders of magnitude
  - BR($\mu \rightarrow eee \approx 10^{-15}$) in phase I (2025+2026)
  - BR($\mu \rightarrow eee \approx 10^{-16}$) in phase II (2029+)



Experimental challenges

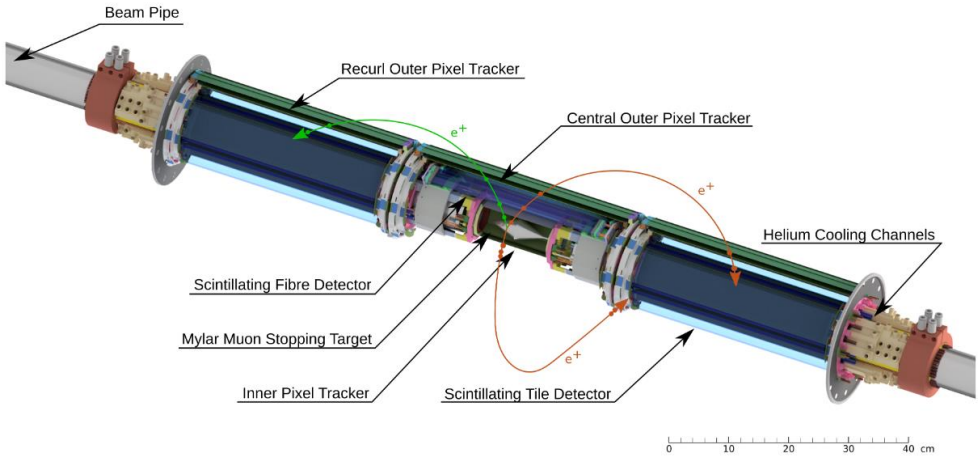
- Low momentum particles
  - Muons decay at rest
    - → Electron/Positron momenta < 53MeV/c
- Momentum resolution limited by multiple Coulomb scattering
- Accidental background in signal region must be minimized

→ Low material budget
→ High granularity and fast processing
→ Excellent momentum resolution
→ Good timing (order of 100 ps) and vertex resolution (≈ 0.5 mm)



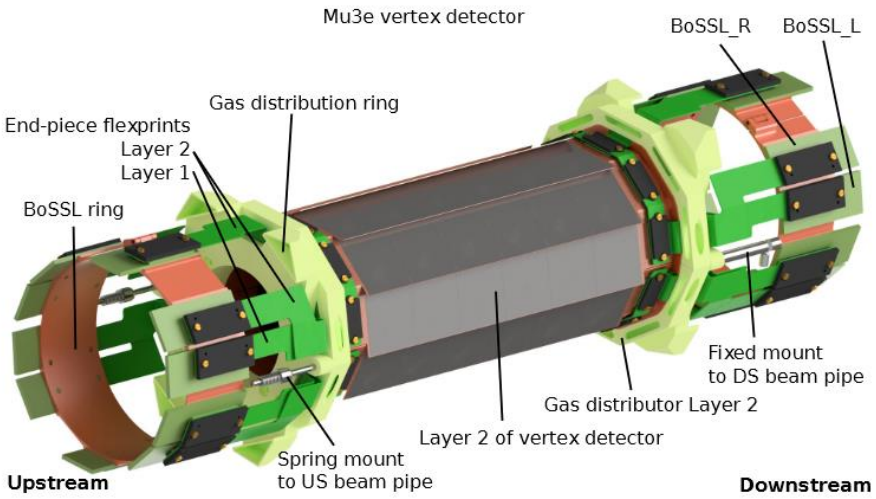
The Mu3e detector

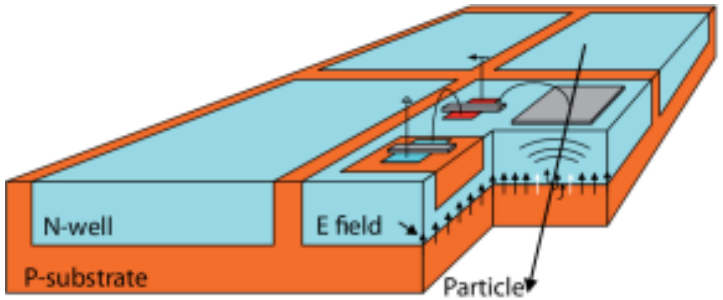
- Hollow double cone stopping target
- Homogeneous solenoidal magnetic field
- 4 layers of pixel sensors
  - Inner two layers for vertexing
  - Pixel recurl stations for optimal momentum resolution and acceptance
- Scintillating fibres and tiles for precise timing measurements
- High rates 10^8 muon decays per second)
- Expected data rate of up to 100GBit/s



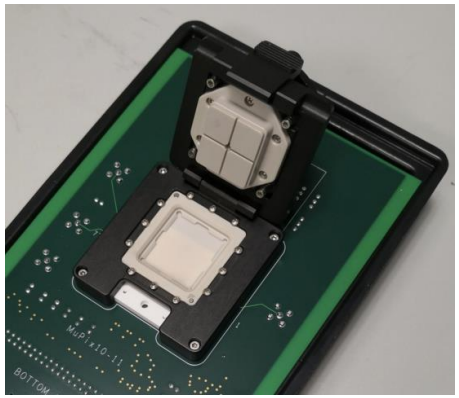
Mu3e Vertex Detector

- Two layers of 50µm thin Mupix 11 pixel sensors
  - High-Voltage Monolithic Active Pixel Sensor (HV-MAPS)
  - Detection and Readout combined in one chip
  - Fully digital 1.25Gbit/s LVDS output
  - 99% efficiency with less than 20ns time resolution
- Mechanical support
  - Aluminized Kapton foils HDI
  - Sensors glued on foils + spTAB for electrical connection
- DAQ to sensor connection via micro-twisted pair cables and other flexes produced with standard processes
- Cooled by gaseous helium

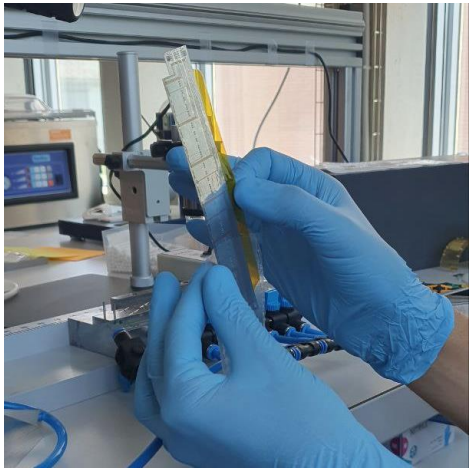




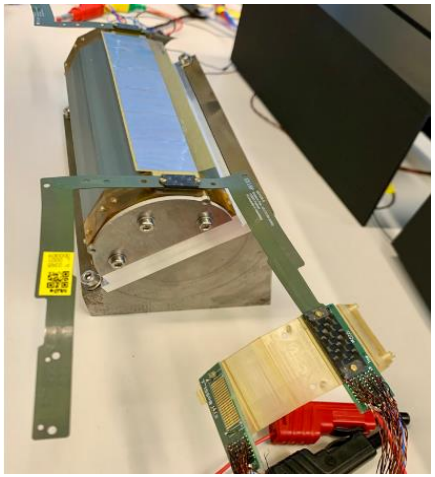
Construction of the Vertex Detector



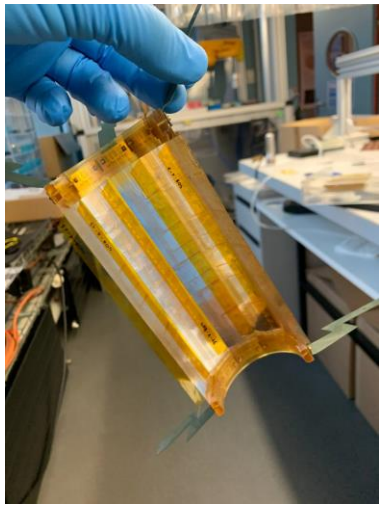
Single Chip QC



Ladder Production

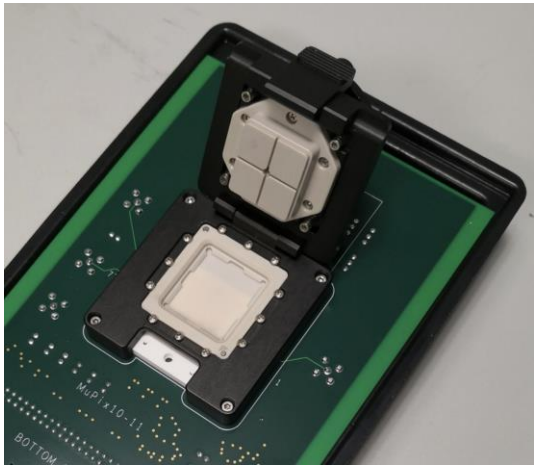


QC of Ladders and Services



Module assembly

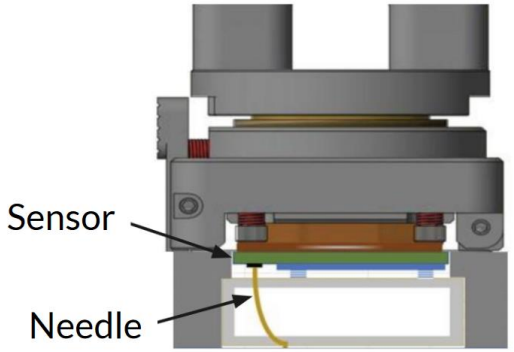
Manual Single Chip QC



- Press down mechanism with contact needles
- Single chip QC consisting of 8 electrical tests
  - Basic electrical tests (IV, on chip voltage regulation, power consumption)
  - LVDS link stability
  - Noise scan

- QC takes 30min per chip
- Based on a grading scheme

- Current chip yield of 50-60 % after single chip QC



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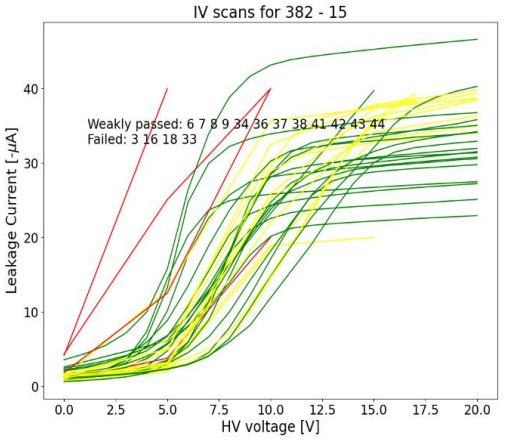

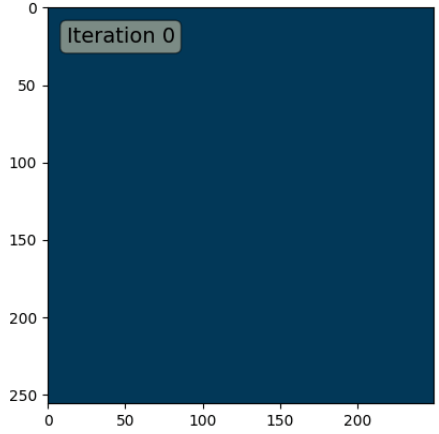

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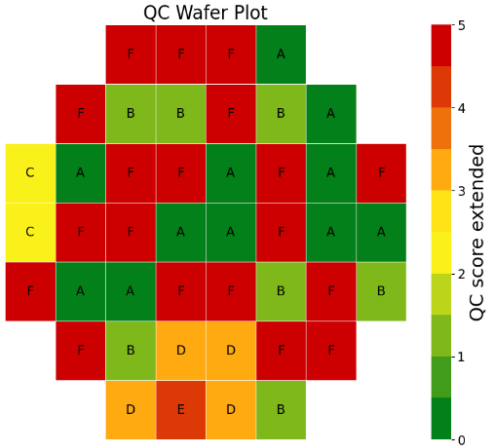

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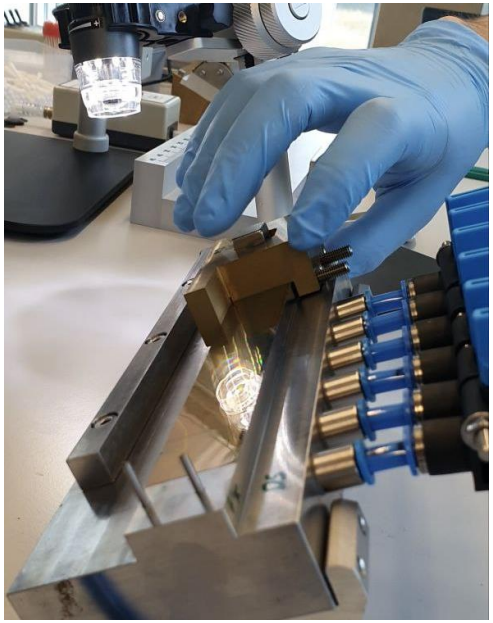
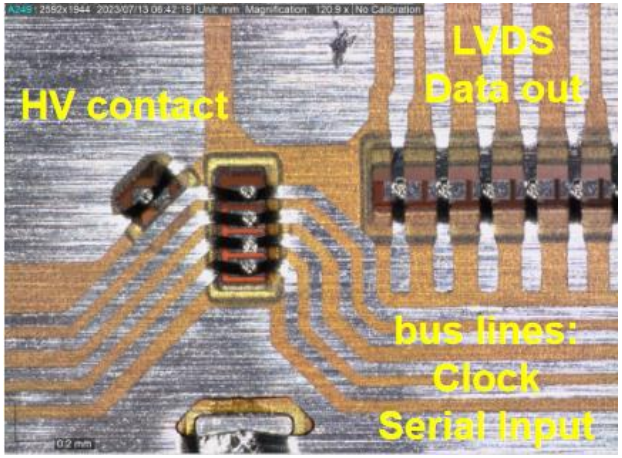


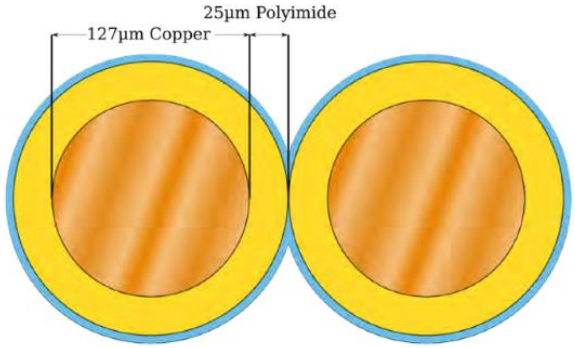
Manual chip placement

Distribution of the glue on the Mupix sensors

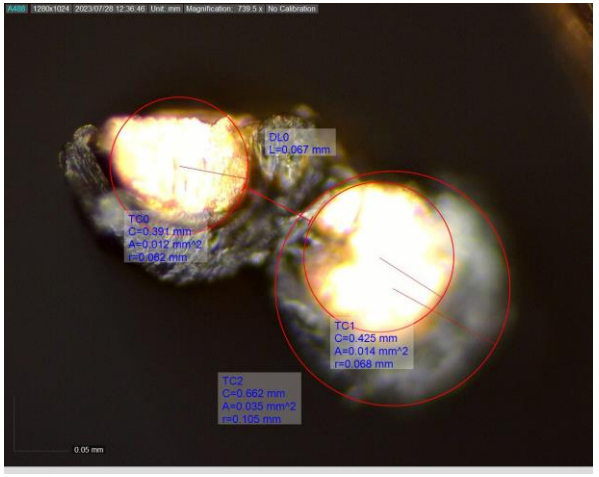


spTAB connections from HDI to the MuPix chips

µTP cables



- Need to use µTP cables due to space limitations
  - Successfully used by CMS pixel detector, at a lower a data readout
- Measured significant variation in impedance, increased signal loss, and differential pair distances compared to spool used by CMS
  - Signal loss up to ≈ 70% at 1.25Gbit/s
- QC for µTP cable
  - Measurement of insertion loss, differential impedance and cross talk



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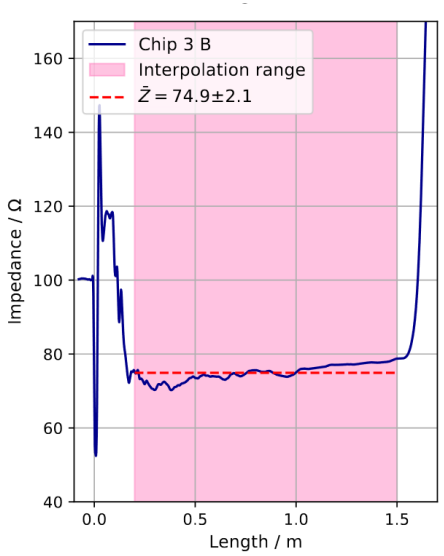
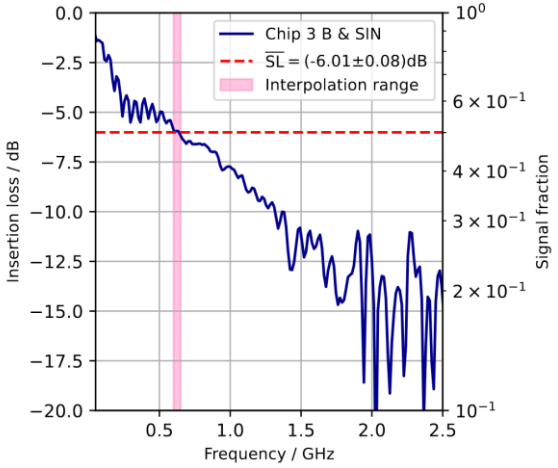
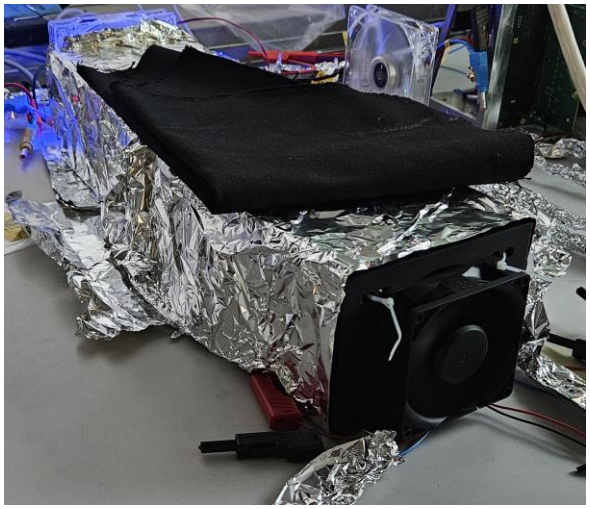
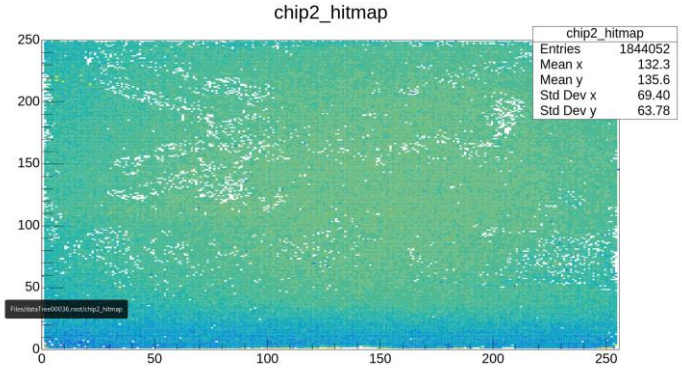




Ladder QC

- Ladder placed a 3D printed box
  - Cooled with two fans
  - Shielded with aluminum foil
- Ladder is connected via µTP to the FPGA
  - All connections placed as in the final detector
  - Only DC-DC-converter and HV boxes are replaced with comericial power supplies (Hamegs + Keithleys)
  - Temperature readout through on chip temperature diode
- Similar QC test procedure as for the single chip
  - Additional signal transmission test
  - Final source scan with applied noise masking at a low threshold
- Takes ~6h per ladder
- Goal is to find 18 good working ladders + spares



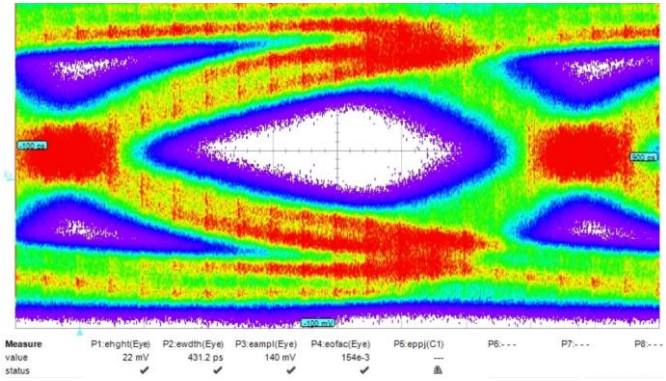


Signal transmission test

- Challenge of errorfree links on a ladder
  - 8b10b encoding & disparity errors
  - Crucial for a precision experiment
- Different causes compared to single chip QC
  - Light + Heat → high leakage current →noise
  - Connections of various detector components
  - Different voltage drops over a ladder
  - No specific ladder DAC optimization
  - High signal loss due to transmission through µTP cables
  - only short connections used with single chips

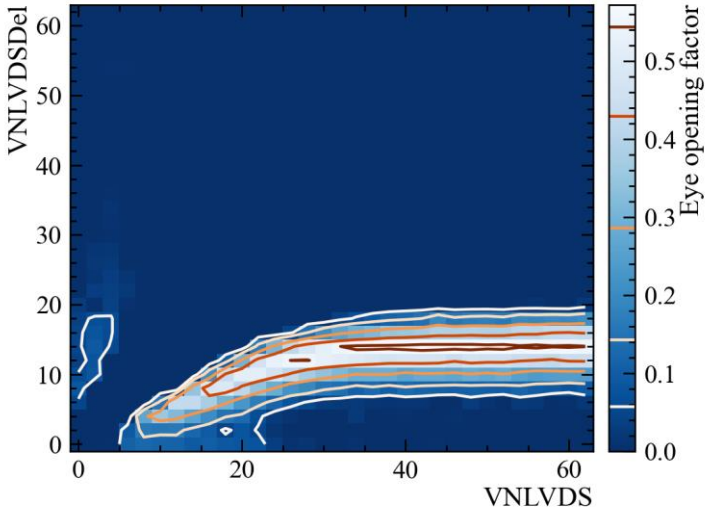
Signal transmission test

- Chip internal peremphasis + signal amplication can recover the eye opening of transmitted chip data
- Design of additional QC test
  - µTP signal transmission studies show optimal transmission at preemphasis ~ 30% signal amplitude



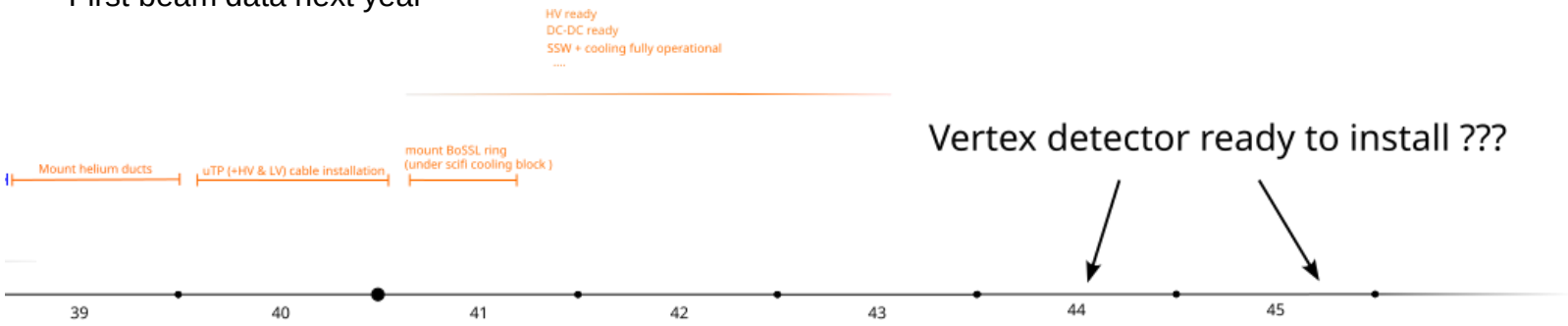
- Found plateau where error free transmission is possible
  - With increase of preemphasis eye opening factor increases
  - Signal amplitude dereases

- 3 dimensional scan in „plateau region“ for each chip
  - Additional scan of another DAC for the regulation of the differential current logic



Current time line

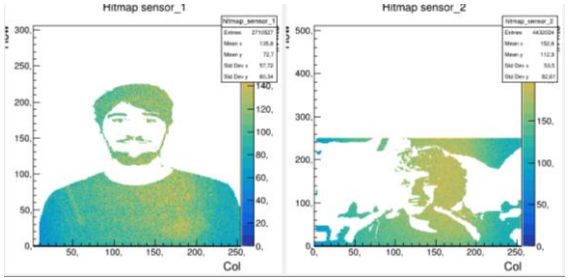
- Cosmic run with all services installed in November/December
  - Development of calibration, monitoring and data taking routines
- Tested seven wafers for production
- Ladders are currently constructed and qualified
  - Current ladder yield of <50% (preliminary)
- Module construction in the first week of October
  - Module QC (basic tests)
- Services/Cooling and DAQ are currently being installed
- Also other Detector components are installed
- Yifeng will give an overview in the next talk
- First beam data next year



Backup

Testbeam at Desy in May and PSI in October 2023

- 50µm & 70µm single chip testbeam at Desy
  - Demonstrated the capability of masking
  - Efficiency studies showed capapility to go to efficiency of 99%



- First testbeam with 2 operational ladders at PSI
  - Beam clearly visible on ladder
  - Correlation studies with 2 quad modules + scifi