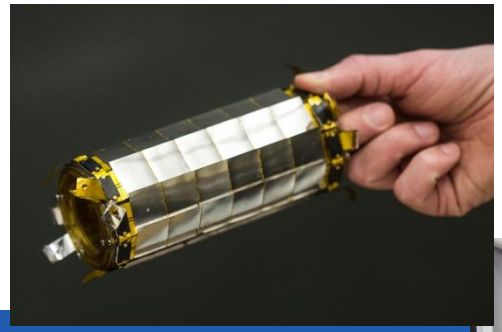
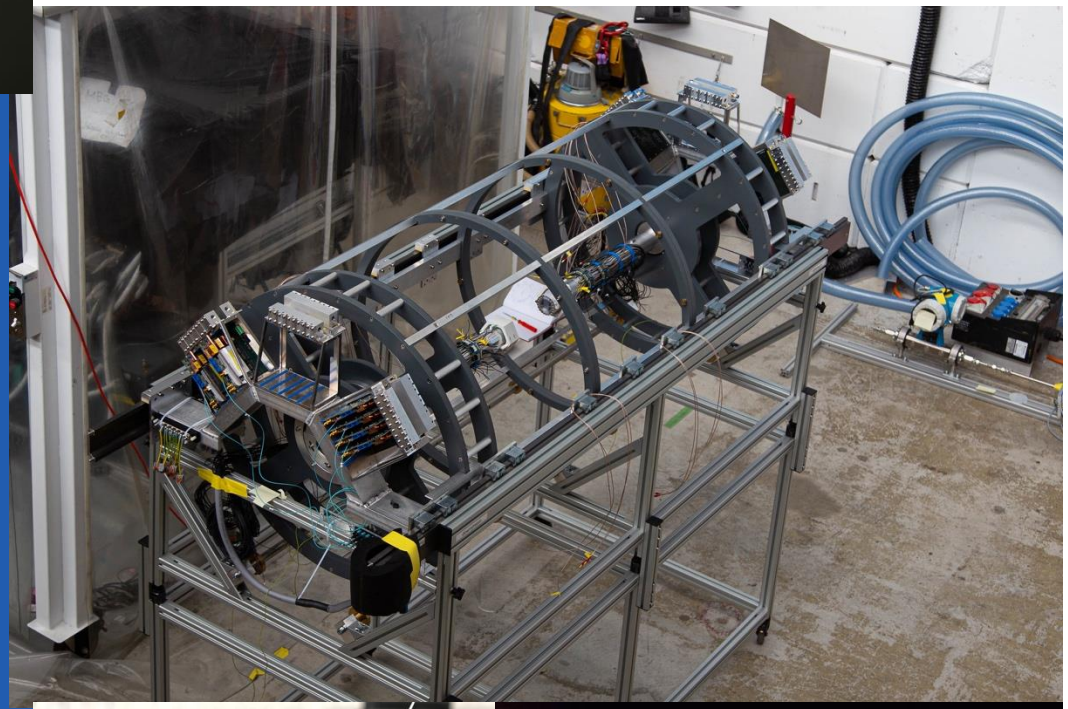
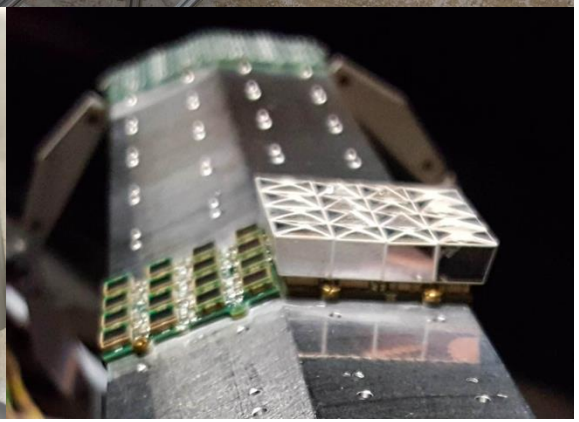




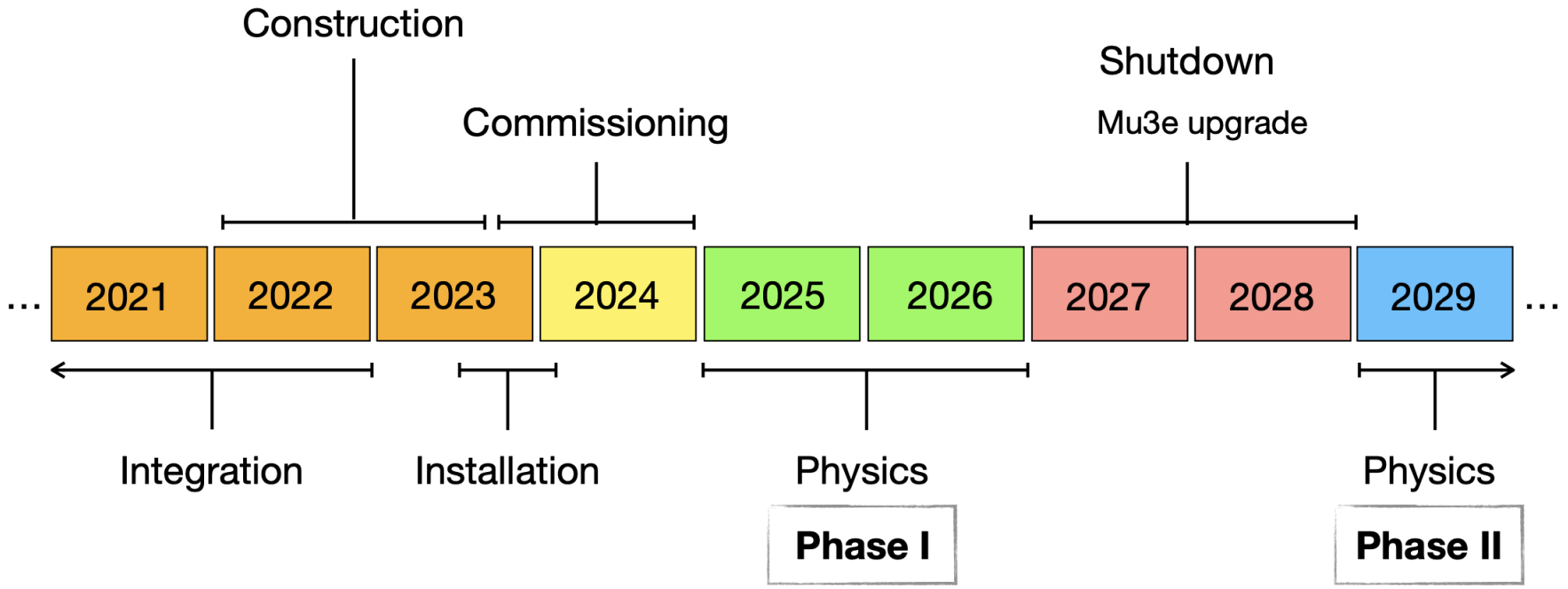
SciFi and DAQ Status Report of the Mu3e Experiment

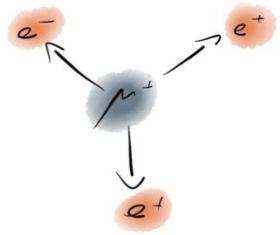
SPS annual meeting 2024

Yifeng Wang
10.09.2024



Schedule

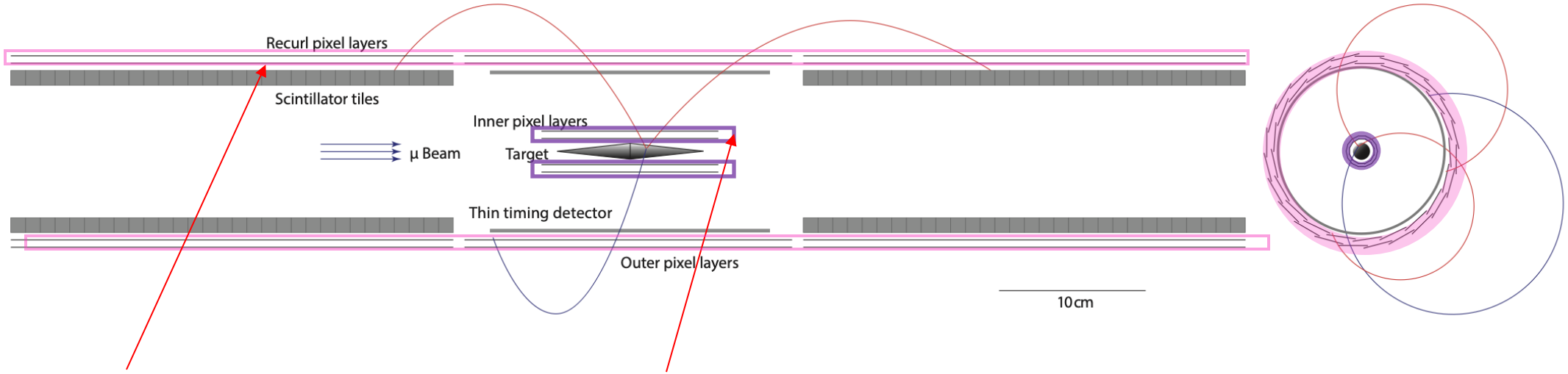




Phase I: >10^{15} muons = time * rate = 2.5*10^{7}s (290days) * $10^{8}\mu^{+}$/s

$\Rightarrow \boldsymbol{\mathcal{B} < 2 \times 10^{-15}}$

Mu3e detector overview

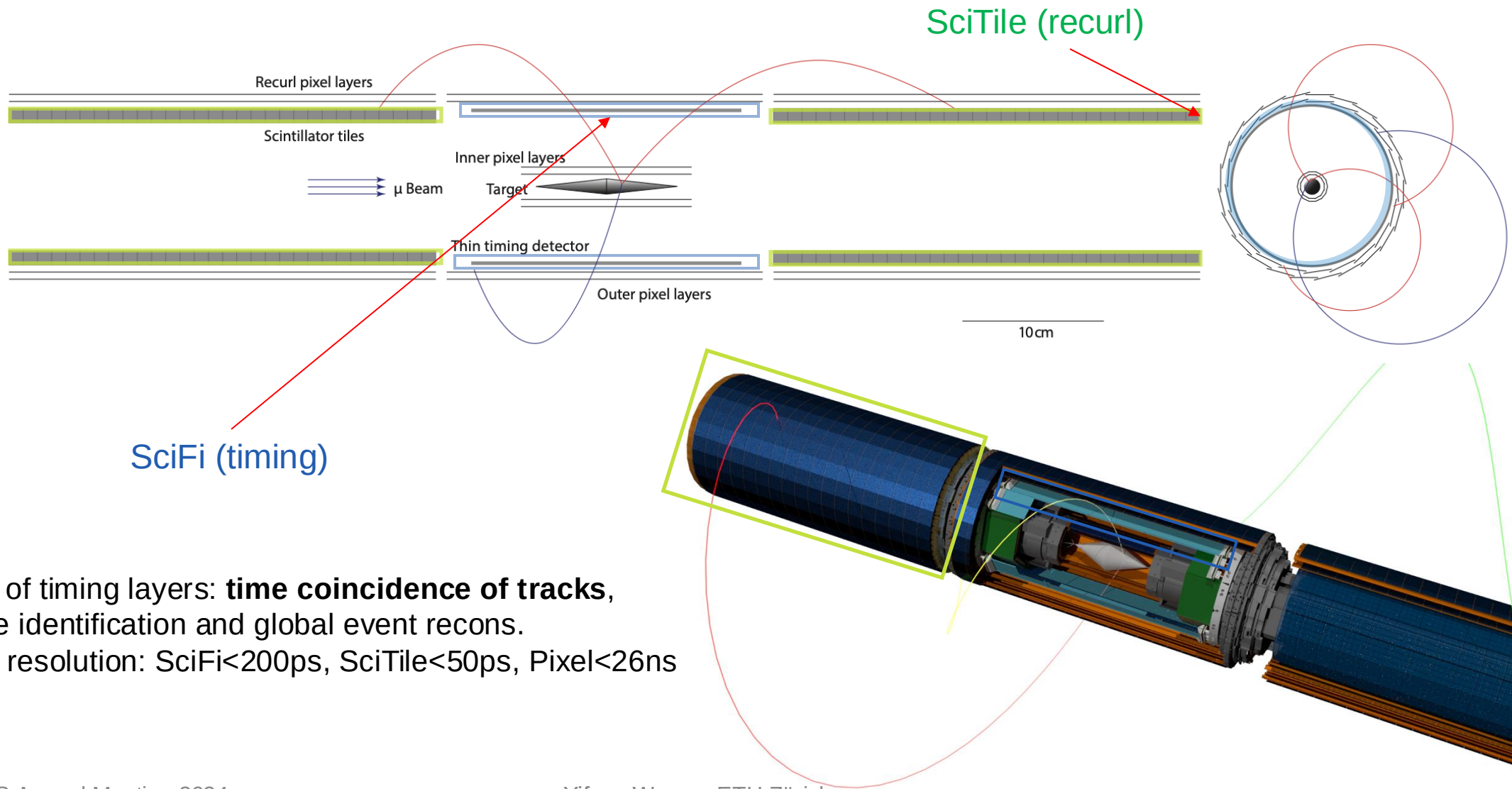


Outer pixel (recurl)

Inner pixel (vertex)

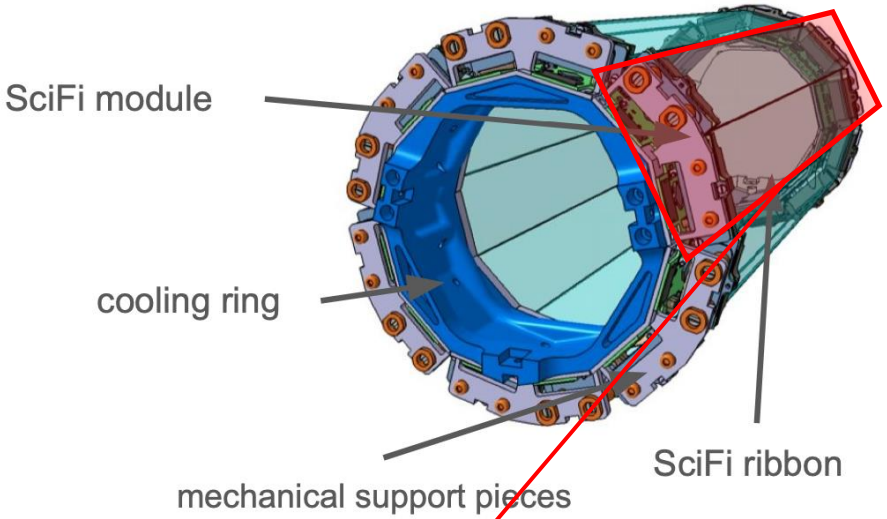
See Thomas Senger's talk

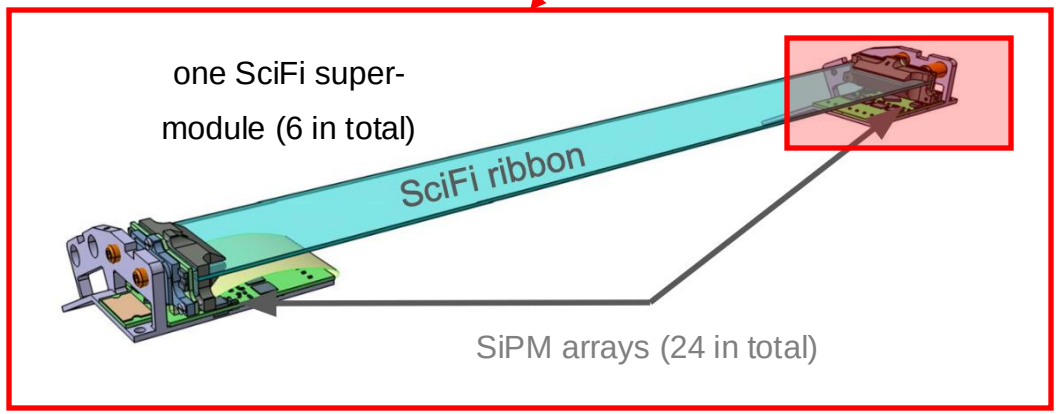
Mu3e detector overview



Goals of timing layers: **time coincidence of tracks**,
charge identification and global event recons.
timing resolution: SciFi<200ps, SciTile<50ps, Pixel<26ns

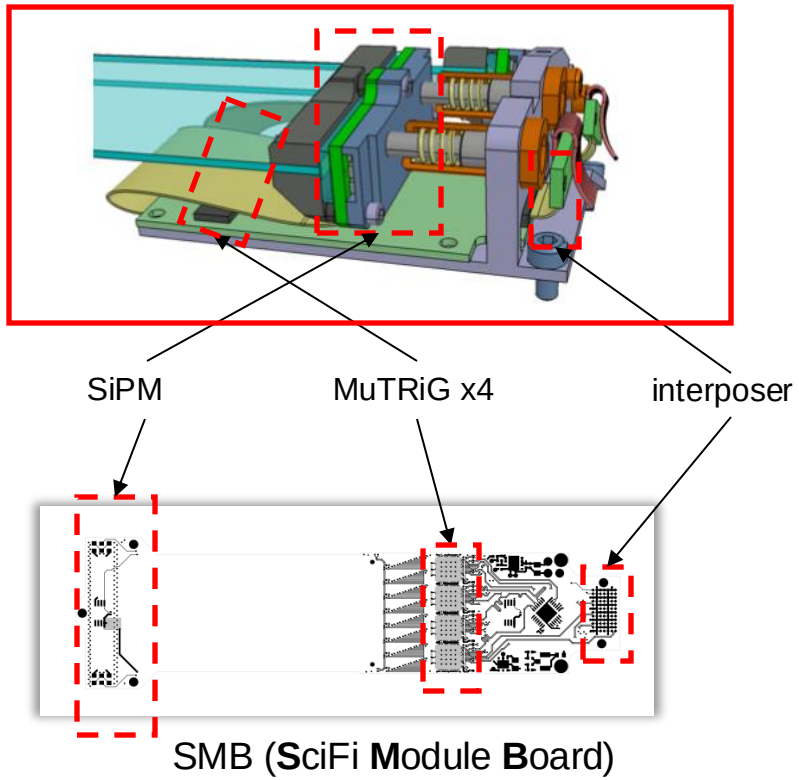
SciFi detector overview





Ref: Y. Demets, BVR 2023

Ref: 2208.09906



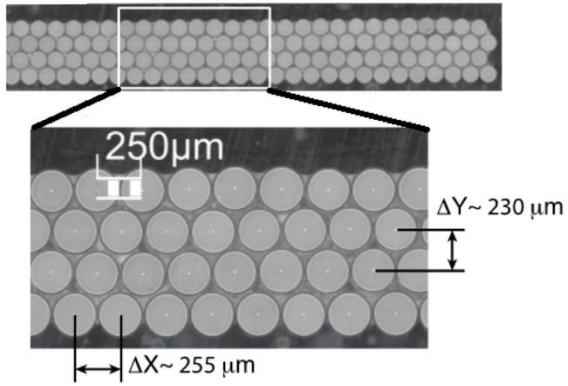
SMB (**S**ciFi **M**odule **B**oard)

<u>Detection and data flow:</u>

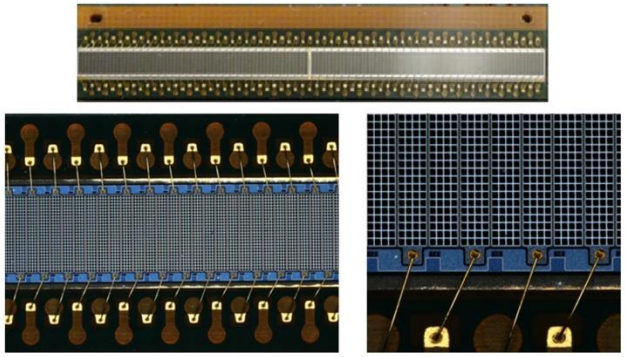
Ribbon → (photon) SiPM → (electrical (analog)) MuTRiG → (electrical (digital)) FPGA

Connection

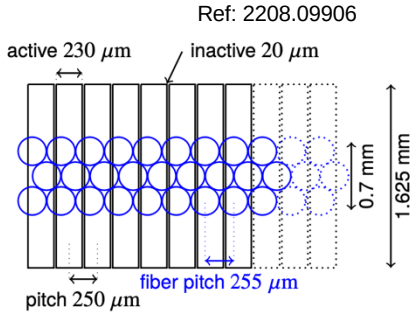
Fiber ⇔ SiPM



Cross-section of fiber ribbon end (stagged 4 layers of fiber)



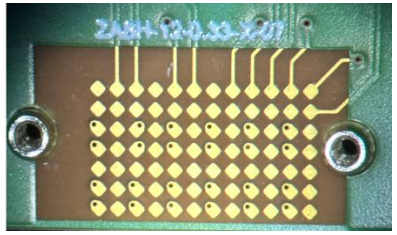
SiPM array (Hamamatsu S13552)



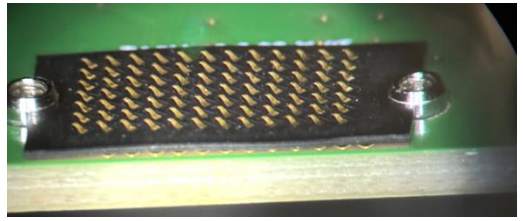
Fiber attaching to SiPM

SMB ⇔ uTP cable

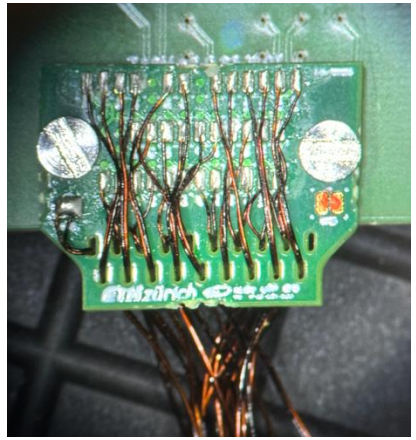
SMB PCB footprint



Interposer

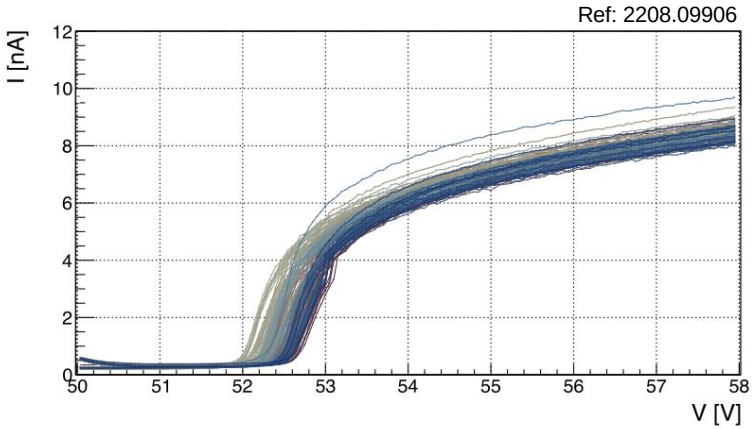


uTP cable connector PCB



Calibration and pre-installation quality control

SiPM QC



1) Measure IV curve of 128 ch of SiPM array => **breakdown voltage (gain)**

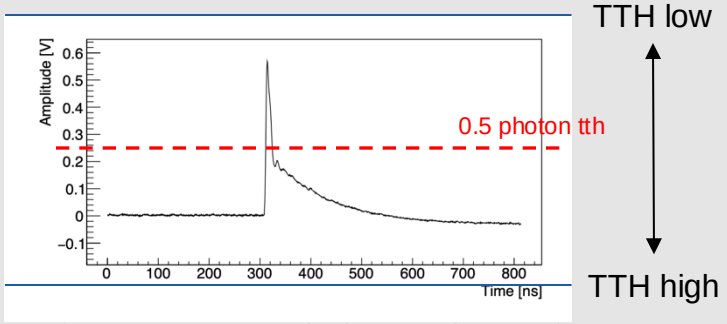
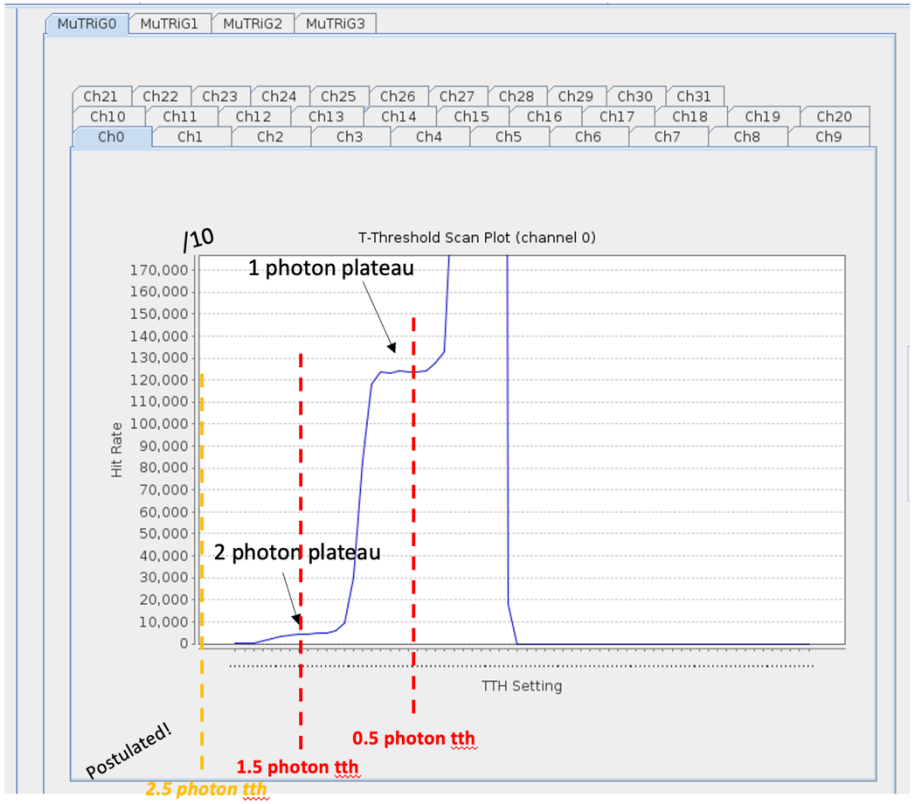


Figure of DRS4 measured SiPM 1-ph waveform
(for illustration only)

MuTRiG Calibration (Threshold)

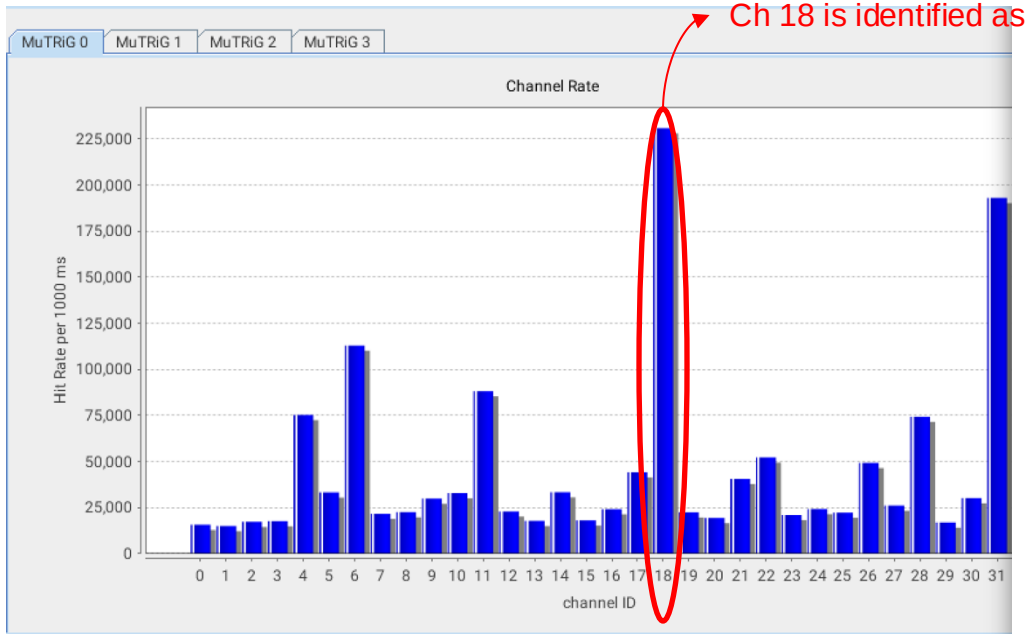
2) Measure TTH scan => **threshold for TDC**



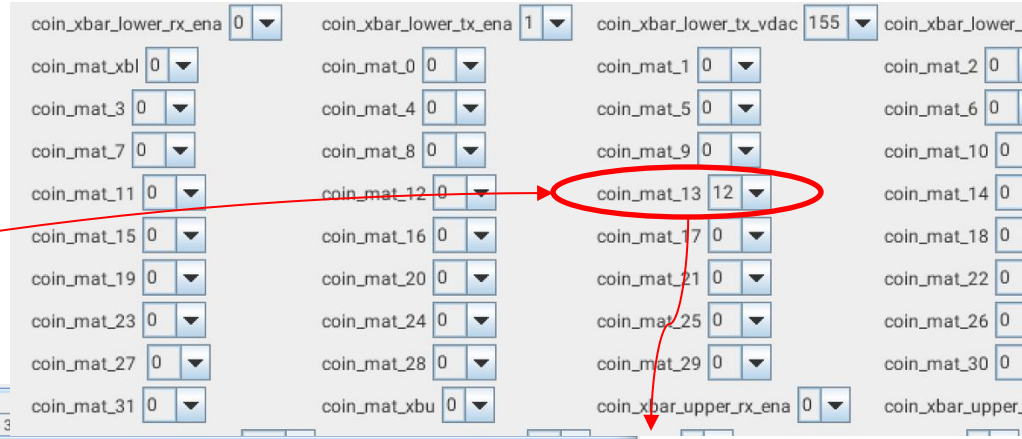
Demo of TTH scan; TTH (x) vs event rate (y) of single ch of MuTRiG

Calibration and pre-installation quality control

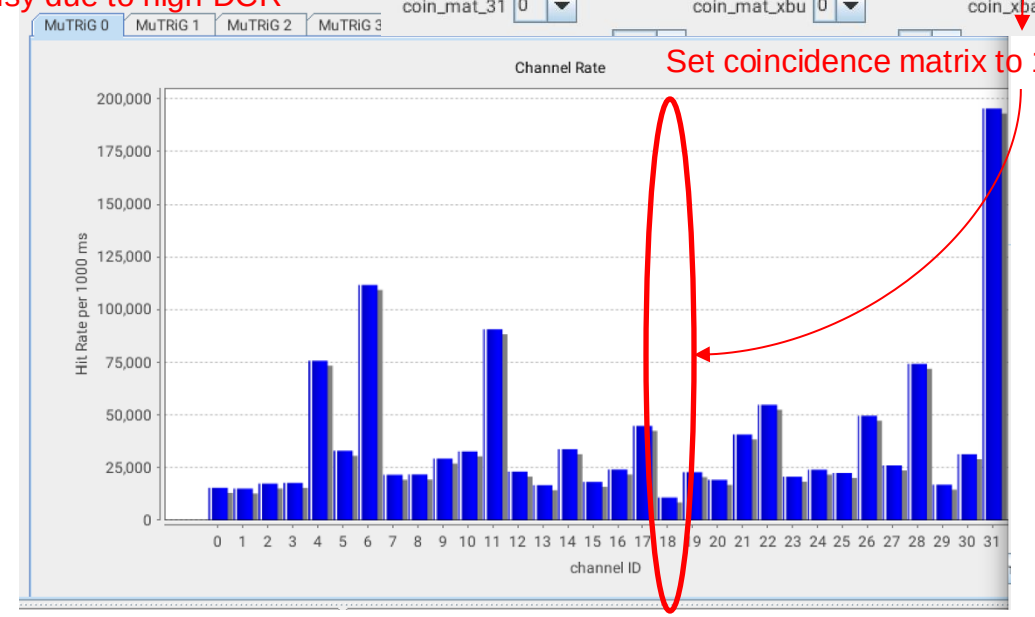
MuTRiG Calibration (noise supp.)



Ch 18 is identified as noisy due to high DCR



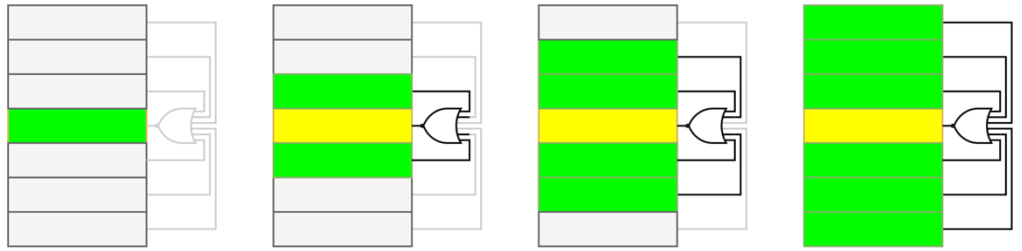
Set coincidence matrix to 12 (dec) or 001100 (bin)



DCR is suppressed!

Coincidence logic:

- within 1-2 clock cycle upon hit, if neighbor channels are hit, this channel's data is kept, otherwise discarded.

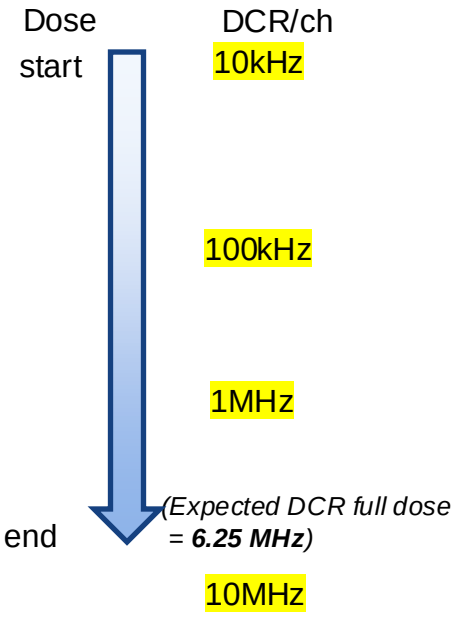


Behavior	Off	left-right 1 ch	left-right 2 ch	left-right 3 ch
Setting (bin)	000 000	001 100	011 110	111 111
Setting (dec)	0	12	30	63

MuTRiG Calibration (Simulation)

ϵ (efficiency) := max readout speed / tot hit(signal+DC)

π (purity) := signal hit ref / signal rate with injection



Expected dose on SiPM and inflected DCR

DCR / ch	ϵ	π	Reduction ratio	Event rate / ASIC
0	100%	1 (ref)	0.798	6.77 MHz
100k	100%	99.4%	0.577	6.81 MHz
500k	100%	94.0%	0.292	7.20 MHz
1M	100%	82.4%	0.201	8.21 MHz
2M	100%	56.9%	0.163	11.9 MHz
3M	100%	38.3%	0.168	17.7 MHz
4M	98.1%	26.6%	0.186	25.5 MHz
5M	71.1%	19.2%	0.208	35.2 MHz
6M	53.6%	14.5%	0.231	46.6 MHz
7M	41.9%	11.3%	0.255	59.7 MHz
8M	33.6%	9.03%	0.280	74.5 MHz
9M	27.5%	7.45%	0.305	**90.8 MHz**

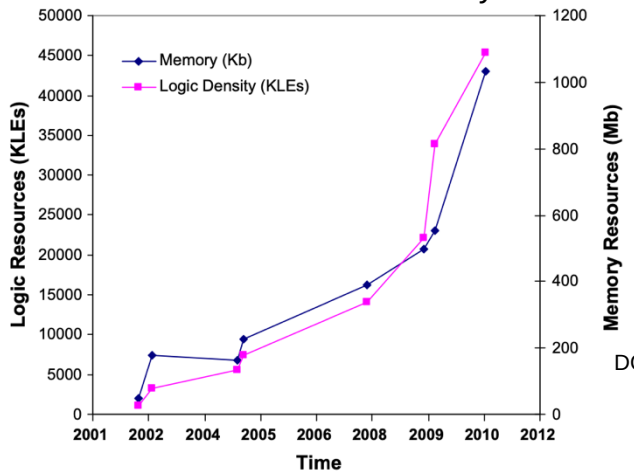
Simulation condition: 1 neighboring – 6.4 ns – 0p5

FPGA firmware design methodology

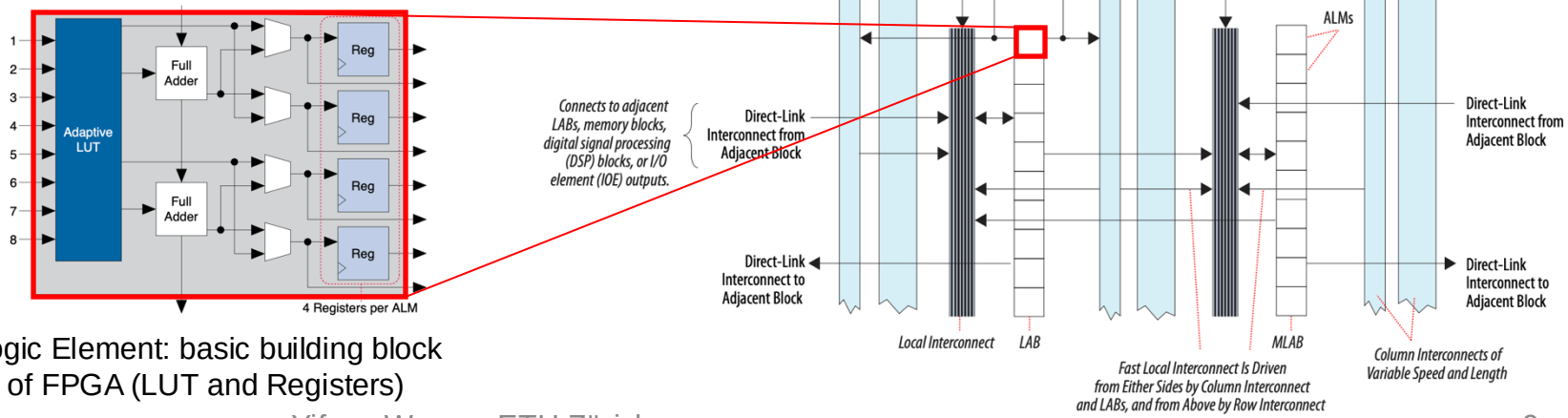
Background

- LE density: from 90nm to 10nm, logic density in FPGA increased exponentially.
- Route-ability: Global routing do not scale well! => long compilation time (hrs+) and low fmax
- Design practice: no global async reset => local sync reset

Evolution of the capacity in logic and memory resources in FPGA devices of the Altera Stratix family



DOI:10.1016/j.compeleceng.2011.09.006

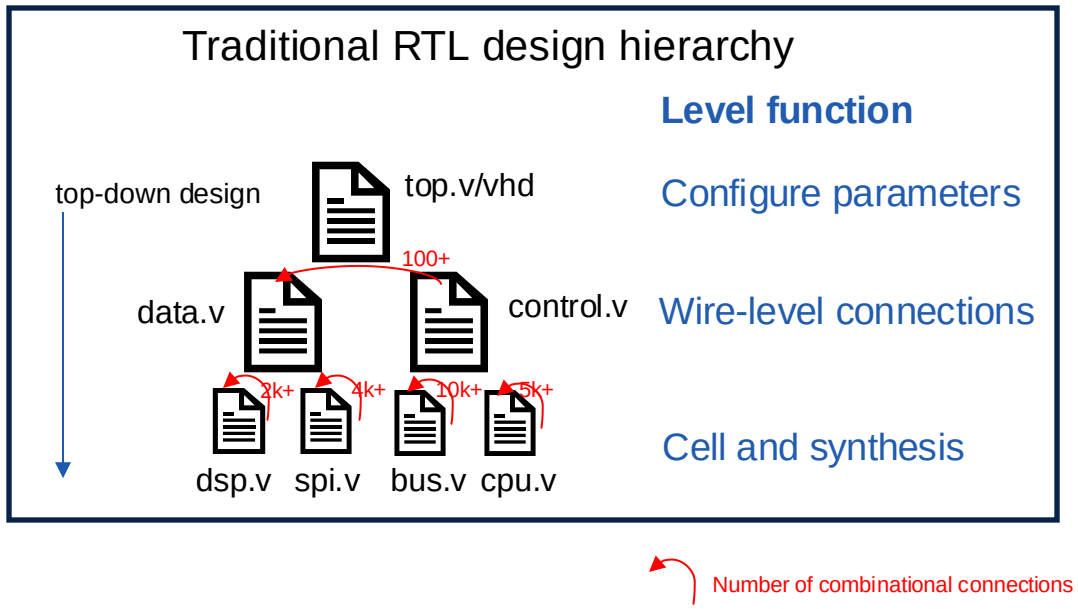


Logic Element: basic building block of FPGA (LUT and Registers)

FPGA firmware design methodology

Drawback

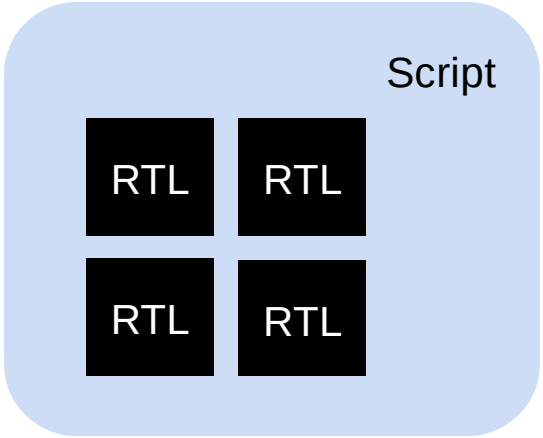
- **Fixed hierarchy**: no elaboration callback to pass information from bottom to top.
- **No explicit boundary**: rely on the practice of individual programmer. Gate clustering.
- **Hard to interconnect**: large number of combinational wires mapped to global wires.
- **Pipelining global wires:** not trivial, manual and fluctuates depending on the random seeds.



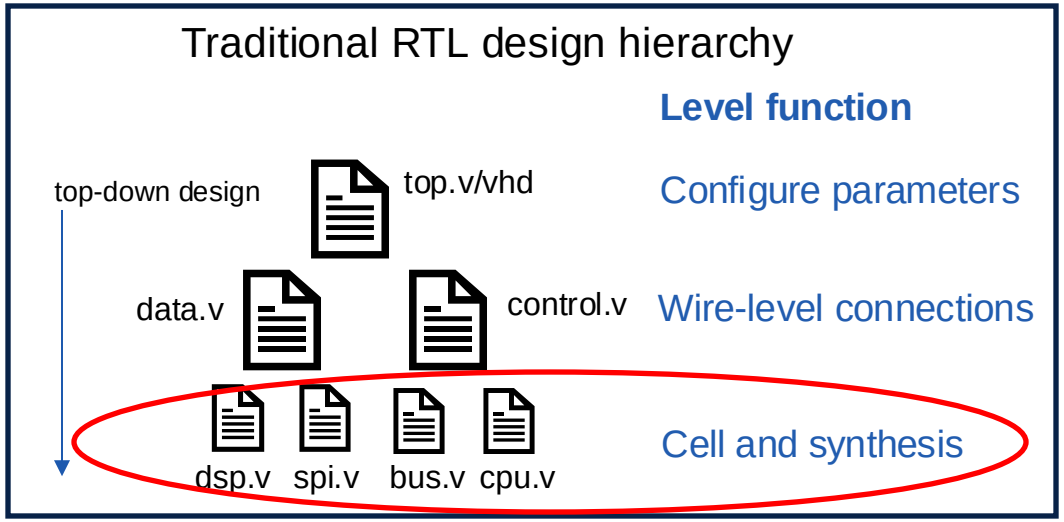
FPGA firmware design methodology

Goal

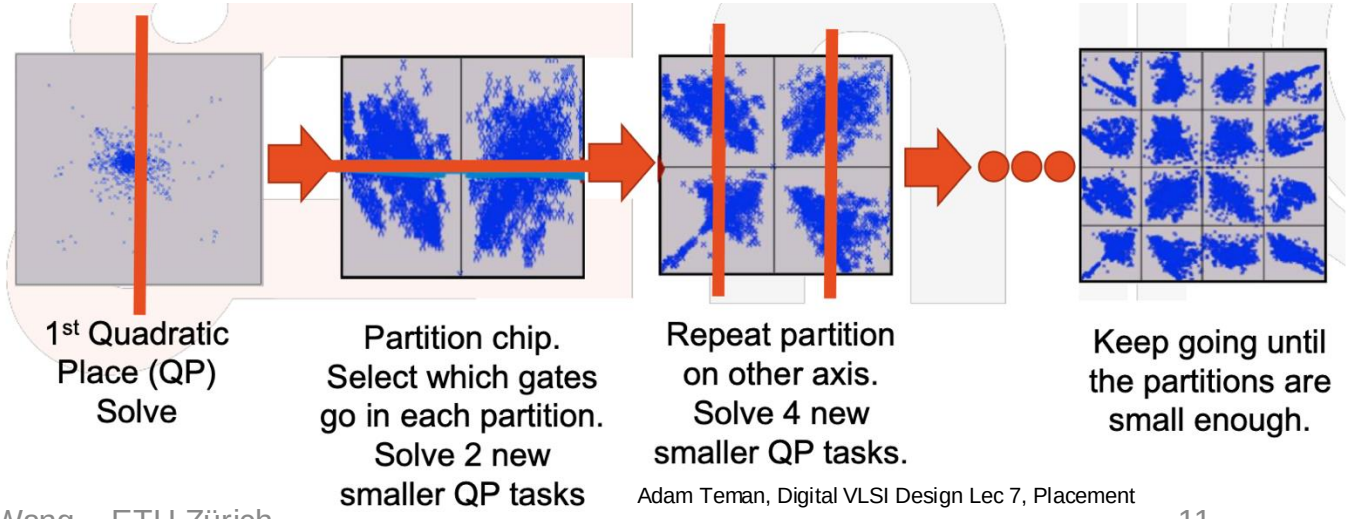
- **System integration tool**: flexible and dynamic configuration.
- **Design partition**: confine designs into small islands and interconnect them.
- **Interoperability**: fine-granularity version control and block design.



System Integration with RTL as black-box and scripting lang. (tcl, python, etc) for configuration and dynamic port connection.



Gate clustering! => extreme compilation time and timing-violation

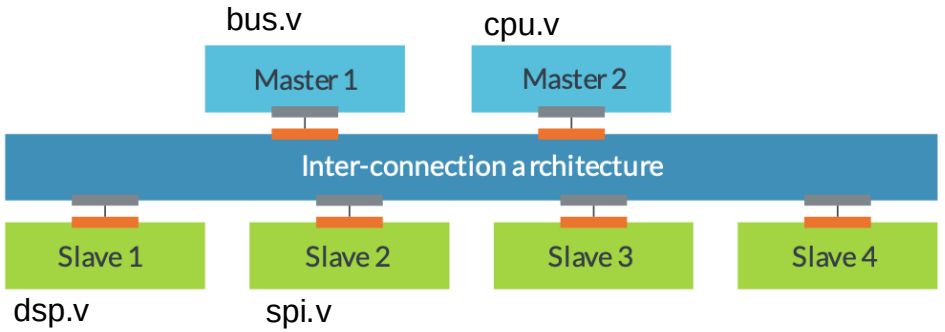


Adam Teman, Digital VLSI Design Lec 7, Placement

FPGA firmware design methodology

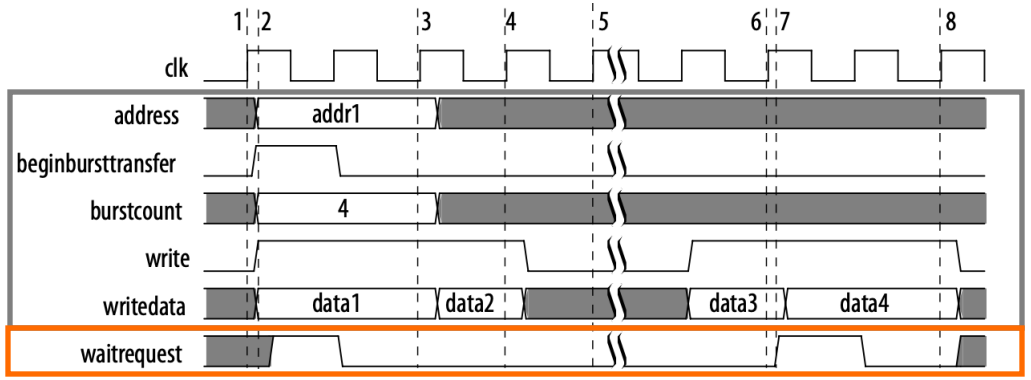
Solutions

- **Network-On-Chip (NOC) interconnect**
  - Packetized transaction
  - Channelized
  - Router-based (pipelined)
  - Handshaking
  - Benefit from Vendor's existing interconnect



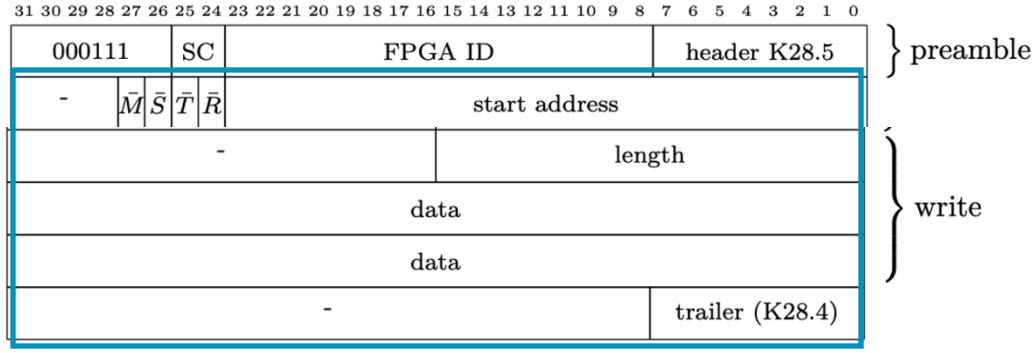
Introduction to AMBA AXI4 - ARM

- Designs are interconnected by NoC
- Data transfer are localized (master<->NoC, NoC<->slave)
- Pipelined for optimal placement and routing



Master <-> interconnect communication

Avalon® Interface Specifications - Intel



Packet across designs (inter-FPGA or within FPGA)

Mu3e Spec Book – Mu3e collaboration

FPGA firmware design methodology

Solutions

- **IP packing / wrapping**
  - Black-boxed small set of RTL files
  - Expose standard Interface (AXI4 or Avalon) for NoC you chose
  - Individual version control as git submodule
  - Interplay across FPGA and systems
  - Easy-for-verification (BFM)

Unique IPs

Mu3e IP Library

- **20+** IP cores (increasing…)
- **open-sourced**
- Fully **verified** on-fpga

IP List

IP Name	IP Description	Status
Slow-Control Hub	Translate the **Mu3e Slow-Control packet** into **Avalon Memory-Mapped** transations.	Release
Onewire Temperature Sensor Controller	Periodically read the temperature sensor with **1-Wire** protocol.	Release
MuTRiG Frame Deassembly	Dismantle the MuTRiG frame into header and hits. Derive individual **hit error** and **frame CRC error**.	Release
CAM (Content Addressable Memory)	Primitive of CAM. Use an template for user to construct their own complex system. *For example, build a CPU-cache, bookkeeping roster, correlator, IP-address to MAC address decoder, etc...*	Minor Debug
MuTRiG Timestamp Processor	Process the timestamp of the MuTRiG (i.e. tracking overflow and mapping **MuTRiG timestamp to Global timestamp**)	Release
Histogram Statistics	Build histogram with update/filter key from selected data segment. Snoop on the data stream. High-performace: SAR bin-calculation and DP-RAM counter.	Release
MuTRiG Controller	Perform **SPI** configuration of the attached MuTRiG(s) and automatically scan the T-Threshold values (use their last configs). Scan results for all channels are stored locally.	Release
Charge Injection	Generate digital pulse with **arbitary** frequency and duration. Use in pair with correct hardware (e.g. **DAB2.1** or older for TDC injection or **DAB2.2** or newer for TDC and analog injection). Targeted to functionally verify the MuTRiG given the test pulse.	Release
Altera Temperature Sensor Controller	Interfacing with the official `alt_temp_sense` IP on **28 nm** device. Store the last result. Can be halted	Release

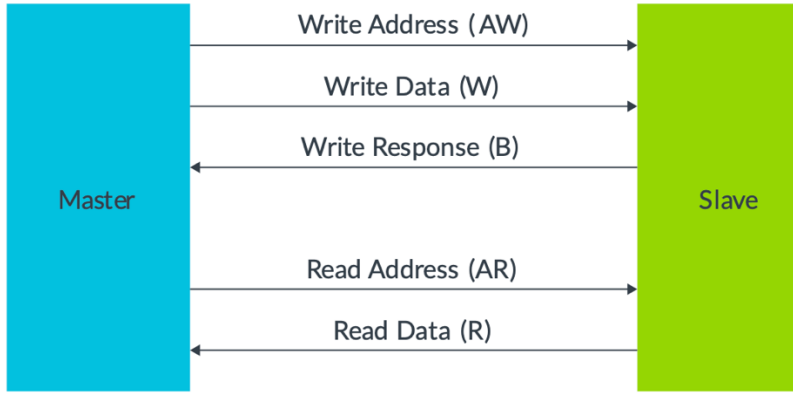
Preliminary at https://github.com/yifeng-ethz/mu3e-ip-cores

Back up

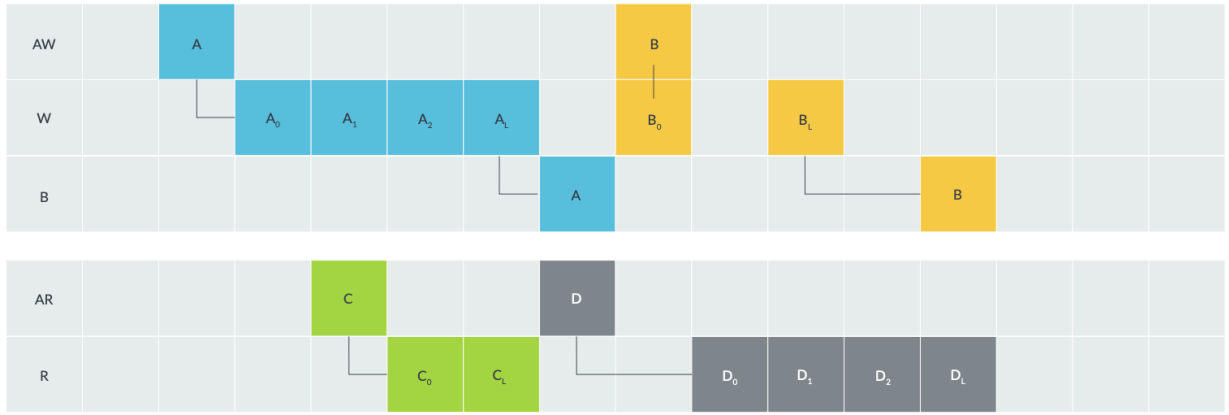
7.1 Examples of simple transactions

Examples of simple transactions help to explain the relationships between the different AXI channels.

The following diagram shows a time representation of several valid transactions on the five channels of an AXI3 or AXI4 interface:



five independent transaction channels
(example from AXI4)



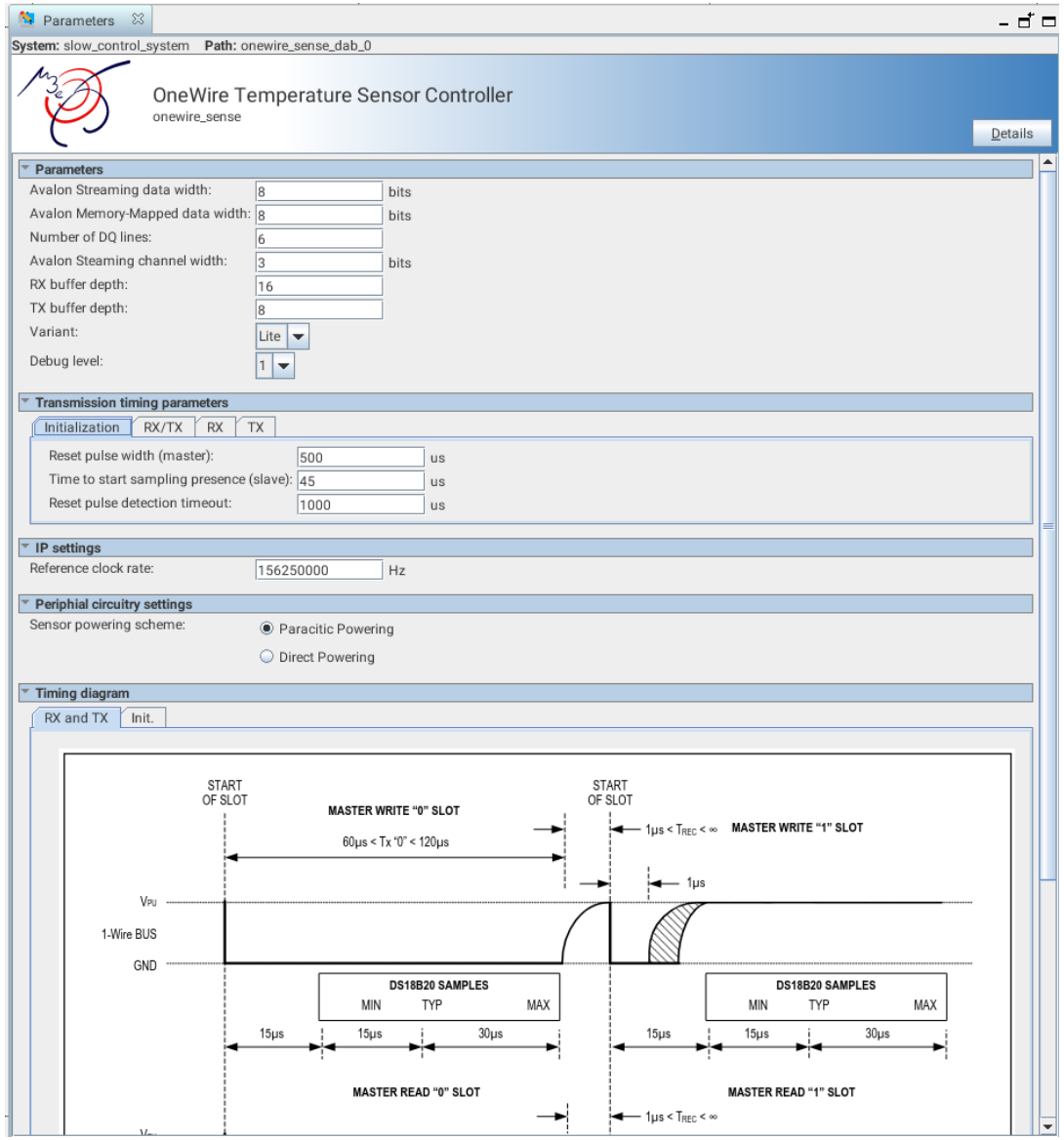
The different transactions in this example are as follows:

1. Transaction A, which is a write transaction that contains four transfers.

   The master first puts the address A on the AW channel, then soon puts the sequence of four data transfers on the W channel, ending with AL where L stands for last.

   Once all four data transfers complete, the slave responds on the B channel.

2. While transaction A was occurring, the master also used the read channels to perform a read transaction, C, which contains two transfers.


Parameters
System: slow_control_system Path: onewire_sense_dab_0
OneWire Temperature Sensor Controller
onewire_sense
Details
Parameters
Avalon Streaming data width: 8 bits
Avalon Memory-Mapped data width: 8 bits
Number of DQ lines: 6
Avalon Steaming channel width: 3 bits
RX buffer depth: 16
TX buffer depth: 8
Variant: Lite
Debug level: 1
Transmission timing parameters
Initialization RX/TX RX TX
Reset pulse width (master): 500 us
Time to start sampling presence (slave): 45 us
Reset pulse detection timeout: 1000 us
IP settings
Reference clock rate: 156250000 Hz
Periphial circuitry settings
Sensor powering scheme:
Paracitic Powering
Direct Powering
Timing diagram
RX and TX Init.
START OF SLOT
MASTER WRITE "0" SLOT
60µs < Tx "0" < 120µs
START OF SLOT
1µs < TREC < ∞
MASTER WRITE "1" SLOT
1µs
VPU
1-Wire BUS
GND
DS18B20 SAMPLES
MIN TYP MAX
15µs 15µs 30µs
DS18B20 SAMPLES
MIN TYP MAX
15µs 15µs 30µs
MASTER READ "0" SLOT
MASTER READ "1" SLOT
1µs < TREC < ∞

ETH zürich

Yifeng Wang
D-PHYS
yifenwan@phys.ethz.ch

ETH Zürich
Inst. f. Teilchen- und Astrophysik
HPK E 25
Otto-Stern-Weg 5
8093 Zürich Switzerland