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## **【359】 Deep Learning-Based Data Processing in Large-Sized Telescopes of the Cherenkov Telescope Array: FPGA Implementation**

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The Large-Sized Telescope (LST) is one of the three telescope types being built as part of the Cherenkov Telescope Array Observatory (CTAO). A next-generation camera that can be used in future LSTs is currently being developed. One of the main challenges is the 1GHz sampling rate baseline. After filtering events, the data rate must be reduced to around 30 kHz.

To achieve such a large reduction, several trigger stages will be designed and implemented in FPGA. The final trigger stage is a real-time deep learning algorithm. We will focus on porting this algorithm to FPGAs by using two different approaches: the Intel AI Suite and the hls4ml packages.

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