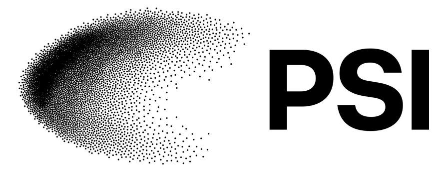
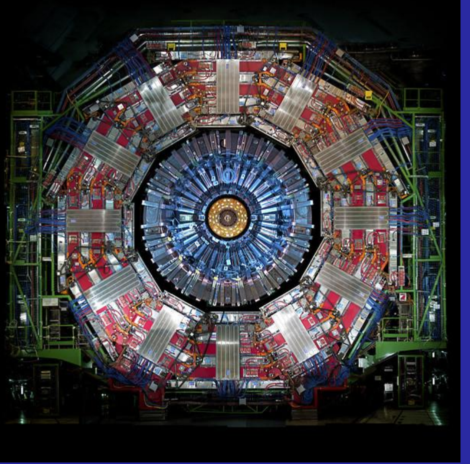


Swiss Physical Society

9 - 13 September 2024, ETH Zürich



TEPX Detector for the CMS Inner Tracker Upgrade: Module Production Status and Plans

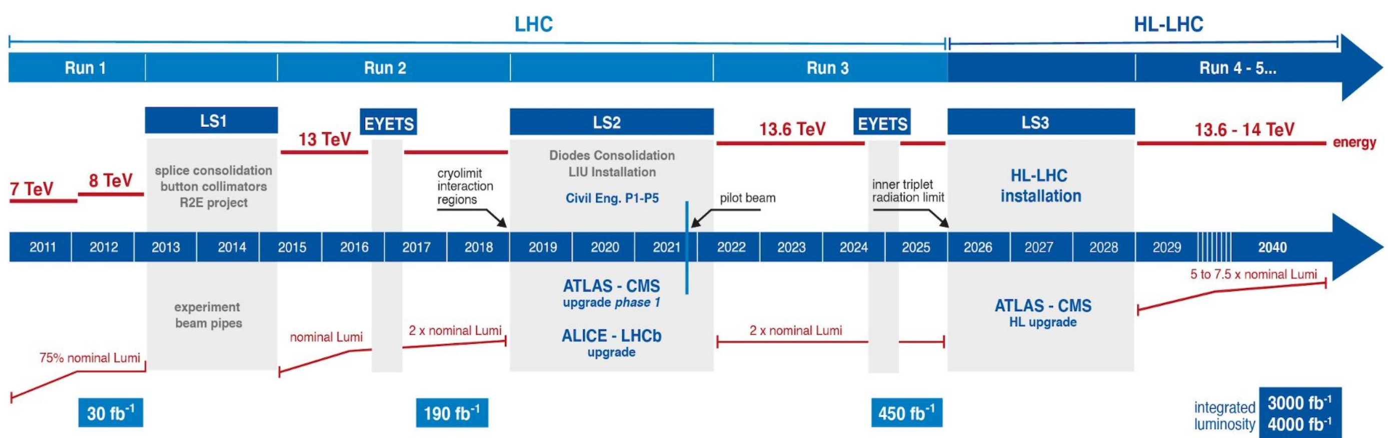
Dr. Amrutha Samalan on behalf of CMS Collaboration,
Paul Scherrer Institute, Switzerland

Overview

- CMS Inner Tracker Upgrade for HL-LHC
- CMS Inner Tracker Layout
- TEPX Detector Layout
- TEPX Hybrid Pixel Modules
- TEPX Module Production
- Recent updates of TEPX module testing and qualification

CMS Inner Tracker Upgrade for HL-LHC

During High Luminosity LHC (HL-LHC) operation, the instantaneous luminosity will be increased to $5\text{-}7.5\times10^{34}\ \mathrm{cm^{-2}\,s^{-1}}$



Increase in the average pileup (50 → 200 pp collisions per bunch crossing) results in:

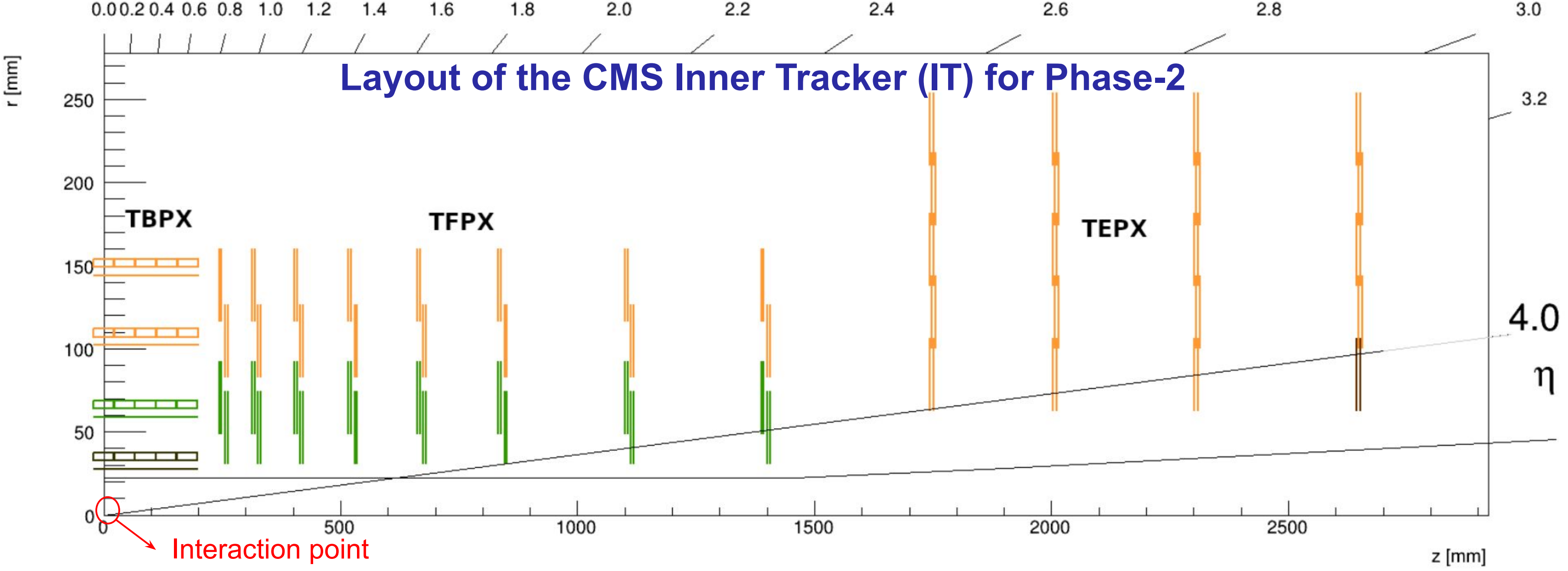
- **Higher hit rate:** up to 3.2 GHz/cm²
- **Longer latency:** 3.2 → 12.8 µs
- **Higher trigger rate:** 100 → 750 kHz
- **Increased radiation:** up to ~1 Grad

  (Fluence of 2.3 x10^16 neq/cm²)

To cope with these challenges CMS is implementing different upgrades of the present systems, including the replacement of the current Inner Tracker (IT) system with an improved one

CMS Inner Tracker Upgrade for HL-LHC

- Increased detection coverage (|η|: 3→4)



- Increased granularity
- Lower detection threshold (new readout chip)
- Reduced material budget (light mechanics, services)

TEPX Layout

8 disks/end;
4 rings/disk

4 disks/end;
5 rings/disk

4 layers

TEPX

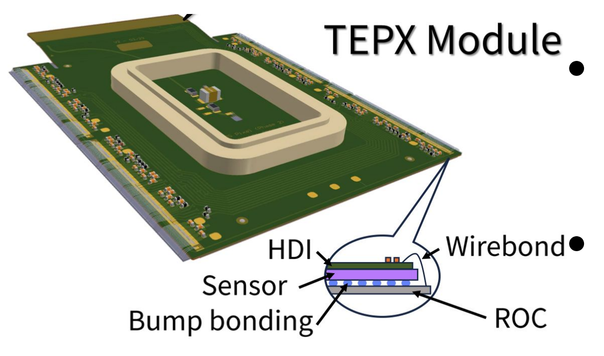
TFPX

TBPX

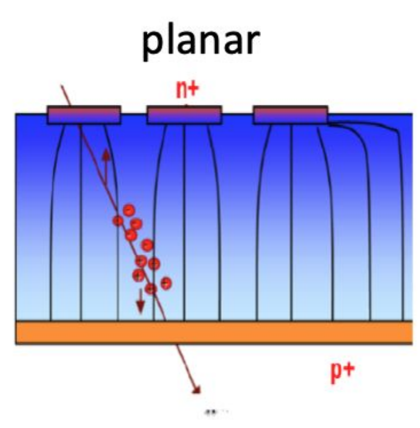
TEPX half-rings

- Total of **eight TEPX disks** in the detector
- Each disk is divided into two halves (known as **Double-Dees)**
- A Double-Dee consists of a front Dee and a rear Dee, mounted back-to-back on a sandwich structure
- Each Double-Dee contains **44 modules**, making a total of **~1,400 modules** for the complete TEPX detector

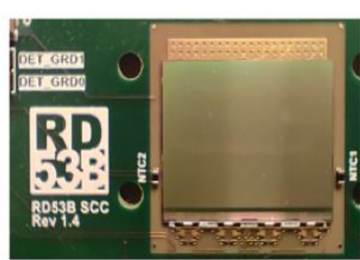
TEPX Hybrid Pixel Modules



- **Planar Si sensors**: 150 μm thickness, n-in-p with 25 x 100 μm^2 pixel size (higher radiation tolerance due to reduced thickness)
- **High-Density Interconnect (HDI)**: glued on top of the sensor and is responsible for **distributing signals and power** to and from the pixel modules, primarily hosts **passive components**, such as decoupling capacitors and connectors



- **CMS Readout Chip (CROC)**



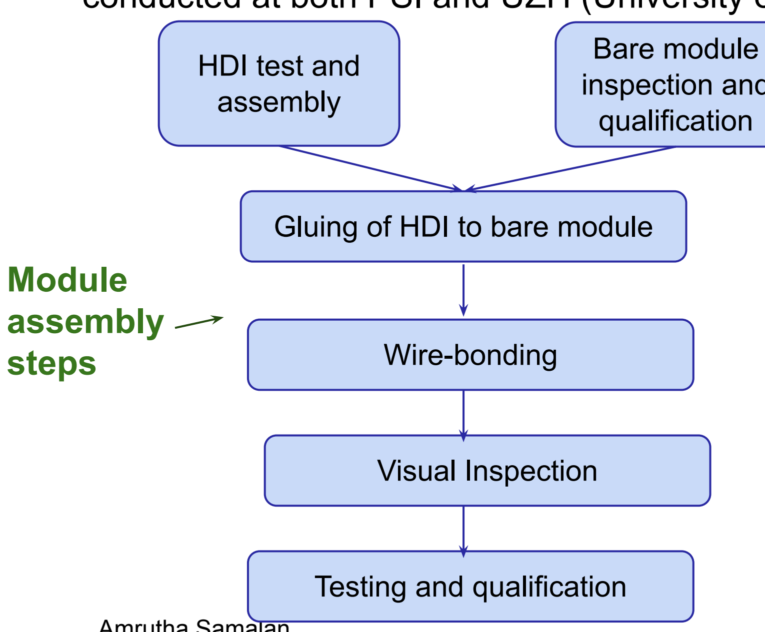
- **CROC 65 nm CMOS ASIC** developed by joint ATLAS-CMS RD53 Collaboration (pixels: 432 x 336; size 21.6 x 18.6 mm^2)
- 50 x 50 μm^2 cell size
- 3.2 GHz/cm² hit rate
- Radiation tolerance up to 1 Grad

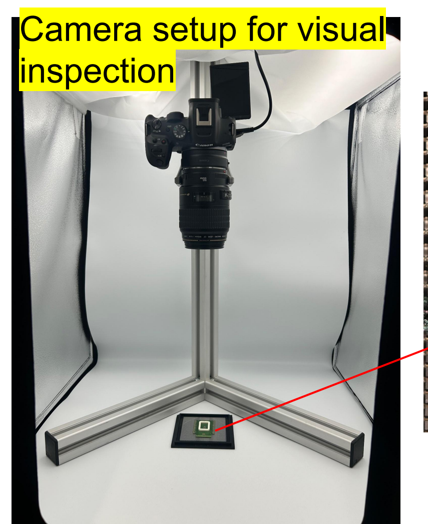
TEPX: one module type with 4 CROCs

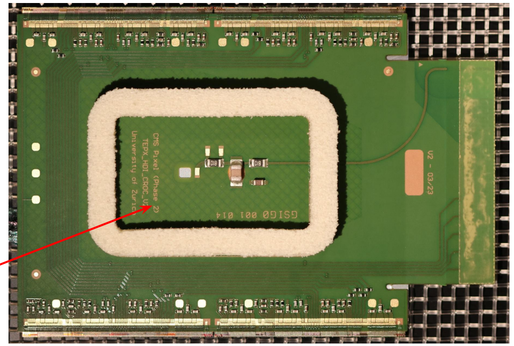
- CROCs on a module are powered in parallel
- Detector modules are powered in series with a current generator

Module Production

- A total of 2000 TEPX modules are planned to be produced
- Kick-off for module production is currently in progress at multiple assembly sites
- PSI is the designated production center for TEPX modules in Switzerland
- Parallel module testing and system validation are actively being conducted at both PSI and UZH (University of Zurich).







TEPX Module

Module Testing and Qualification

- **Quick module functionality test after assembly, including optical inspection**
- **Qualification tests**

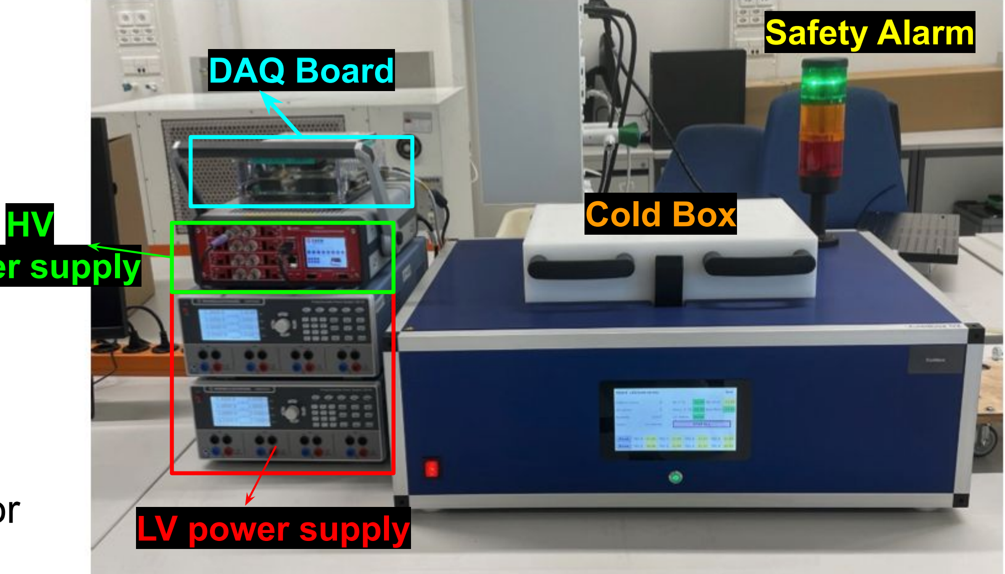
  - IV curves

  - CROC and pixel functionality

  - Bump-bonding

  - Thermal cycling

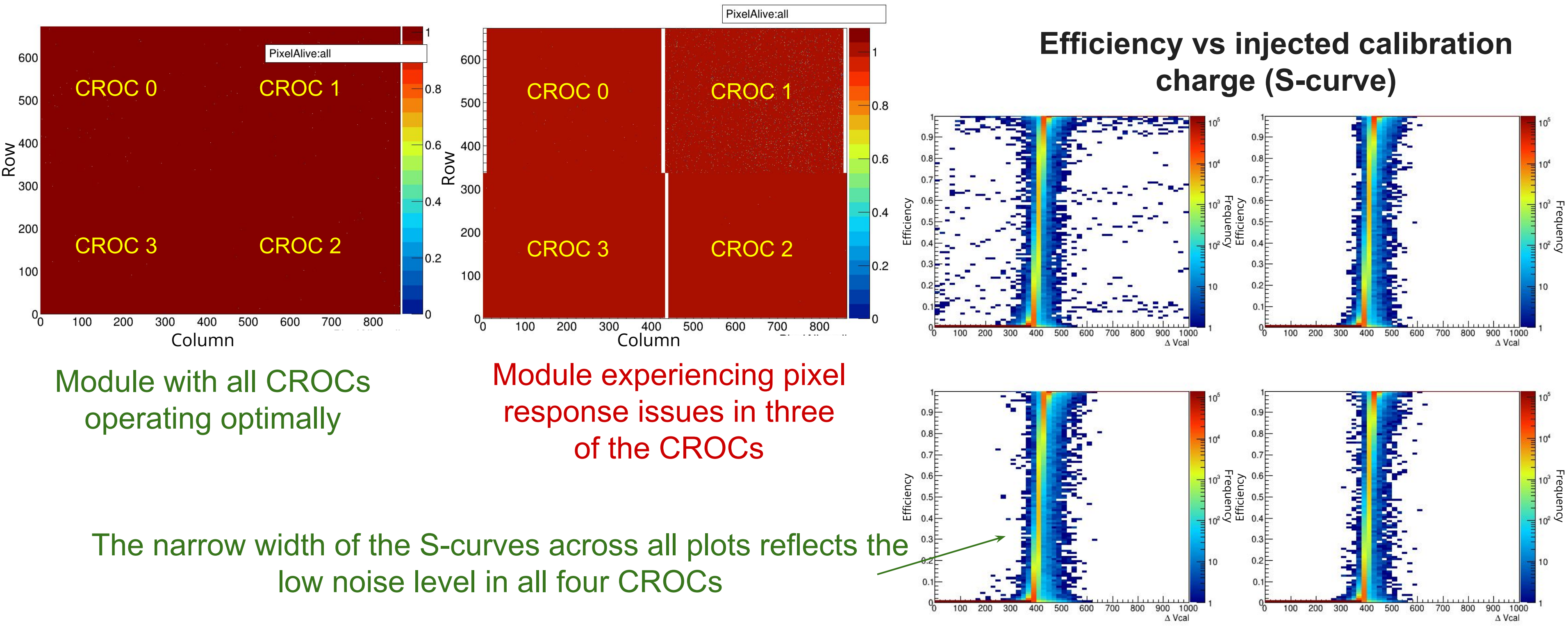
  - High-rate x-ray tests and x-ray calibration for subset of modules



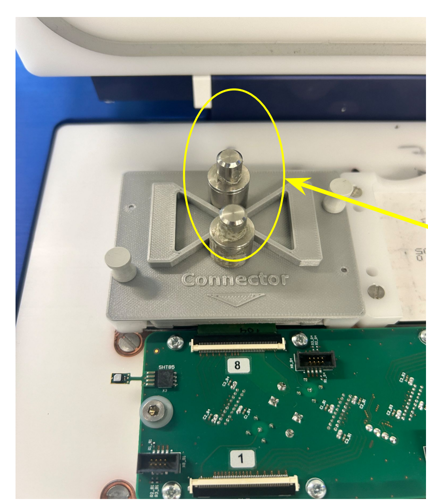
- Several coldboxes operational at PSI and UZH for parallel module testing (8 modules per box)
- Different temperature levels for module testing can be achieved using the coldbox (-4℃ to 20℃)

CROC Configuration Tests

Active pixel scan to identify dead/inactive pixels across the sensor array



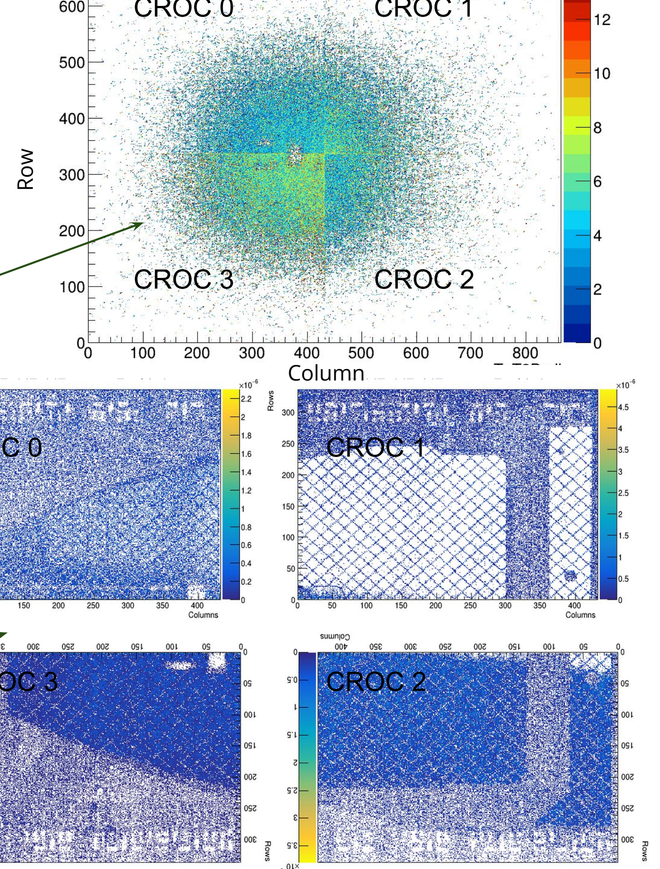
Irradiation Tests



Module functionality tests using two irradiation sources (Sr-90)

Two Sr-90 sources placed on top of the TEPX kick-off module mounted inside the coldbox

Pulse height (ToT) distribution across the module



X-ray high rate tests

Occupancy distribution across the module

HDI High Current Test

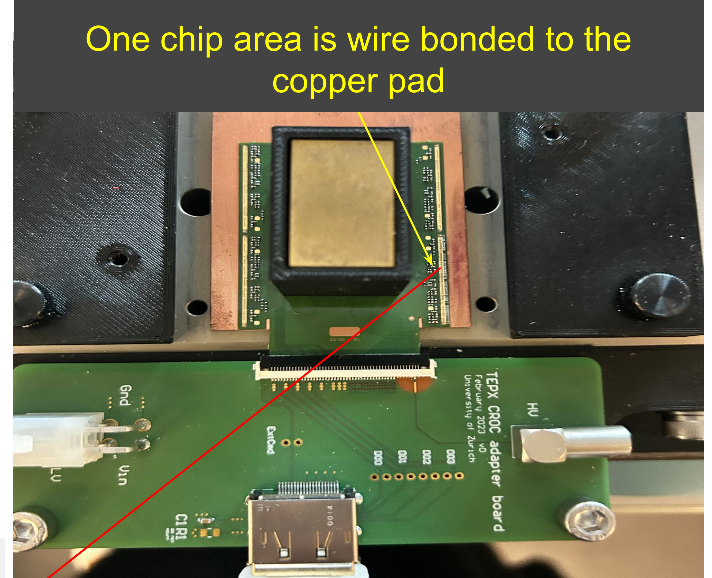
To check the current and thermal tolerance of HDI components and wire-bonds

At current = 8 A -> Temp= 28.3°C

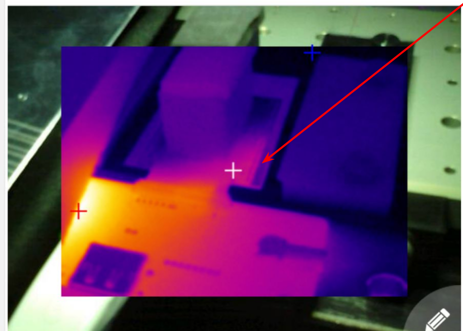
At current = 10 A -> Temp= 32.6°C

*Temperature at other areas= 22°C

8 A for 5 hrs -> No hot points observed

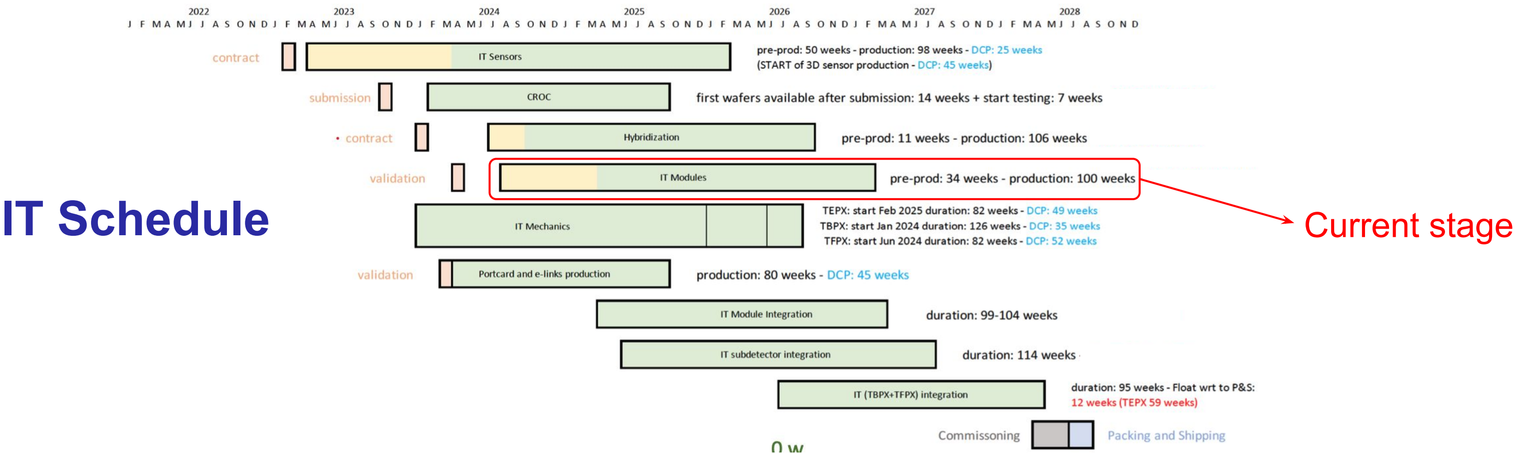


Max : 52,5 °C
Min : 20,9 °C
32,6 °C



Conclusions

- To meet the challenging conditions of the HL-LHC, the current Phase-1 CMS Inner tracker detector will be replaced by the **upgraded and more advanced Phase-2 inner tracker system**
- Increased granularity and extended forward region acceptance from **$|\eta| < 3$** to **$|\eta| < 4$** in the Phase-2 Inner Tracker design



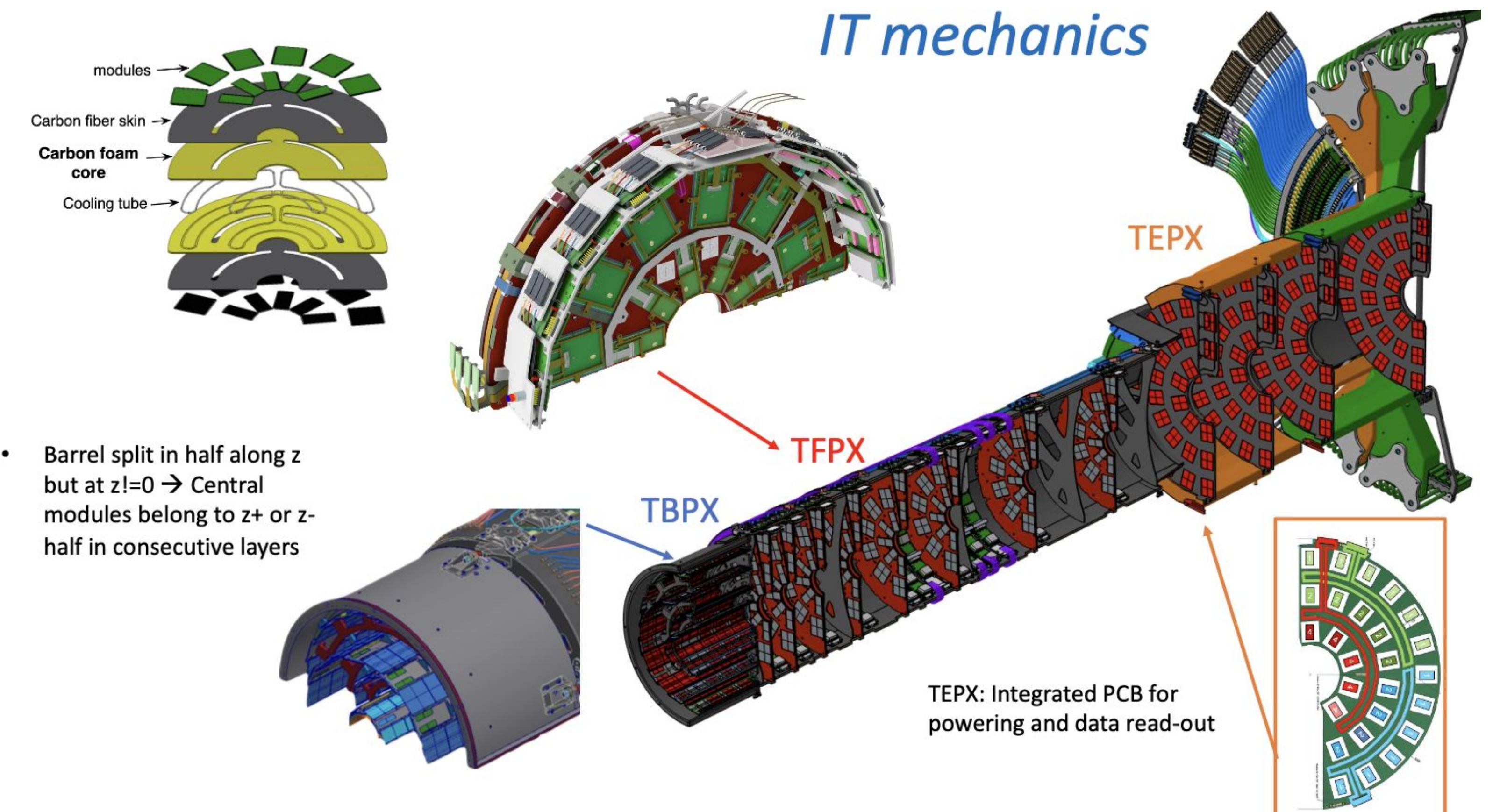
- Currently, pre-production of all the Inner Tracker modules including the TEPX modules is ongoing
- In Switzerland, PSI and UZH are the main assembly/testing centres for TEPX modules
- Recent test results of TEPX kick-off modules are discussed

Thank You

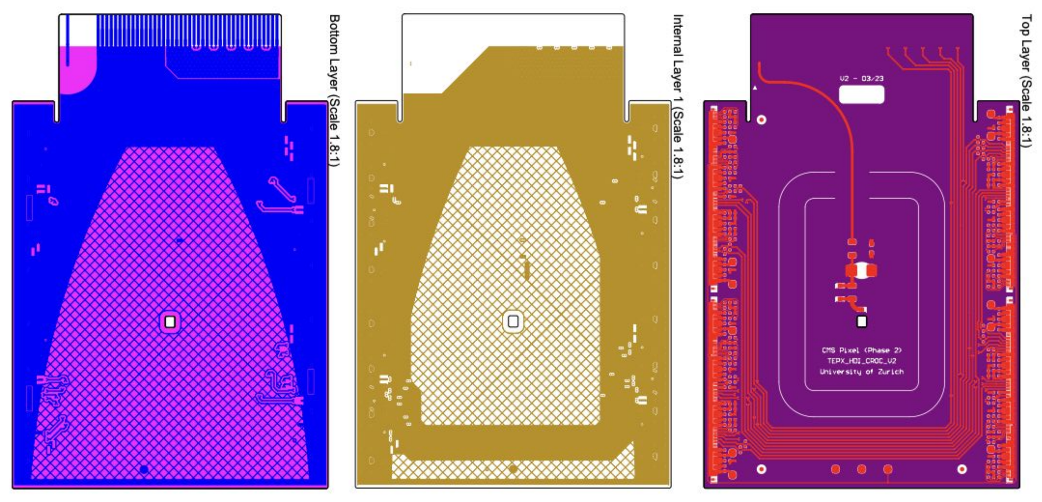
IT Upgrades

	Phase 0	Phase 1	Phase 2
Mechanics	3 layers+ 4 disks	4 layers + 6 disks	4 layers + 24 disks
Inner radius	4 cm	3 cm	3 cm
Active Si area	1 m^2	1 m^2	5m^2
Channels	66M	124M	2000M
Pixel size	100x150 μm^2	100x150 μm^2	25x100/50x50 μm^2
Radiation tolerance	100 Mrad	300 Mrad	1000 Mrad

IT Mechanics



HDI Layers



Coldbox Layout

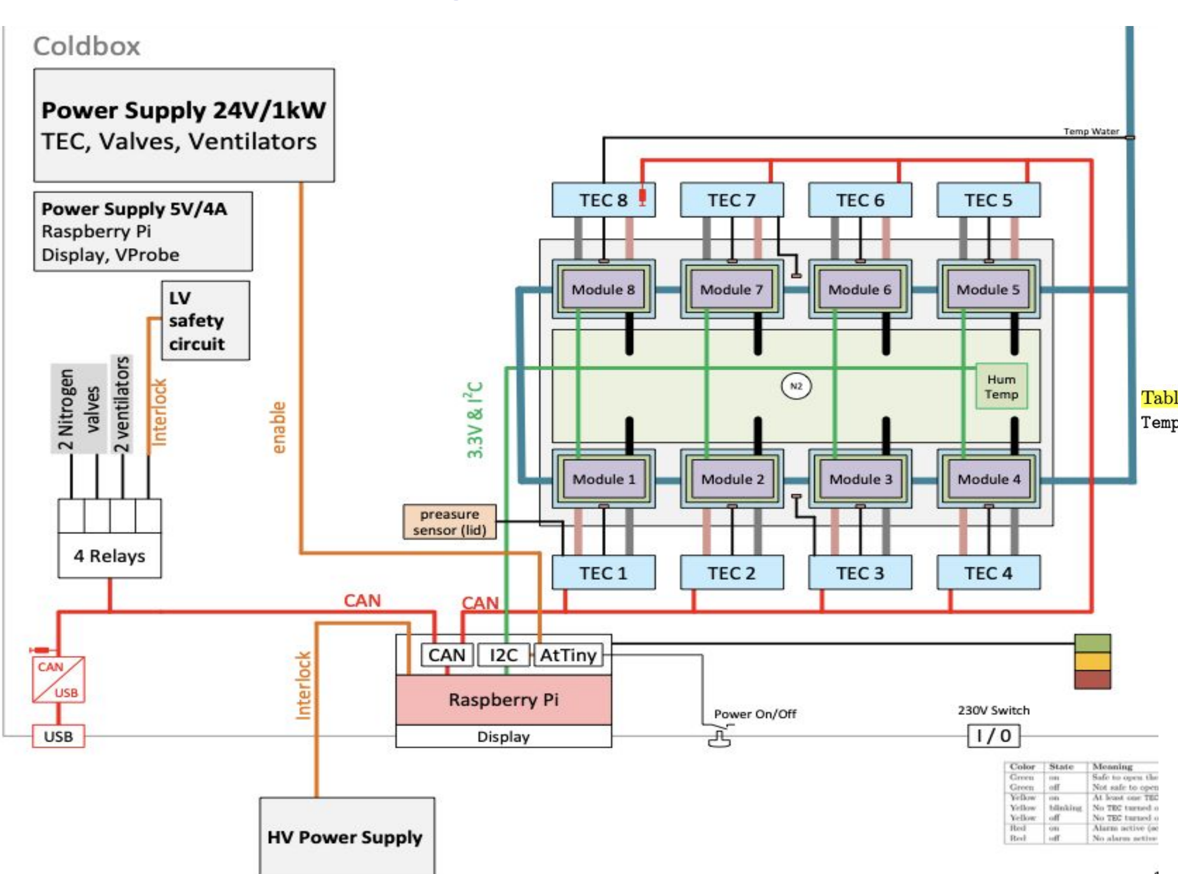


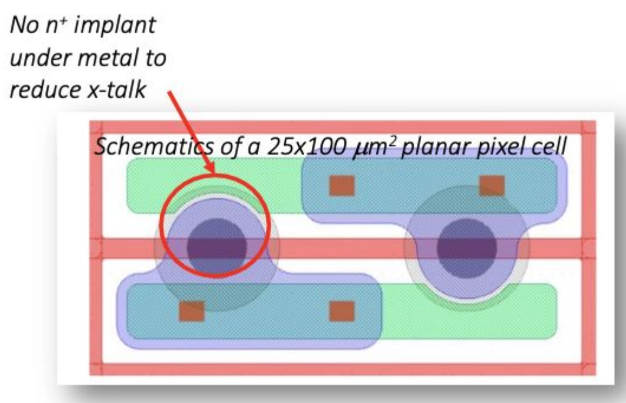
Table 4: Approximate translation between ControlVoltage_Set and PT1000 temperature Temperature_M, with the temperature measured on a powered HDI.

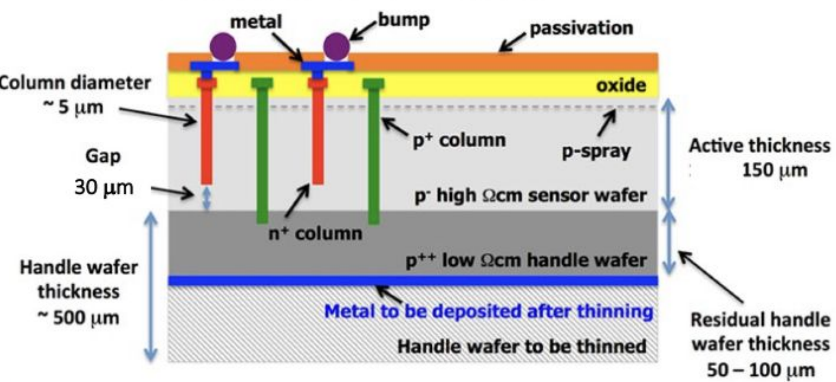
ControlVoltage_Set [V]	Temperature_M [°C]	HDI temperature [°C]
1	20	35–38
2	15	30–35
3	7	20–25
4	0	15–20
5	-4	12–17

TEPX Sensor

- 150 μm bulk thickness, 25x100 μm² pixels cells everywhere
- Planar n-in-p sensors:
  - Bias up to 600V and spark protection between ROC and sensors
  - Three vendors qualified in the Market Survey, Tender being closed in these days
- Bump bonding pattern is 50x50 μm²
  - Cross-talk issues studied and minimized (i.e. bitten implant on planar)

- 3D sensors for barrel L1
  - Short drift distance ~50 μm (3D) vs 150 μm (Planar)
  - Slim edges (150 μm) vs planar (~450 μm) → smaller dead zone
  - Sensors produced at FBK on 6" wafers and CNM on 4" wafers



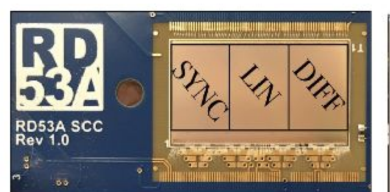


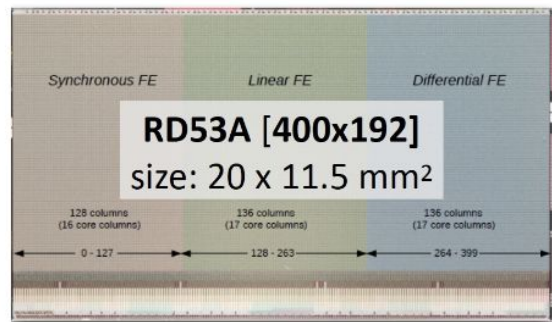
CMS CROC

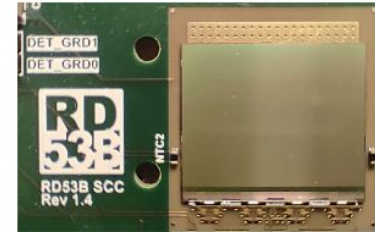
Designed by the RD53 collaboration

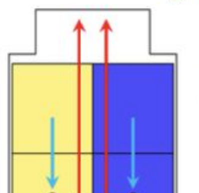
- 65 nm CMOS technology (current detector 250 nm)
- Radiation hard at least up to 0.5 Grad
- 50 x 50 μm^2 pixel size
- 4 data links per chip at 1.28 Gb/s using Aurora encoding
- "Linear" analog input
  - Krummenacher feedback for return to baseline and leakage current compensation
- Digital readout with Time over Threshold
- Column readout, data encoding
- Data merging: read-out of up to three secondary chips through a primary one in the same module

→ reduction of data line in low-occupancy layers



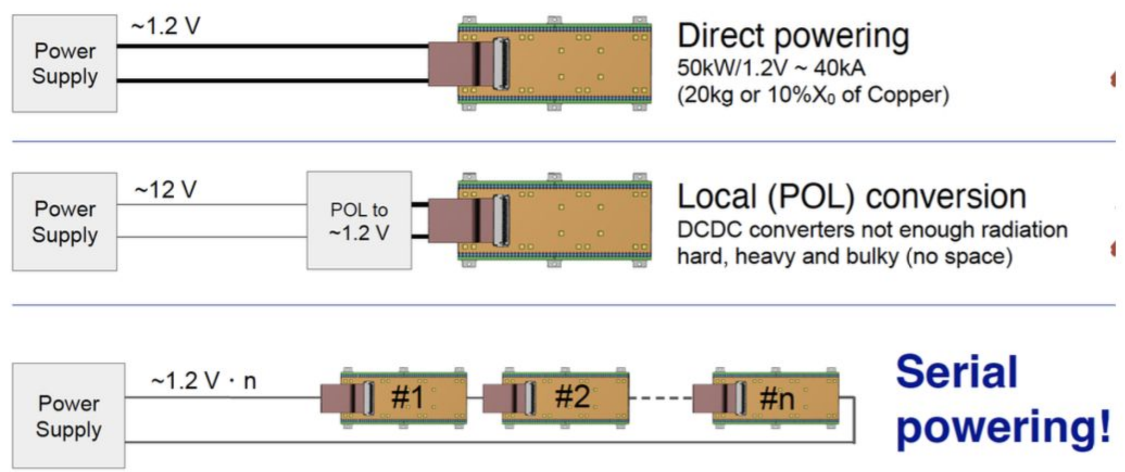


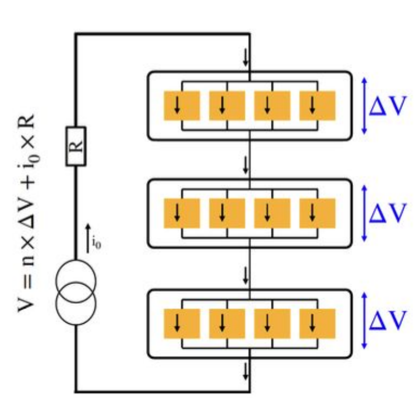




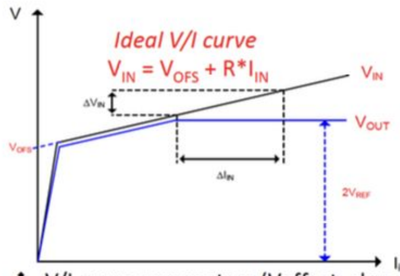
- Serial power scheme of the Inner Tracker is based on a ShuntLDO regulator on chip

Serial Powering





- Only serial power is compatible to the HL-LHC conditions for IT
- Serial power not sensitive to voltage drops → does not pose stringent requirements on R → low mass cables
- Current is shared in parallel between two (double) or four chips (quad) inside the same module
- All chain elements see the same current if they represent the very same and constant load → Shunt LDO
- The most demanding chip in the chain determines the power to be delivered



- V/I curve parameters (Voffset, slope) defined by external resistors
- V_{OUT} tunable by chip configuration