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【304】Timing measurement ASIC using LGAD for possible HL-LHC upgrade

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The Compact Muon Solenoid (CMS) experiment at CERN will undergo a major upgrade for the high-luminosity phase of the LHC (HL-LHC) starting in 2029. In addition to improving the detector rate capabilities and performance at higher luminosities, precision timing measurements are added to mitigate pile-up effects. We plan the extension of the timing capabilities to cover the full tracker acceptance up to $\eta = 4$ using Low Gain Avalanche Detectors (LGAD).
Here, we present the design efforts towards a readout Application-specific integrated circuit (ASIC) capable of operating with LGAD pixel detectors. It is designed in a 28 nm CMOS technology, to process efficiently the signals from the LGADs.

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