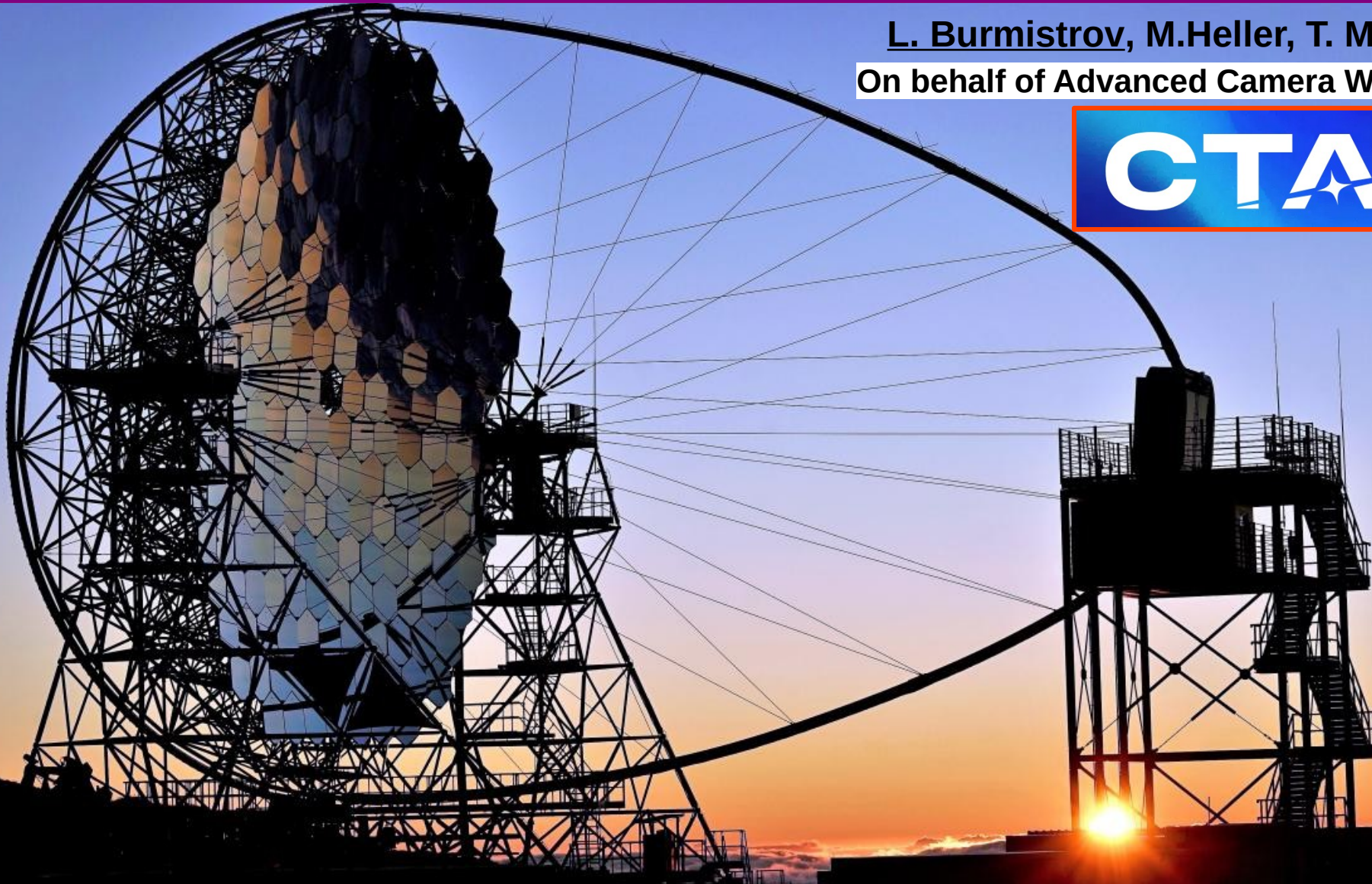


The next generation cameras for the Large-Sized Telescopes of the Cherenkov Telescope Array Observatory

Annual Meeting of SPS 9-13 September 2024, ETH Zurich

L. Burmistrov, M.Heller, T. Montaruli
On behalf of Advanced Camera WG of LST

The logo for the Cherenkov Telescope Array Observatory (CTAO). It features the letters 'CTAO' in a bold, white, sans-serif font. A stylized white starburst or lens flare is positioned between the 'A' and 'O'. The logo is set against a blue rectangular background with a thin orange border.

→ Introduction

Cosmic rays and extensive air showers.

The Large – Sized Telescopes (LSTs) for gamma ray detection.

→ LST photo sensitive camera.

The current Photo-Multiplier Tube (PMT) - based camera.

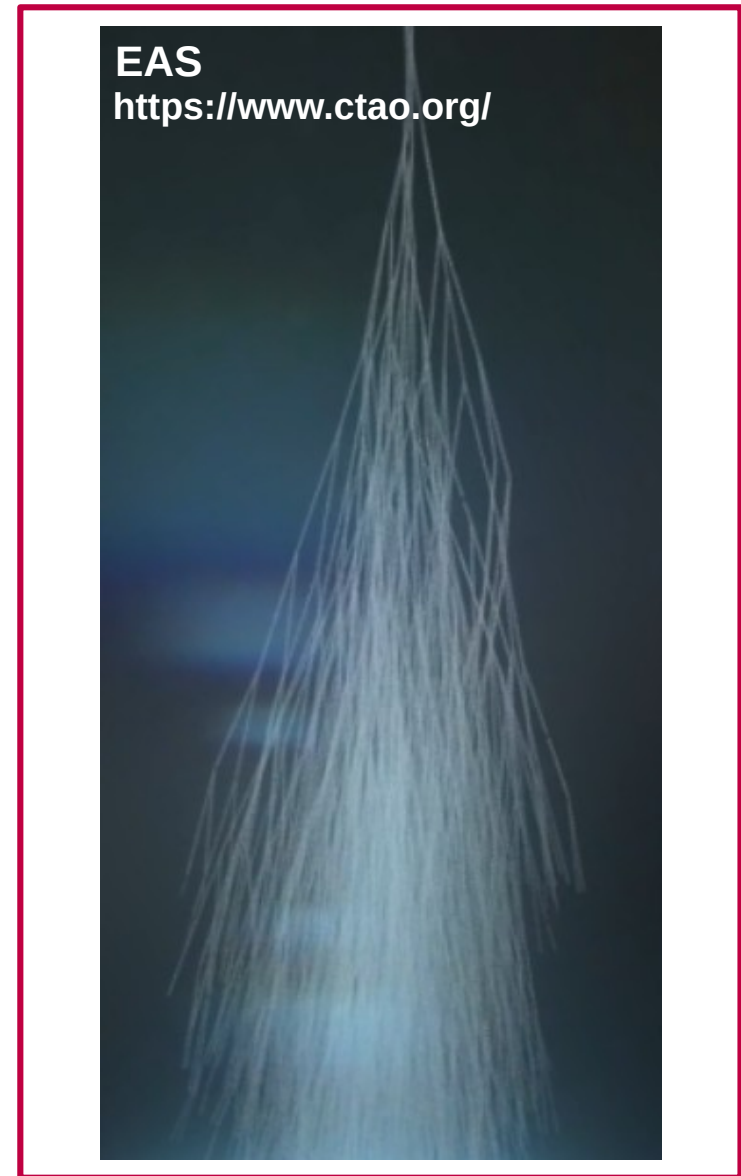
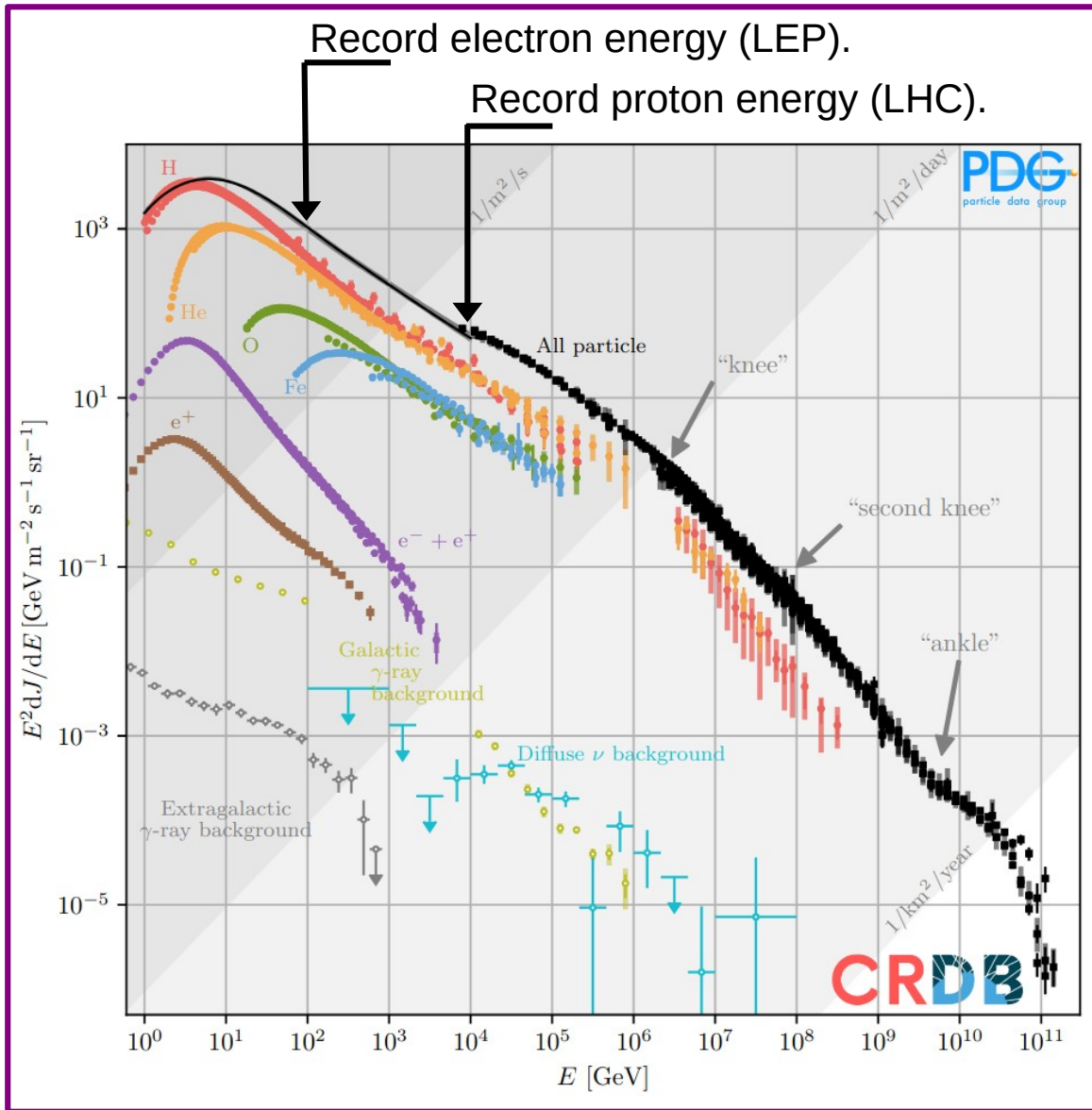
The advanced camera: next generation of LST cameras based on silicon photo-multipliers SiPMs

- Night sky background mitigation

- Readout chain and light sensor

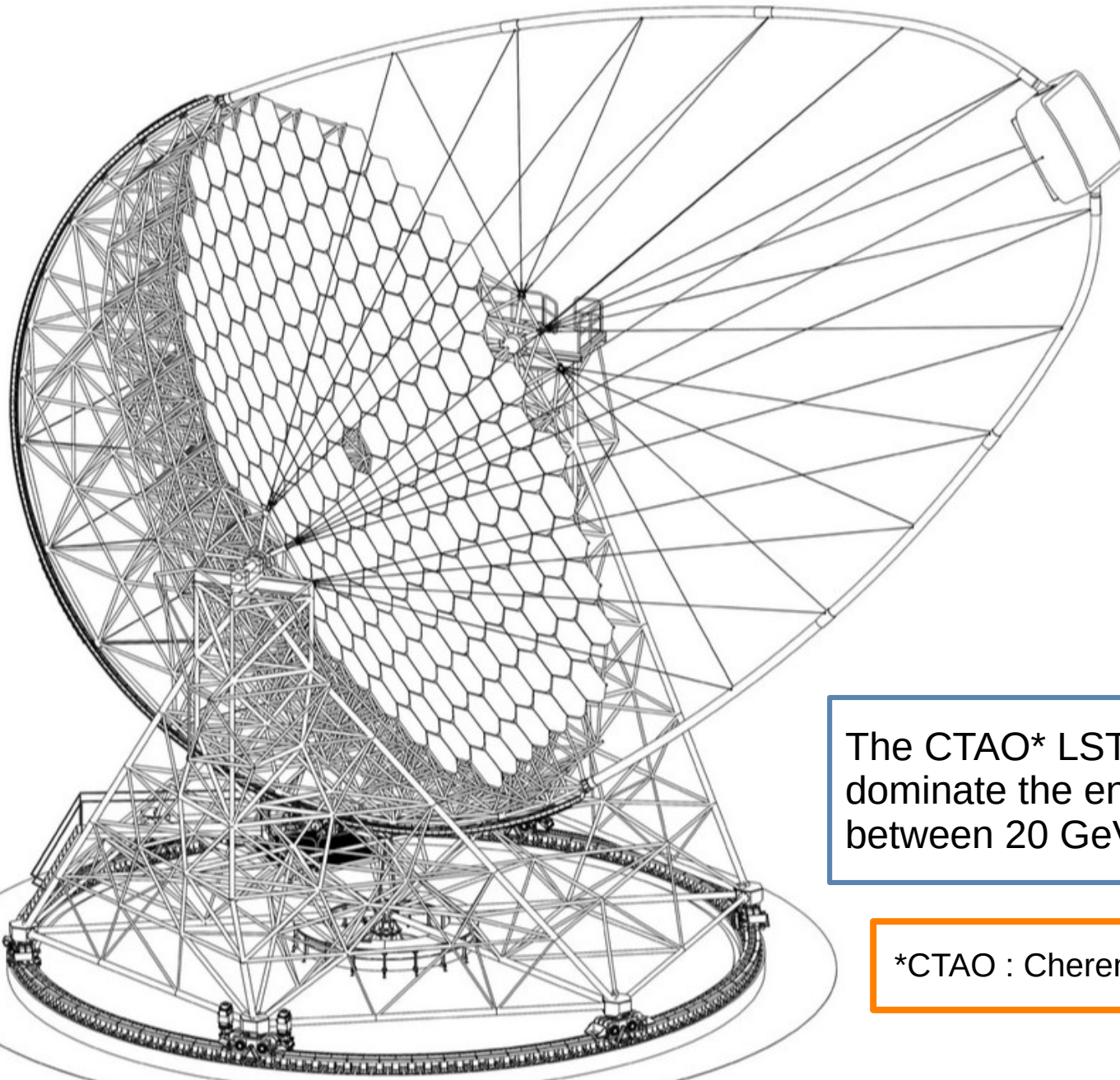
- Data volume reduction with digital sum and DBSCAN.

L. Giangrande (UNIGE), D. Gascón, R. Manera (UB), P. Altet, X. Aragones, S. Gómez,
D. Mateo (UPC)
Y. Uzun, K. Yldirim, B. Efe, E. Charbon (EPFL)
M. Bellato, F. Marini (INFN/Padova)
M. Barcala, G. Martinez, J. Sastre (CIEMAT)
M. J.A Barrio, A. Pérez, L. A. Tejedor (UCM)



The cascade of secondary particles initiated by a single primary particle will produce Cherenkov photons in the atmosphere, primarily generated by electrons, positrons, and muons. This light can be detected by Cherenkov telescopes.

The Large – Sized Telescop the Cherenkov Telescope for gamma ray detection



Parabolic mirror

198 hexagonal mirrors
~1.5 m flat to flat size

Dish diameter 23 m

Mirror area ~ 400 m²

Focal Length 28 m

Field of view ~ 4.4°

Design on-axis PSF 0.05°

Design off-axis PSF 0.11°

The CTAO* LSTs are in an array of 4, will dominate the energy region of the sensitivity between 20 GeV and few 100 GeV.

*CTAO : Cherenkov Telescope Array Observatory

proton_gamma.gif

The LST camera

PMT - based camera

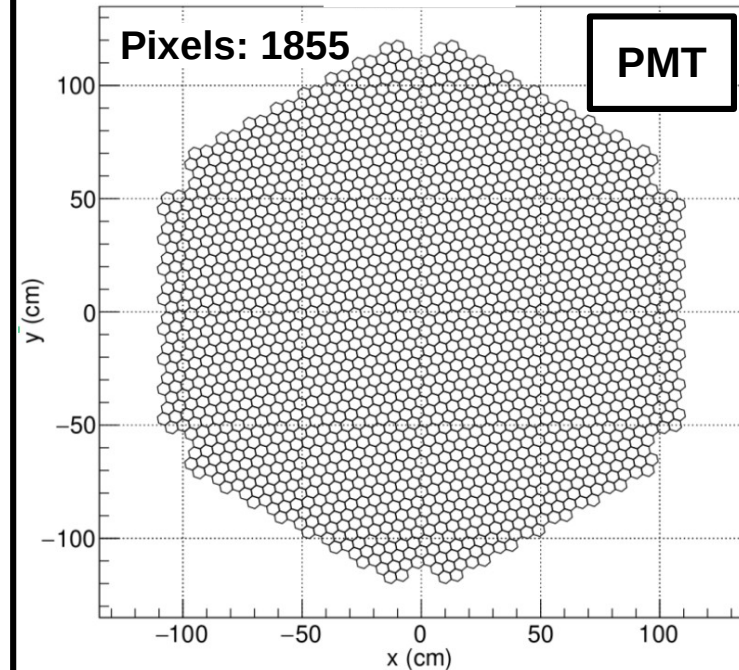
Number of pixels	1855
Pixel field of view	0.1°
Pixel linear size	~50 mm
Analogue memory DRS4 ASIC developed in PSI	
Analogue buffer length	4 μ s
Readout rate	7.5 - 15 kHz
Dead time	5 % at 7.5 kHz

Operates at low gain* 4×10^4

Two readout chains with low and high gain amplifiers

PMTs are coupled to light guides

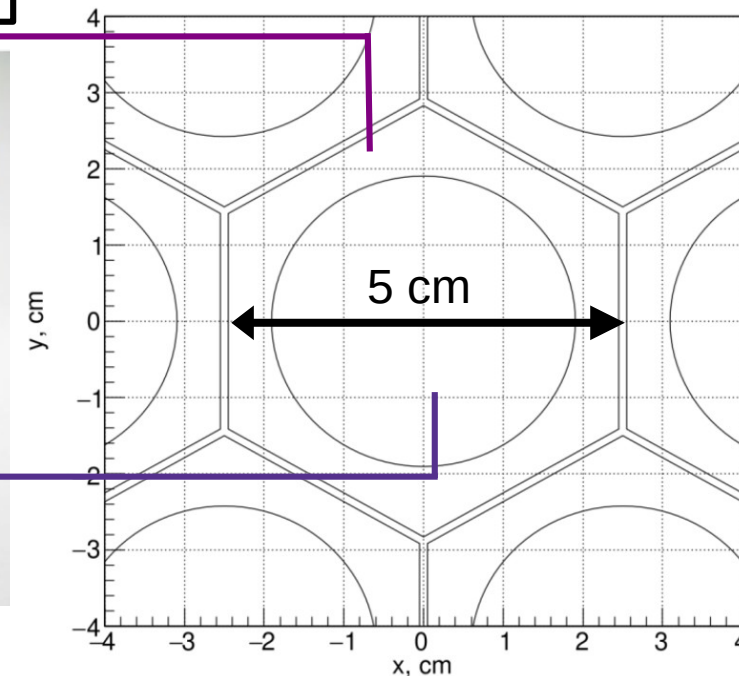
* To ensure the PMT lifetime for 10 years of operation



Light guide for PMTs



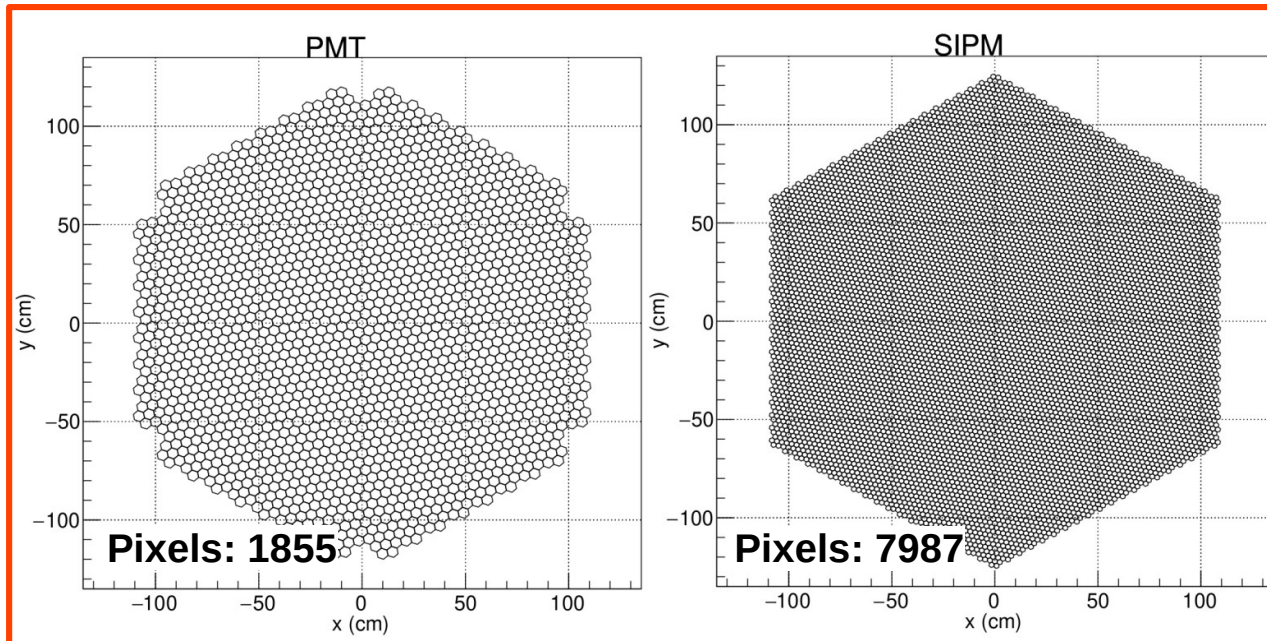
PMT Bias voltage 850-1500 V



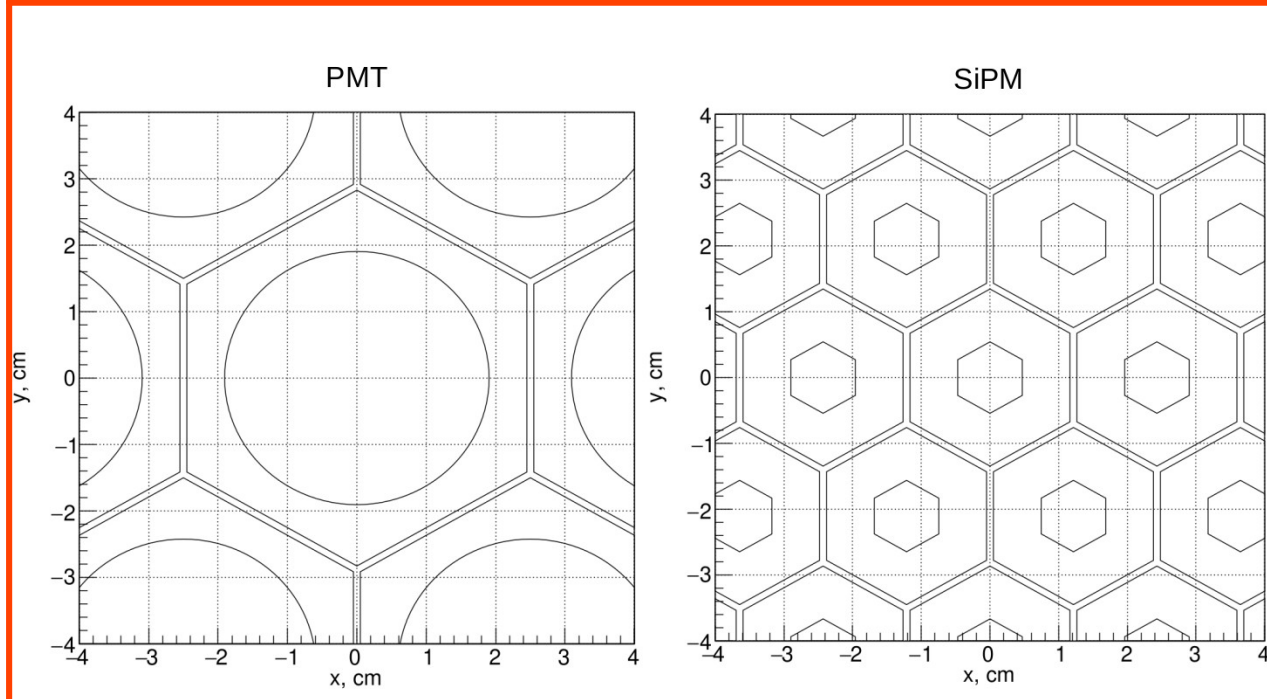
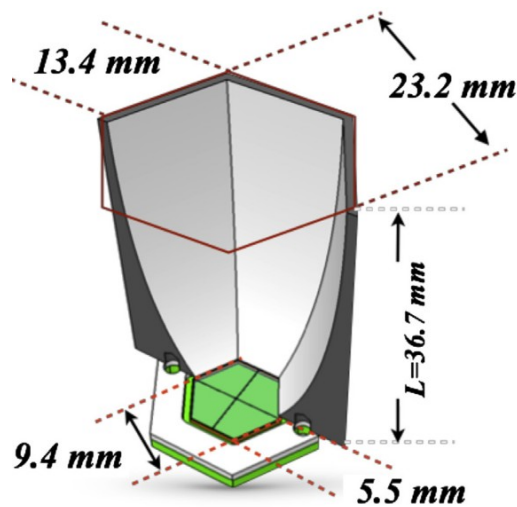
Silicone Photo-multipliers camera for LST

SiPM

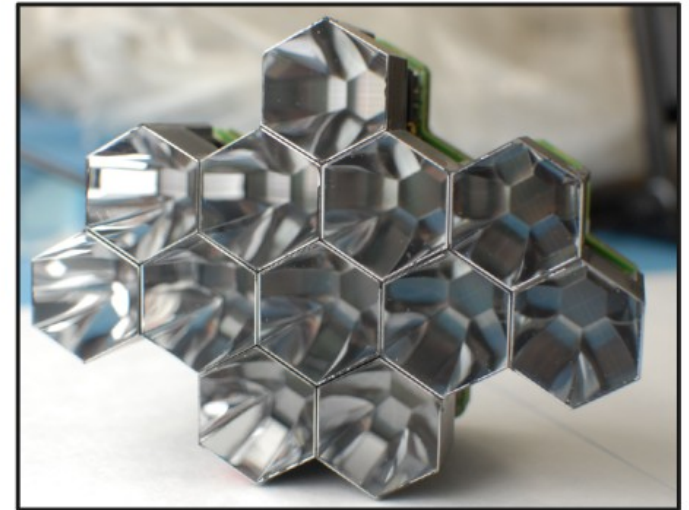
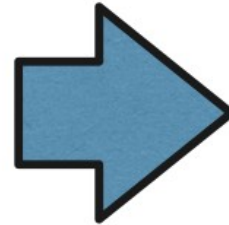
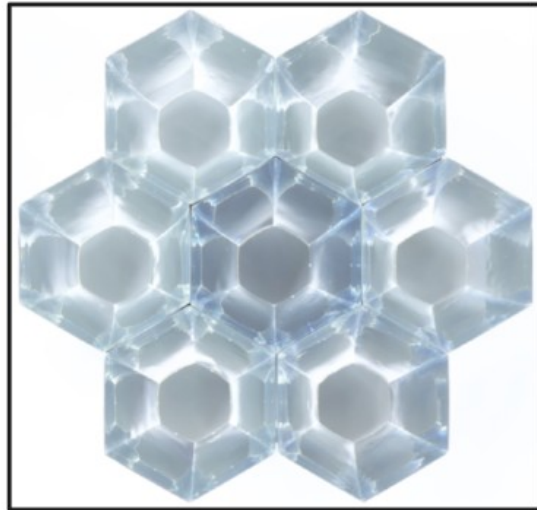
Number of pixels	7987
Pixel field of view	0.05°
Designed on-axis PSF	0.05°
Pixel linear size	~25 μm
Digital buffer length	~4 μs
Readout rate	7.5 - 30 kHz
Dead time	better than 5 %
Single readout chains with one gain	
SiPMs are coupled to the light guides	



SiPM camera detects twice as much light as PMT ones.

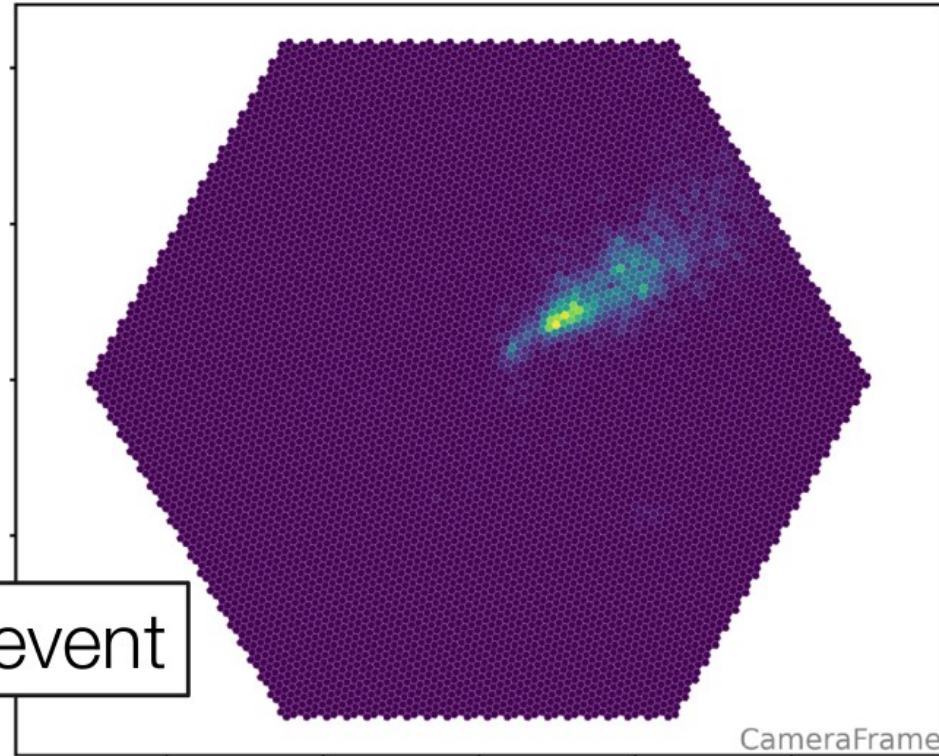
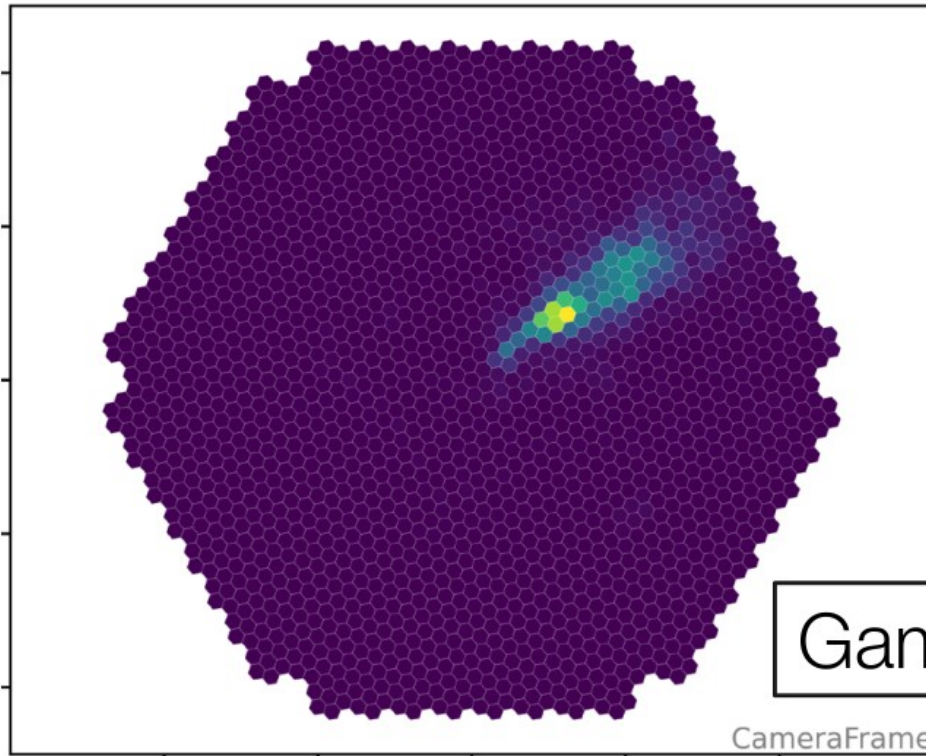


The LST PMT camera to LST SiPM camera



LST PMT camera (**0.1°**)

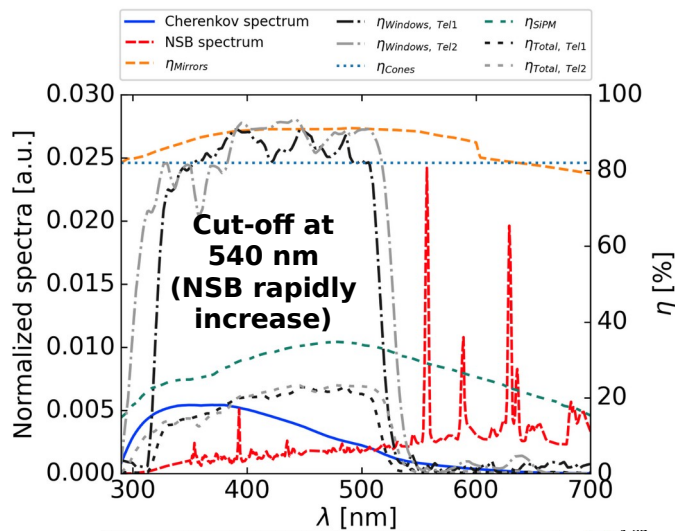
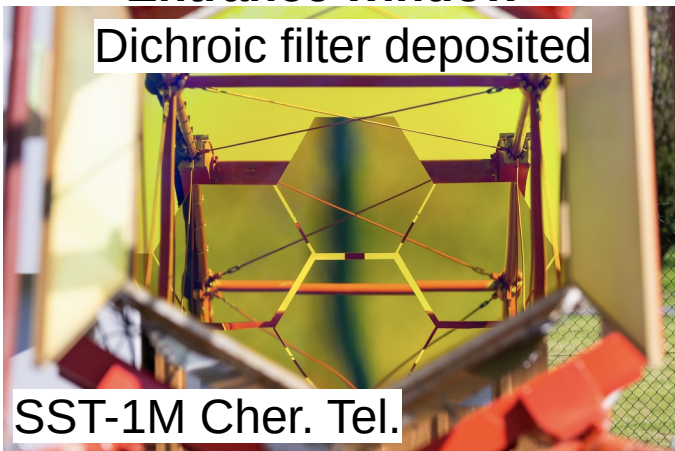
LST SiPM camera (**0.05°**)



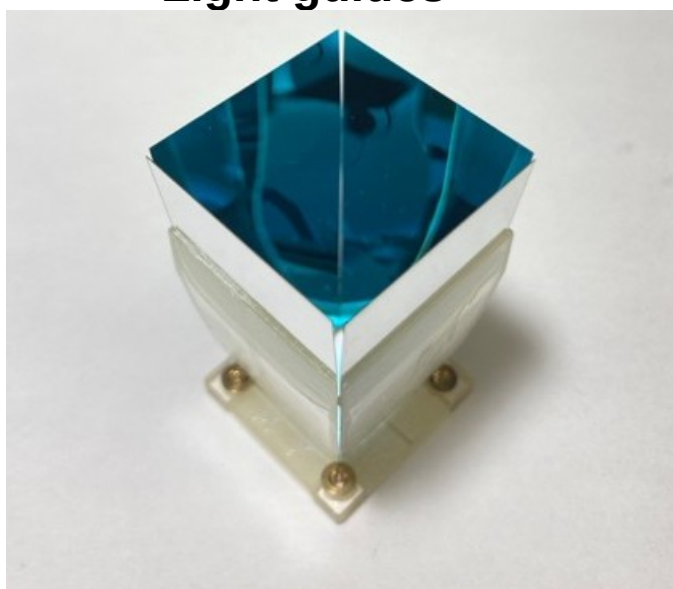
Gamma event

Various options to filter night sky background

Entrance window



Light guides

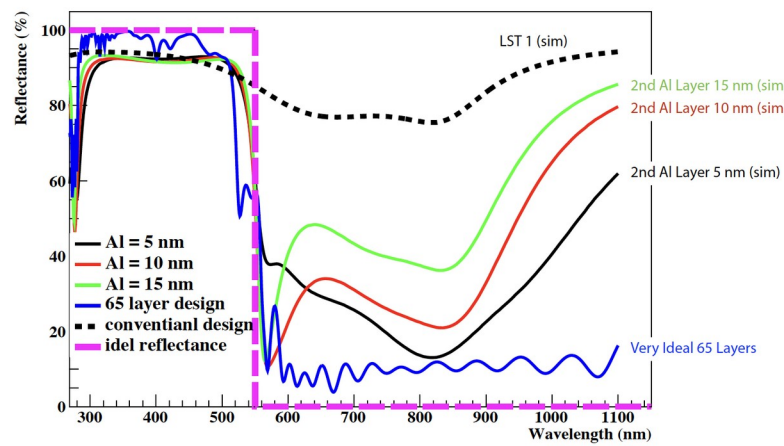
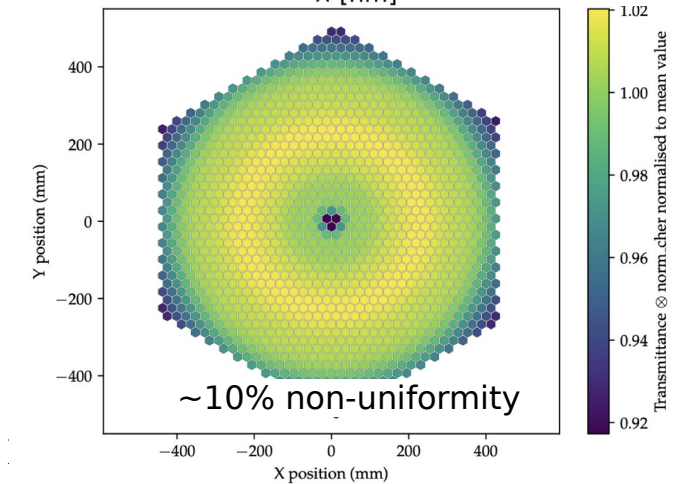
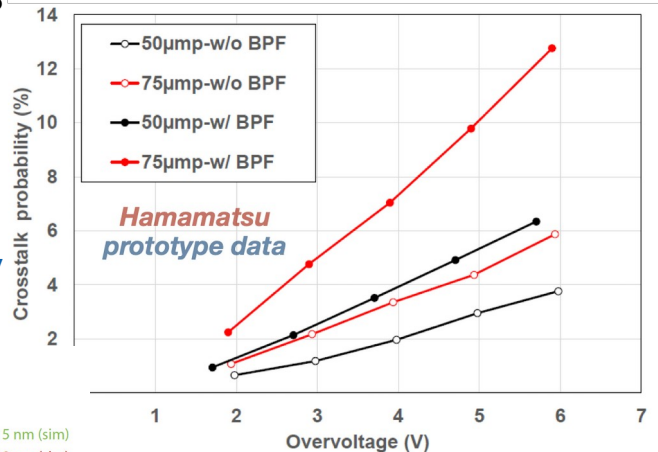
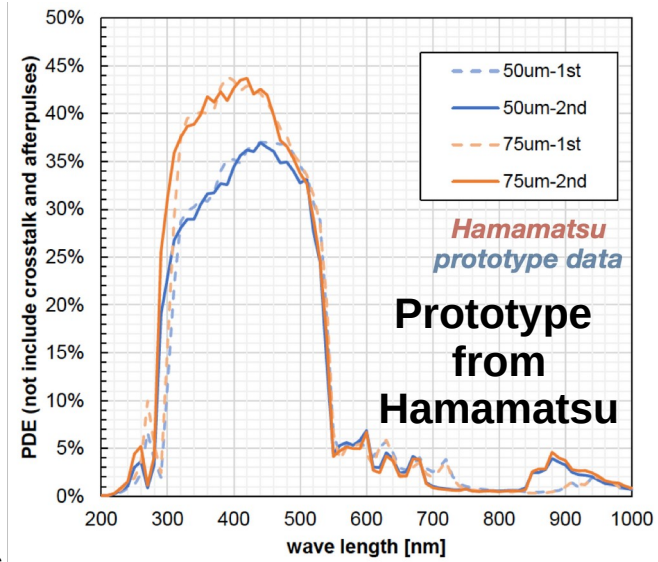


80% of the light undergoes reflections in the light guide

Having "blue" light guides improves NSB rejection, about 40% absorption > 540 nm

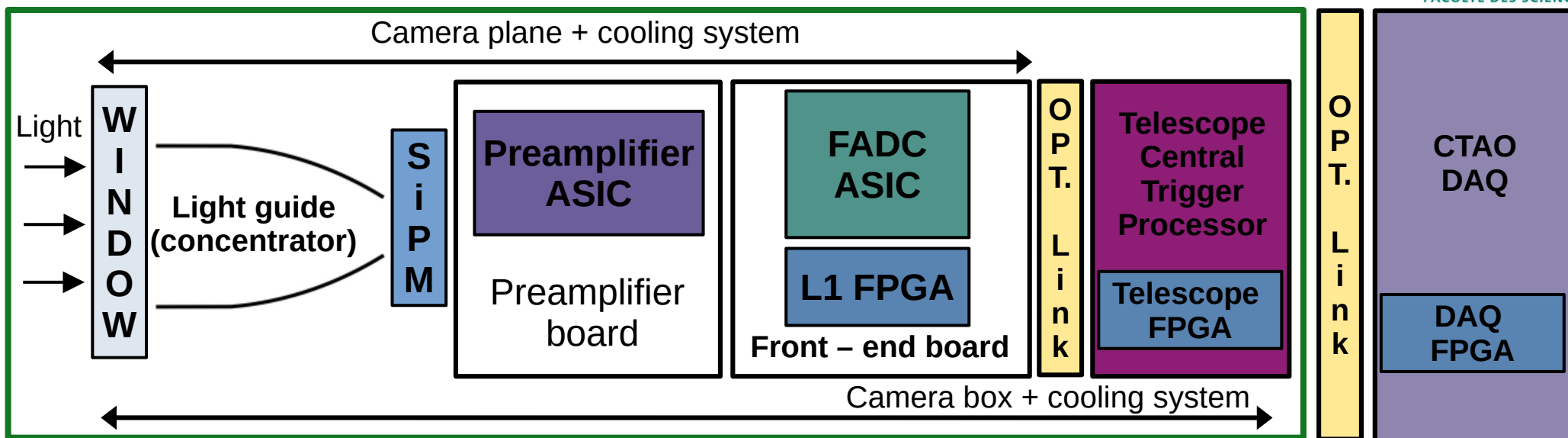
ICRR, University of Tokyo, Kyoto University
Konan University, ISEE, Nagoya University

Sensors



Dichroic filter done directly on the bare silicon surface

Very uniform but increases optical cross talk



Preamplifier board:

Provides biases to SiPM and slow control (temperature, currents ...)
SiPM raw signal amplification (x 10 times – single p.e. 3 mV).

Front – end board:

Digitize the amplified signal with FADC (flash ADC) 12 bits, ~1 Gbps (in total ~100 Tb/s).
L1 FPGA store in the buffers the waveforms
L1 FPGA calculates the digital sum on waveforms (see next slide)
First stage of data volume reduction or Level 1 trigger.

L1 FPGA

Telescope Central Trigger Processor:

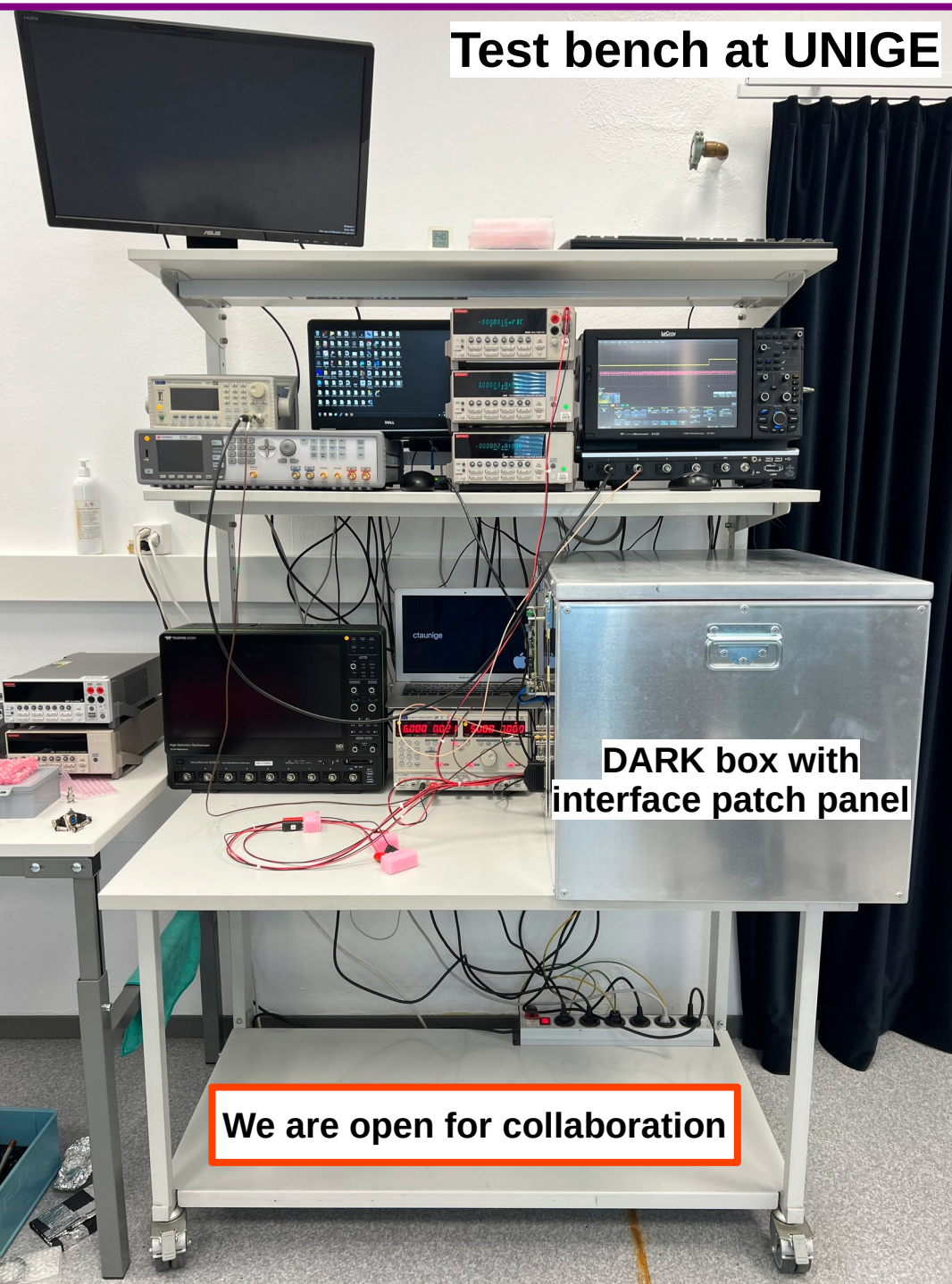
Manage L1 trigger coincidences with other LSTs. If a coincidence is found, the L2 trigger runs
- DBSCAN
- AI trigger (See Tjark's talk)

Telescope FPGA

CTAO DAQ: If the L2 trigger returns true, the further online analysis can run. (See Iaroslava's talk)

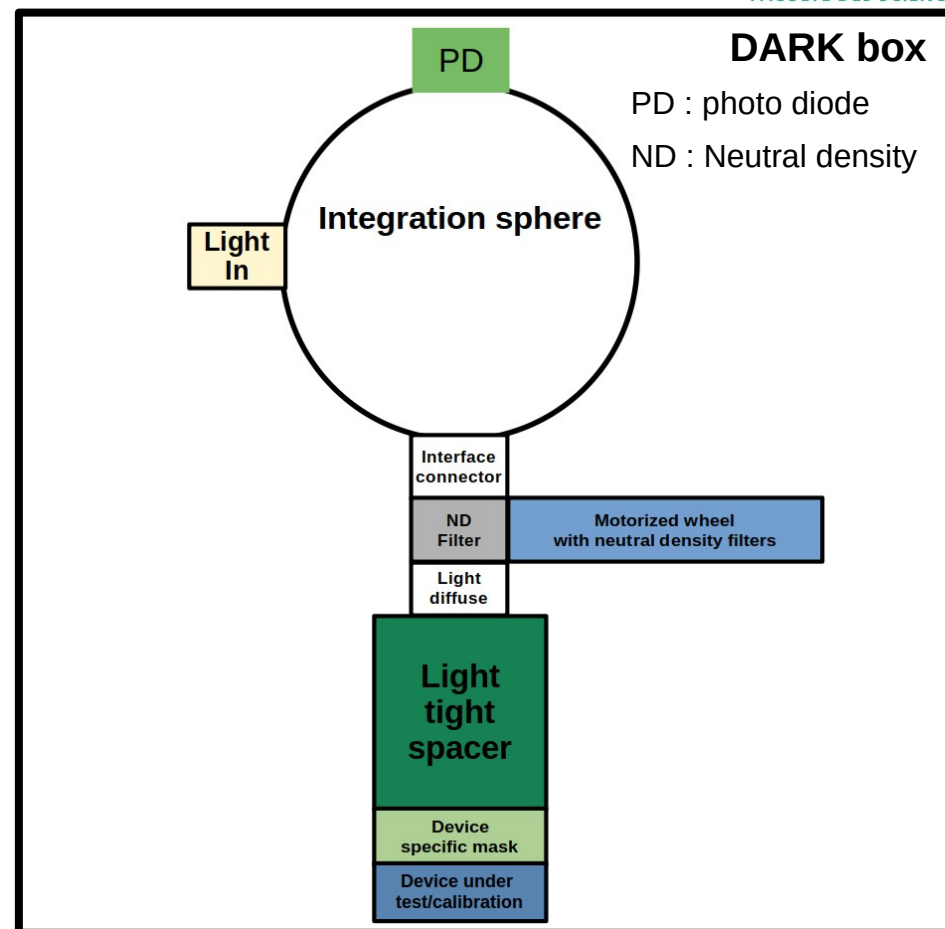
DAQ FPGA

Test bench at UNIGE



DARK box with interface patch panel

We are open for collaboration



DARK box

PD : photo diode
ND : Neutral density

Picoammeters for precise current measurements and SiPM bias.

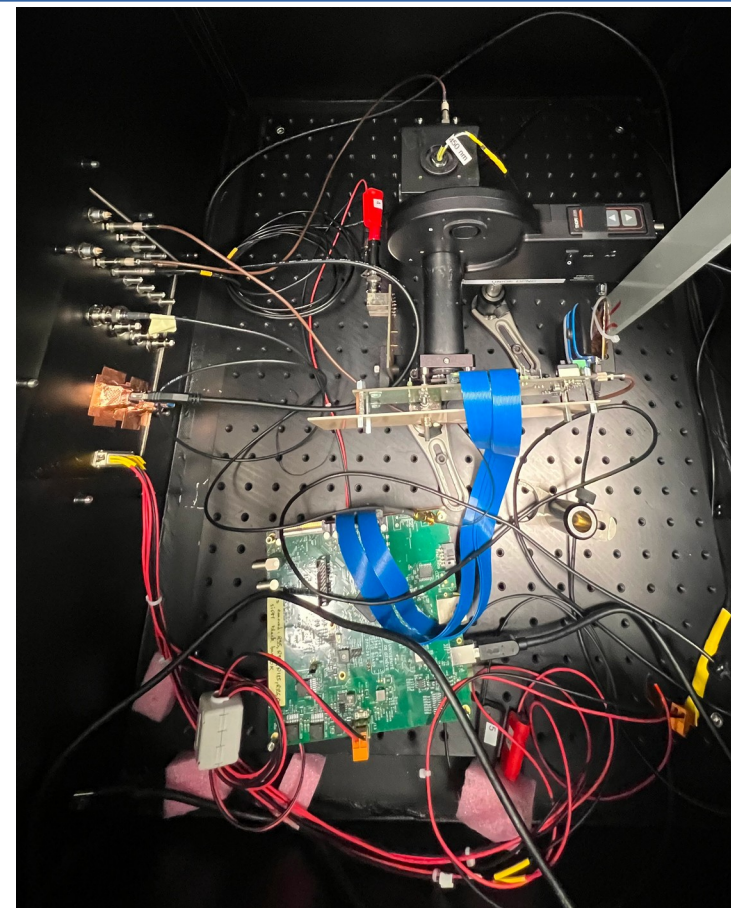
Pulsed and continues light sources
Motorized wheel with neutral density filters
Temperature and humidity sensors
Calibrated photodiodes
2 GHz readout oscilloscope

We plan to add 3D translational stage

Test bench at UNIGE

**DARK box with
interface patch panel**

We are open for collaboration



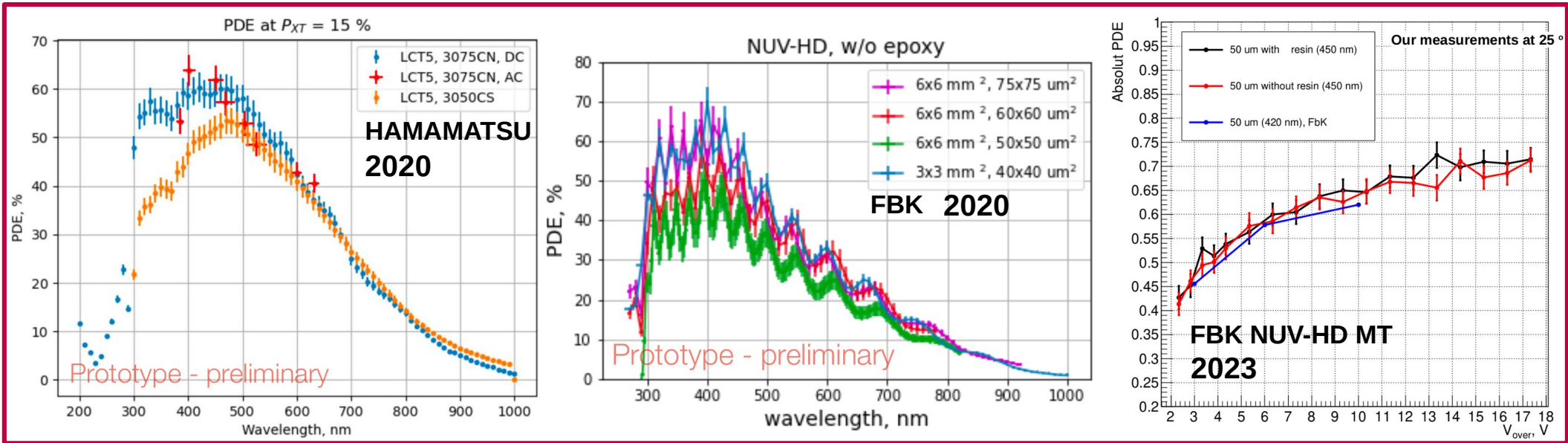
Picoammeters for precise current measurements and SiPM bias.

Pulsed and continues light sources
Motorized wheel with neutral density filters
Temperature and humidity sensors
Calibrated photodiodes
2 GHz readout oscilloscope

We plan to add 3D translational stage

The silicon photomultiplier (SiPM) light sensor.

- Collaboration between the University of Geneva and Hamamatsu for **IACT***.
- Comparison with FbK.
- All the measurements done by UNIGE team.



	HAMAMATSU LCT5	FBK NUV-HD	FBK NUV-HD MT**
PDE (photo det. Eff.), [%]	50 % at 300 nm 60 % at 400 nm	45 % at 300 nm 65 % at 400 nm	57 % at 450 nm
DCR[MHz/cm ²]	2.5 at 6V _{ov}	25 at 6V _{ov}	6 at 6V _{ov}
OCT (Opt. x-talk) [%]	12 % at 6V _{ov}	20 % at 6V _{ov}	4 % at 6V _{ov}
Pulse FWHM [ns]	3	8	~3 (with shaping ampl.)

*Imaging Atmospheric Cherenkov Telescope.

**Very promising device but the packaging remains the major issue.

FANATIC* – the preamplifier ASIC



- ➔ Fully developed by UNIGE, Swiss companies involved for chip packaging.
- ➔ The chips wire bonded at UNIGE.

FLARE project (20FL21-201539)

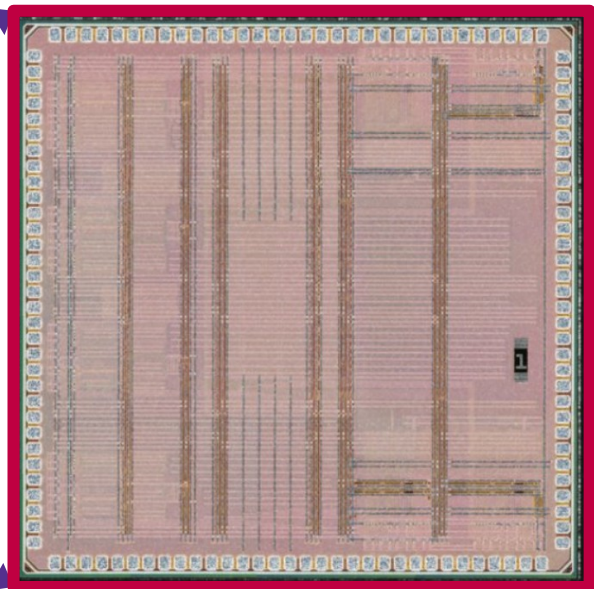
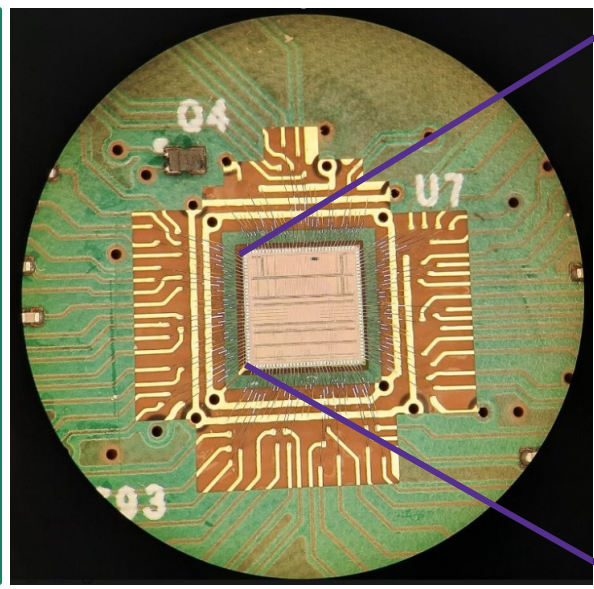
Main specification:

- Power consumption: 40 mW per pixel
- Dynamic range: 1-250 p.e (good linearity)
- Signal-to-noise ratio of 5
- Fast response: 3-5 ns FWHM

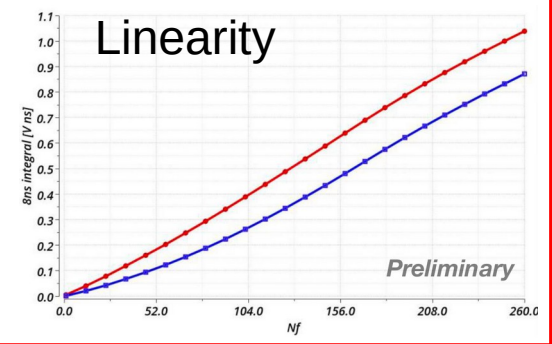
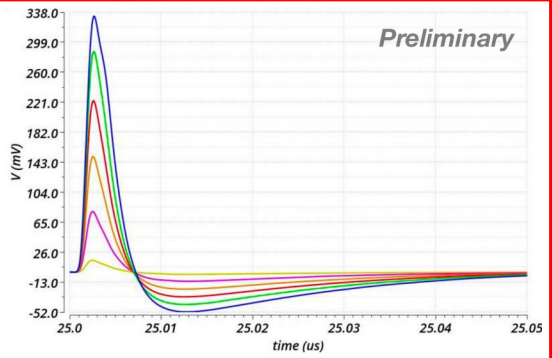
Second version of the ASIC designed in collaboration with Spain

Time line :

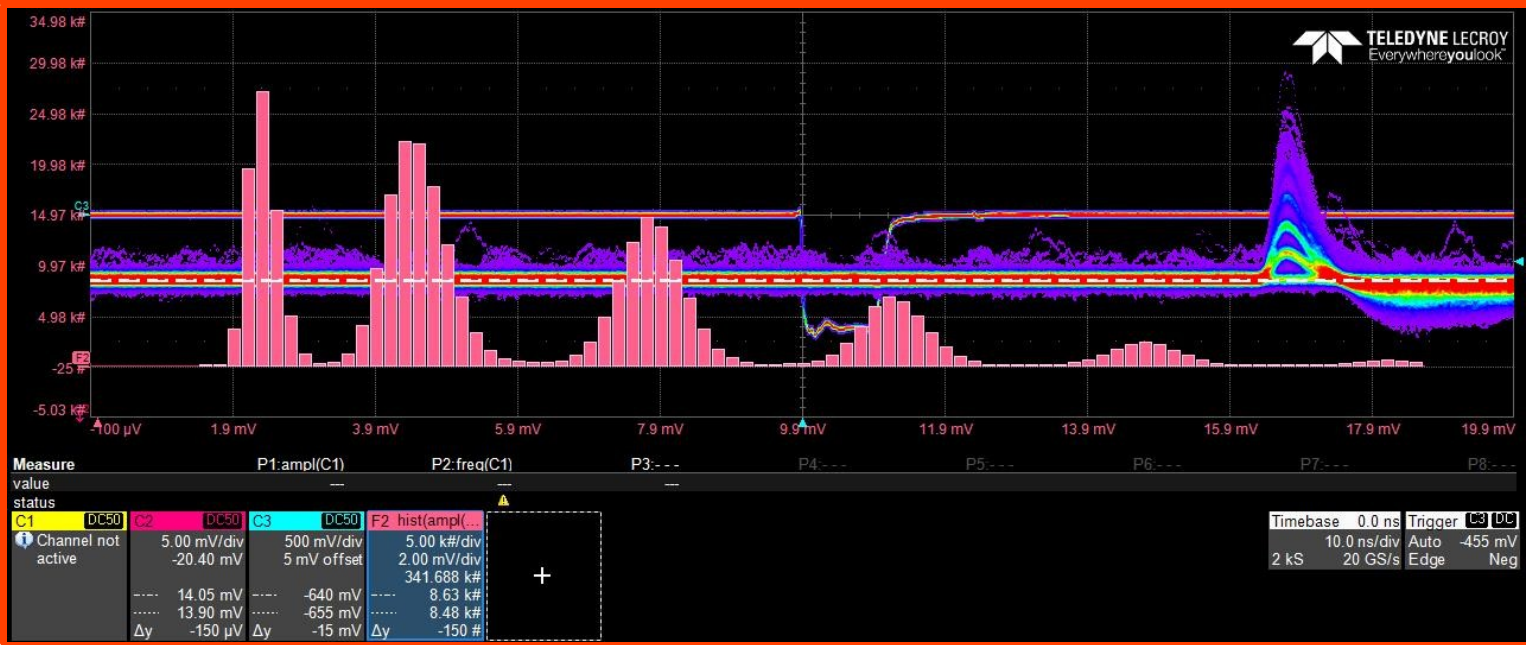
Design end of 2024
Production April 2025



Simulation



Measurements



* Fast **A**NAlog **T**ransimpedance amplifier **I**ntegrated **C**ircuit

L1 board and Telescope Central Trigger Processor (CTP) board

Main components are :

FADC (commercial or custom designed by EPFL)

FPGA: AMD / Xilinx Kintex UltraScale+

Functionalities:

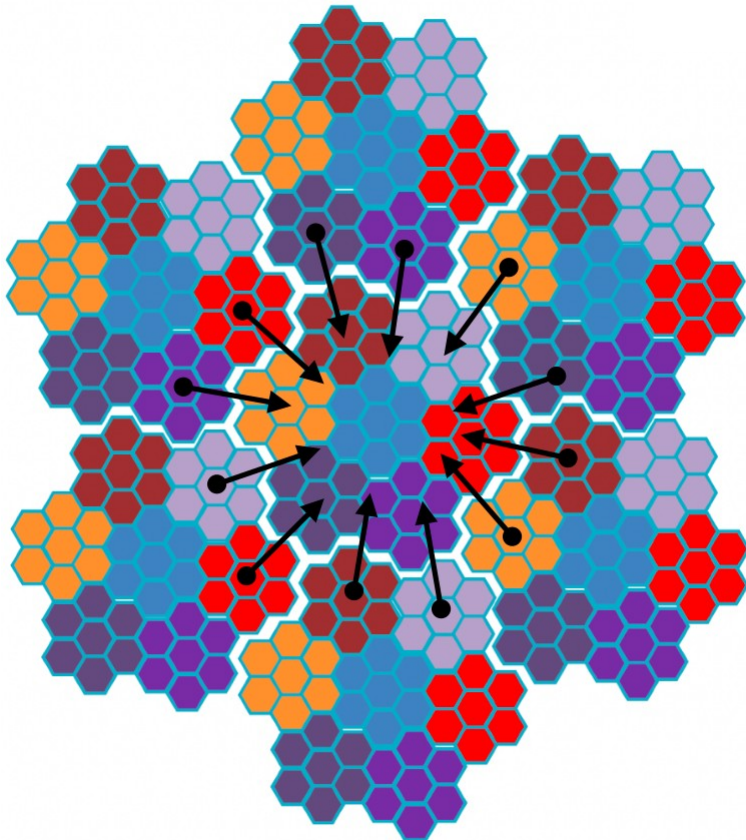
Capture and buffer FADC stream

Perform low level trigger (digital sum of super flower)

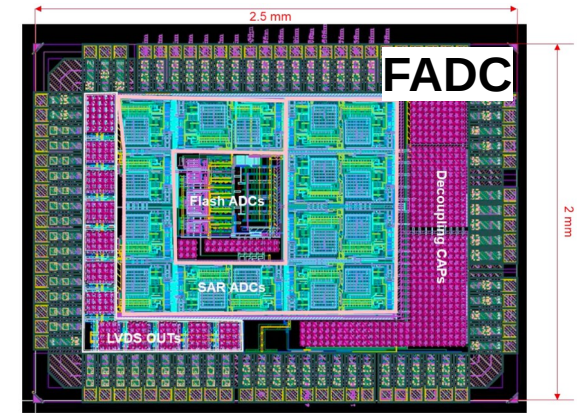
Send to Central Trigger Processor only “triggered events”

Reads 49 pixel (super flower or flower of flowers)

Each L1 board connected to neighbor with 1 or 2 10Gbps links.



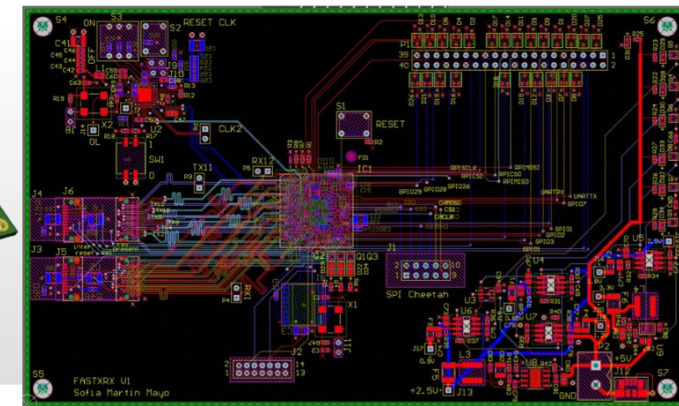
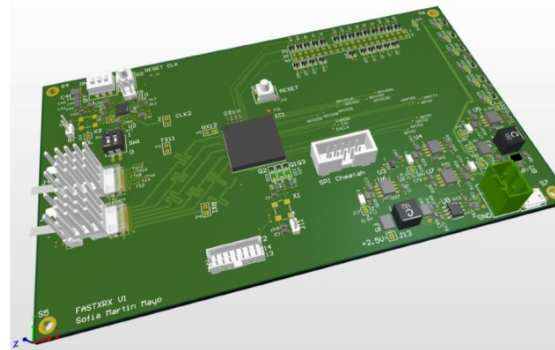
Front – end board



FLARE project (20FL21-201539)

CTP board

- PCB development:
 - Design finished and files sent to the manufacturing company.
 - Right now, they are inspecting the design.



- ➔ Collect data from events passing L1 trigger condition
- ➔ Perform partial event building
- ➔ Manage coincidence of hardware telescope triggers
- ➔ Level 2 trigger with DBSCAN based or/and CNN – based algorithms

L1 board and Telescope Central Trigger Processor (CTP) board

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Functionalities:

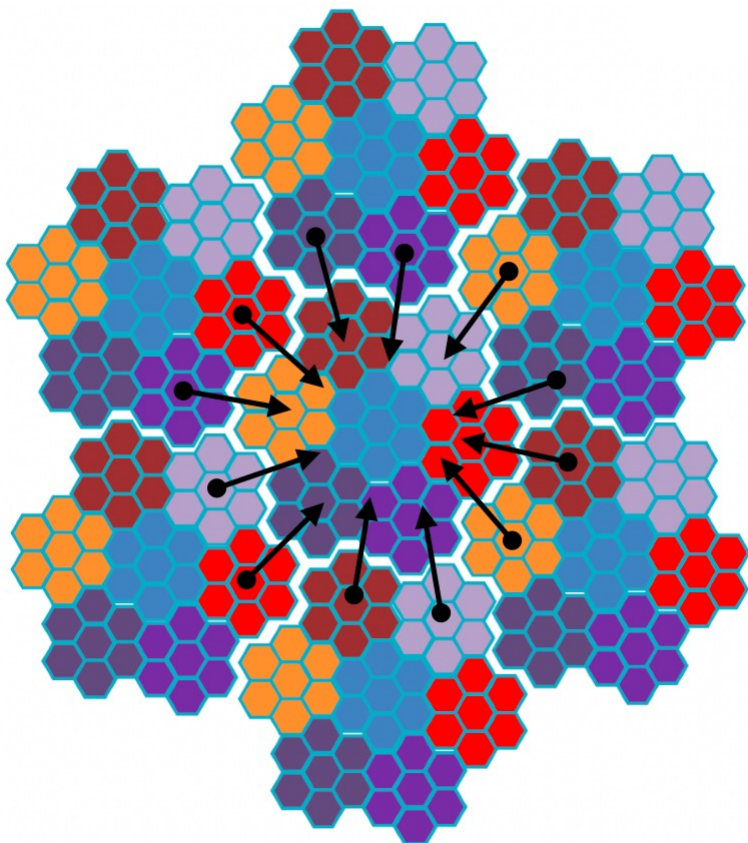
Capture and buffer FADC stream

Perform low level trigger (digital sum of super flower)

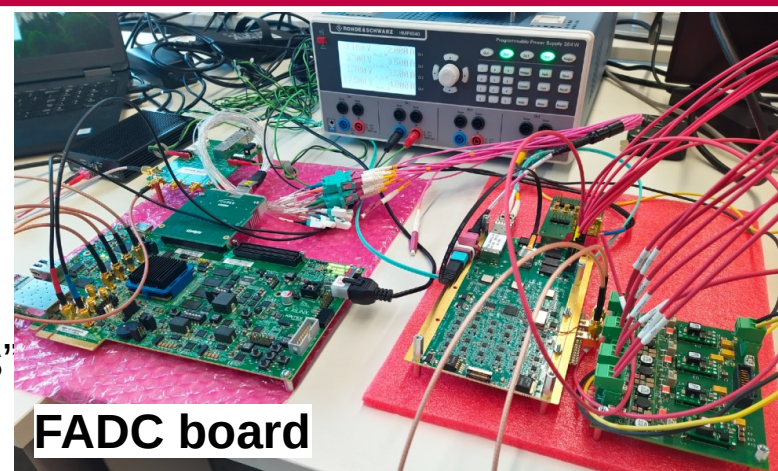
Send to Central Trigger Processor only “triggered events”

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Each L1 board connected to neighbor with 1 or 2 10Gbps links.



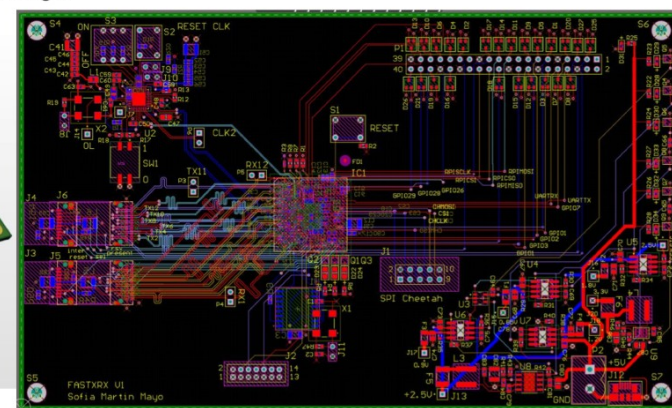
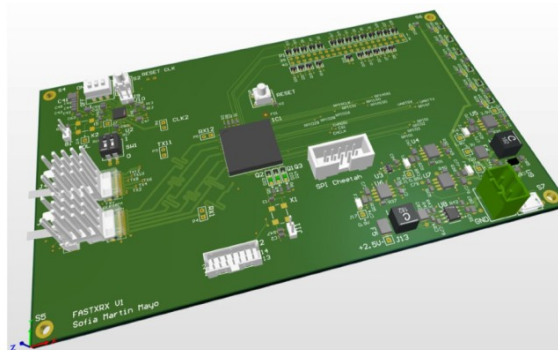
Front – end board



FADC board

CTP board

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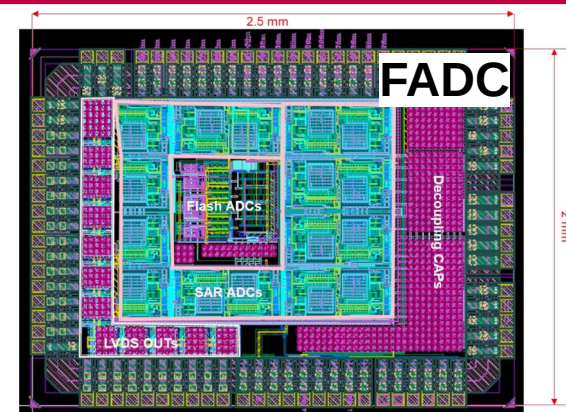
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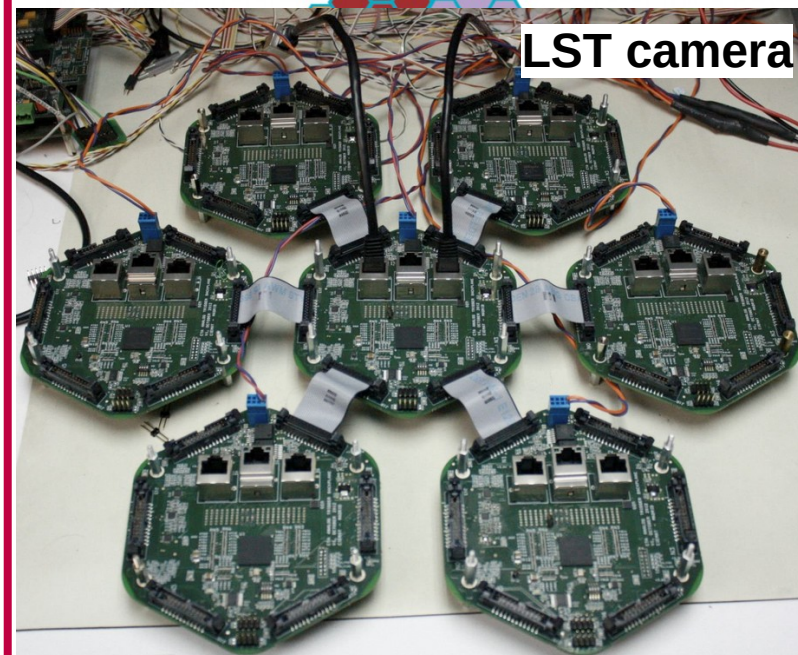
Front – end board



FLARE project (20FL21-201539)

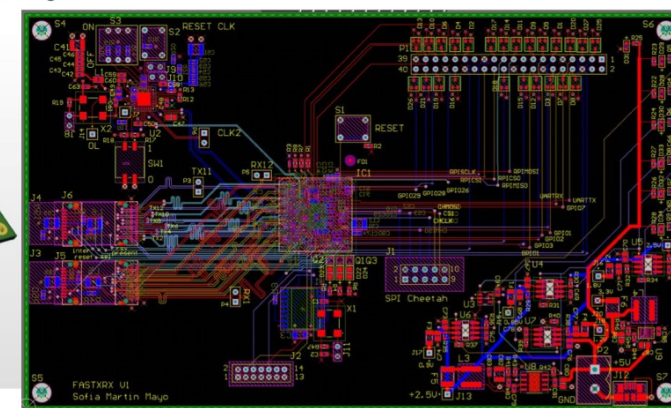
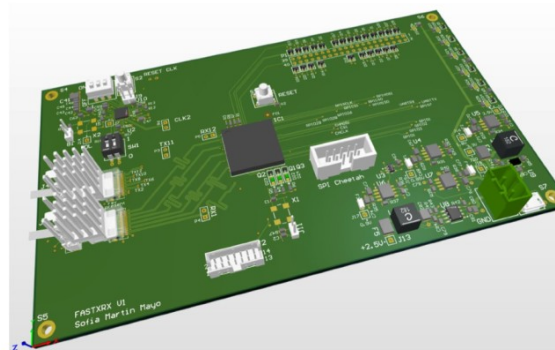


LST camera



CTP board

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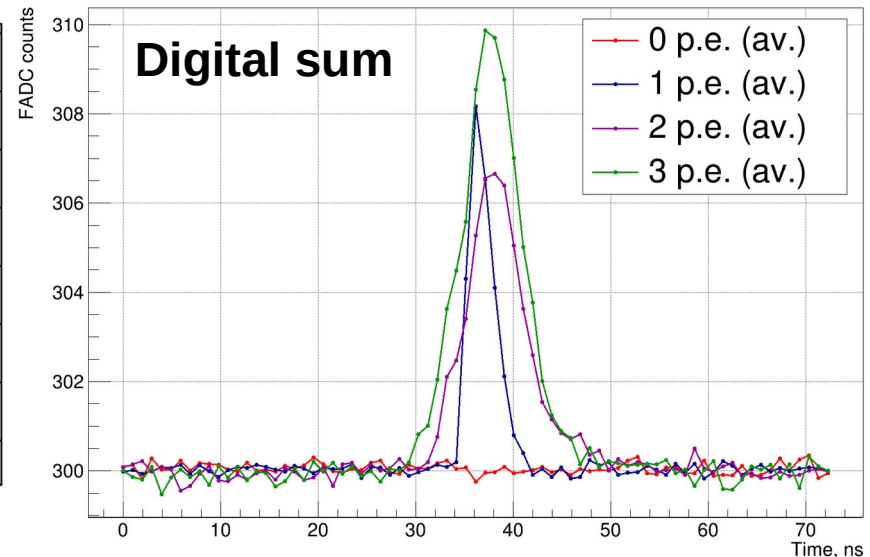
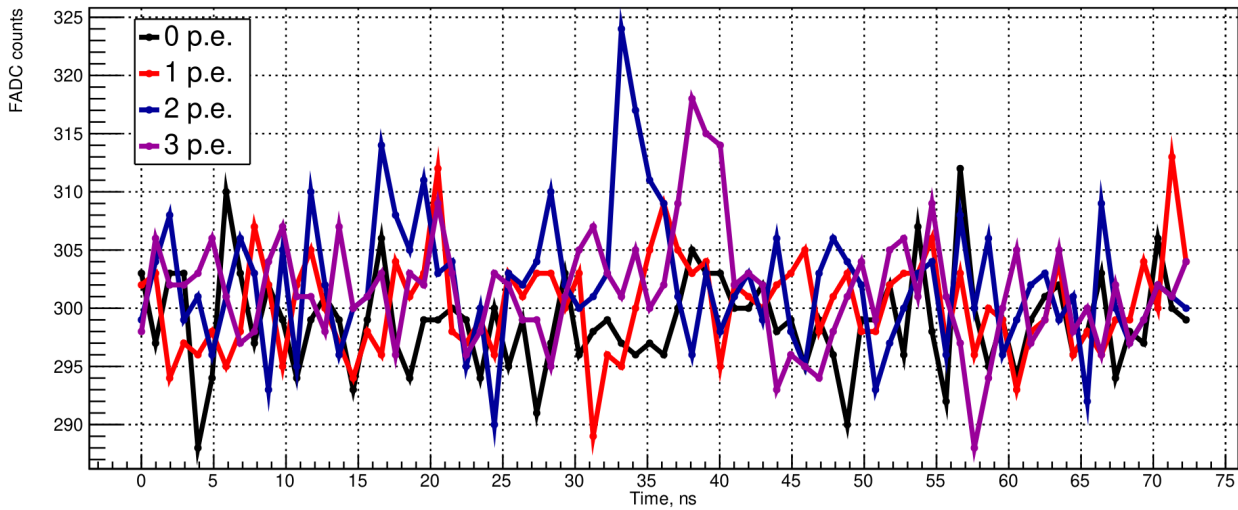
- ➔ Collect data from events passing L1 trigger condition
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- ➔ Manage coincidence of hardware telescope triggers
- ➔ Level 2 trigger with DBSCAN based or/and CNN – based algorithms

Level 1 trigger based on digital sum

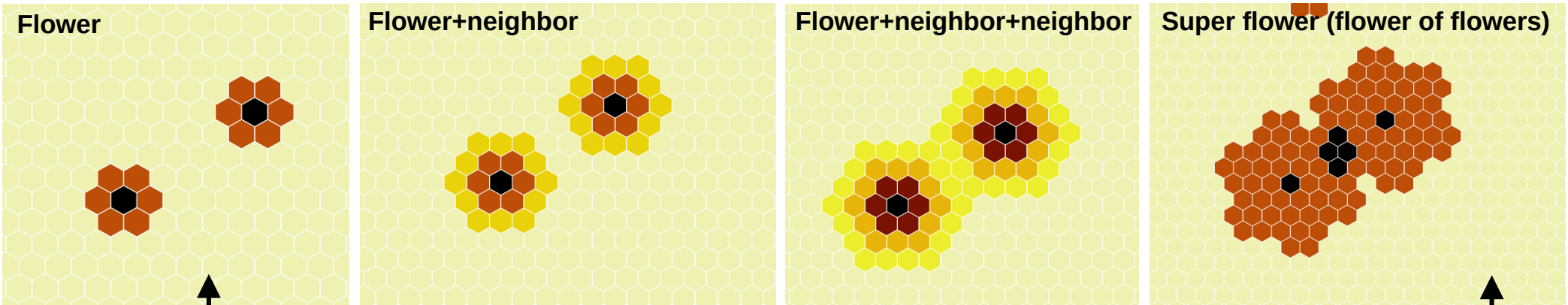
Digital sum definition : $\sum_{\text{time}} \sum_{\text{channels}} (A_{\text{channels}}^{\text{time}})$

It serves as an effective signal amplifier and noise cancellation.

Example of the waveform with 0, 1, 2, 3 photon



Different topologies

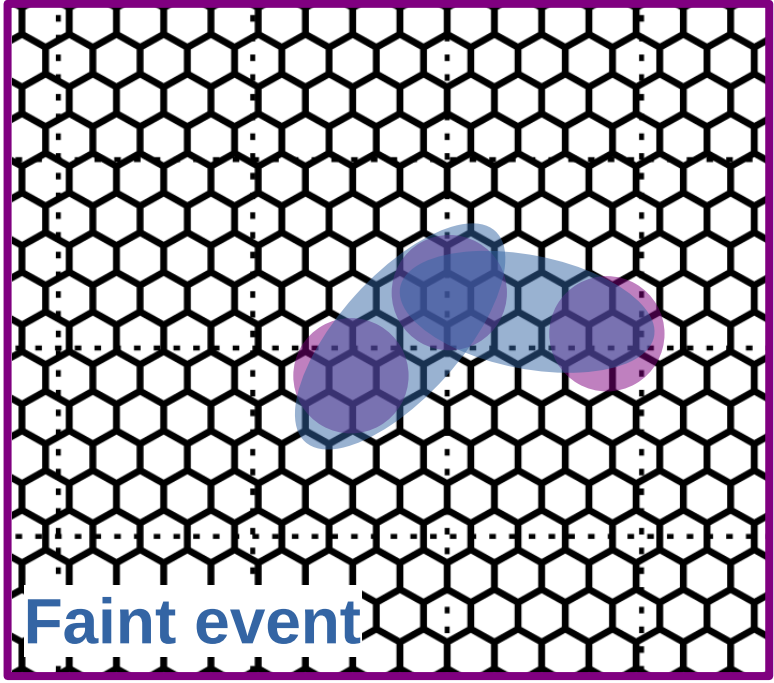


L. Burmistrov Selected input for the L2 trigger.

Selected input for the L1 trigger.

Level 2 trigger based on DBSCAN

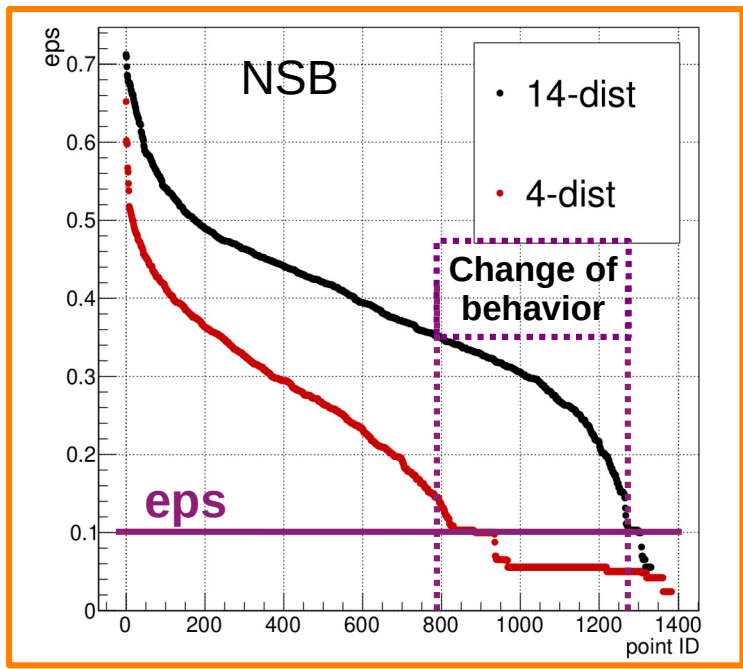
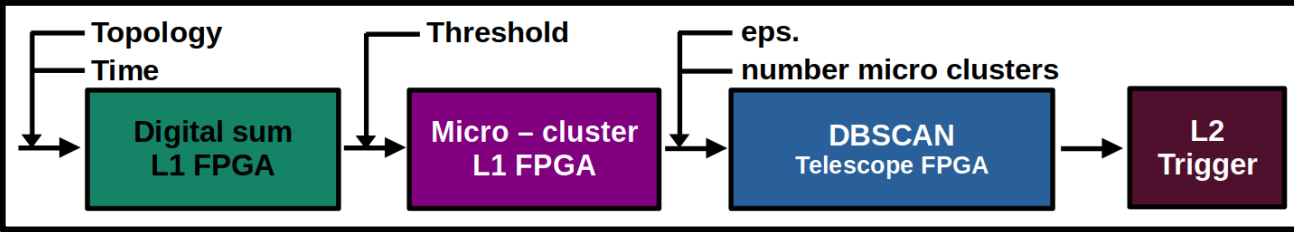
Density Based Spatial Clustering of Applications with Noise



From: KDD-96 Proceedings. Copyright © 1996, AAAI (www.aaai.org).
A Density-Based Algorithm for Discovering Clusters in Large Spatial Databases with Noise. Martin Ester, Hans-Peter Kriegel, Jiirg Sander, Xiaowei Xu

- Faint events have arbitrary shape
- Time introduced in the metric to account for shower development.
- **Spatial – time** clustering with **DBSCAN**
- **DBSCAN** can be used for waveform/image cleaning.

- Type of the digital sum to form a micro-cluster.
- Threshold on the digital sum to form micro-cluster (point for DBSCAN).
- Timing component introduced into the metric
- The maximum distance between two micro-clusters (eps.).
- The minimum number of micro-clusters build the cluster.



Digital sum only

DBSCAN without time information

Spacial clustering only

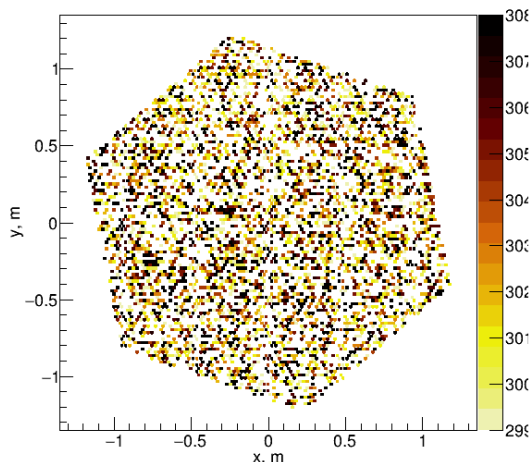
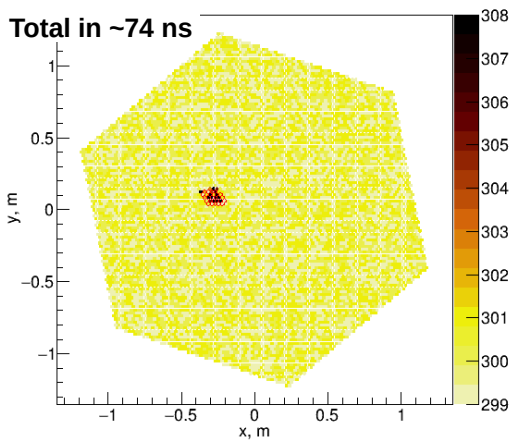
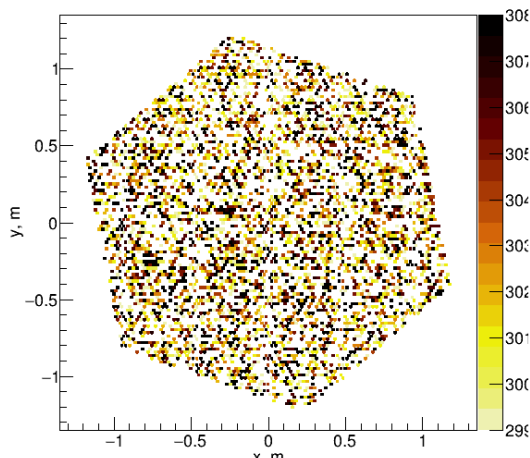
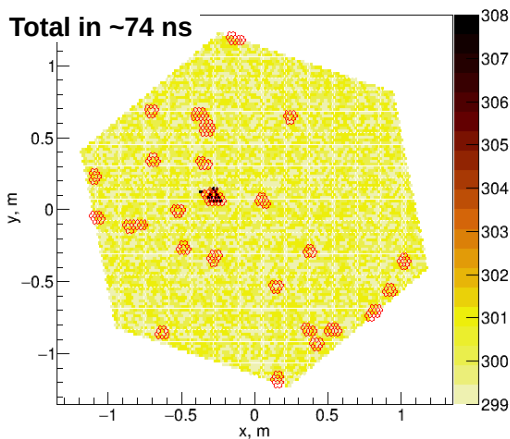
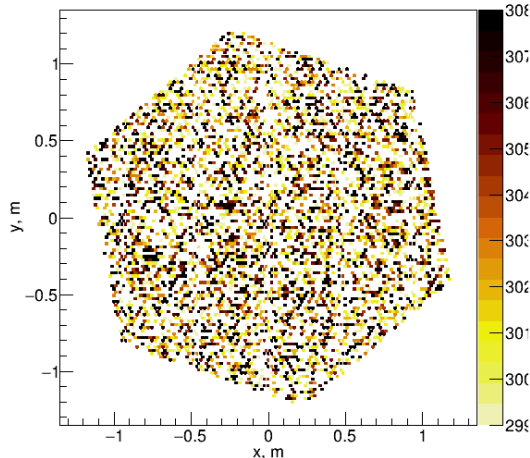
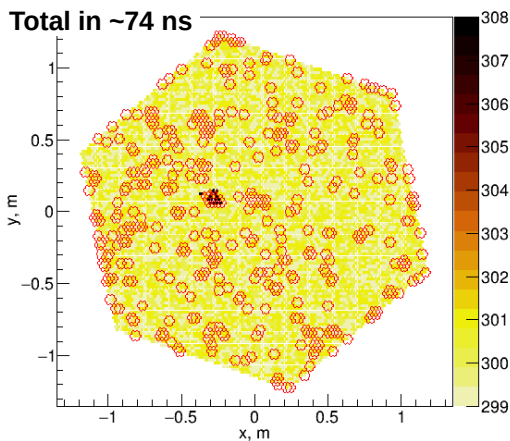
DBSCAN with time information

Time - Spacial clustering

```
wf_time : 37 ns
_gamma
event_id : 29209
energy : 12 GeV
xcore : -145 m
ycore : -221 m
ev_time : 35 ns
nphotons : 123
n_pe : 45
n_pixels : 21
azimuth : 1800/10 deg
altitude : 699/10 deg
h_first_int : 21481 km
hmax : 13667 km
```

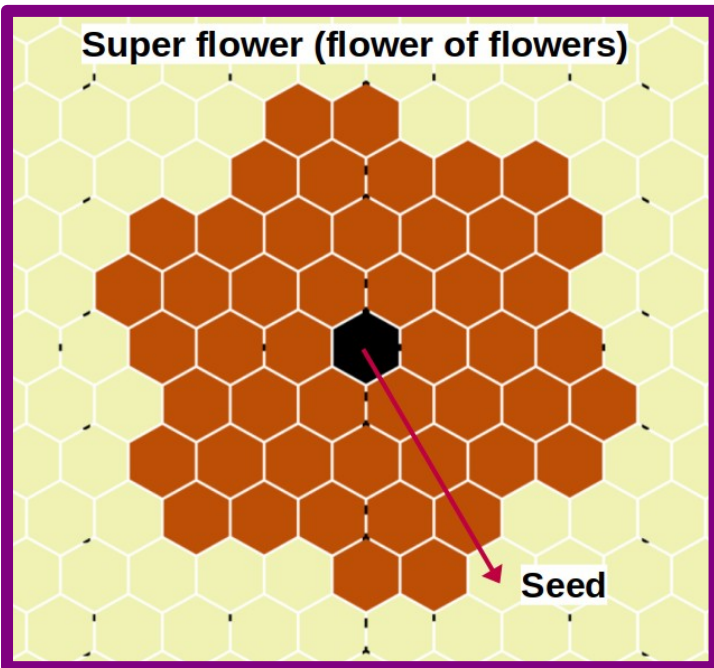
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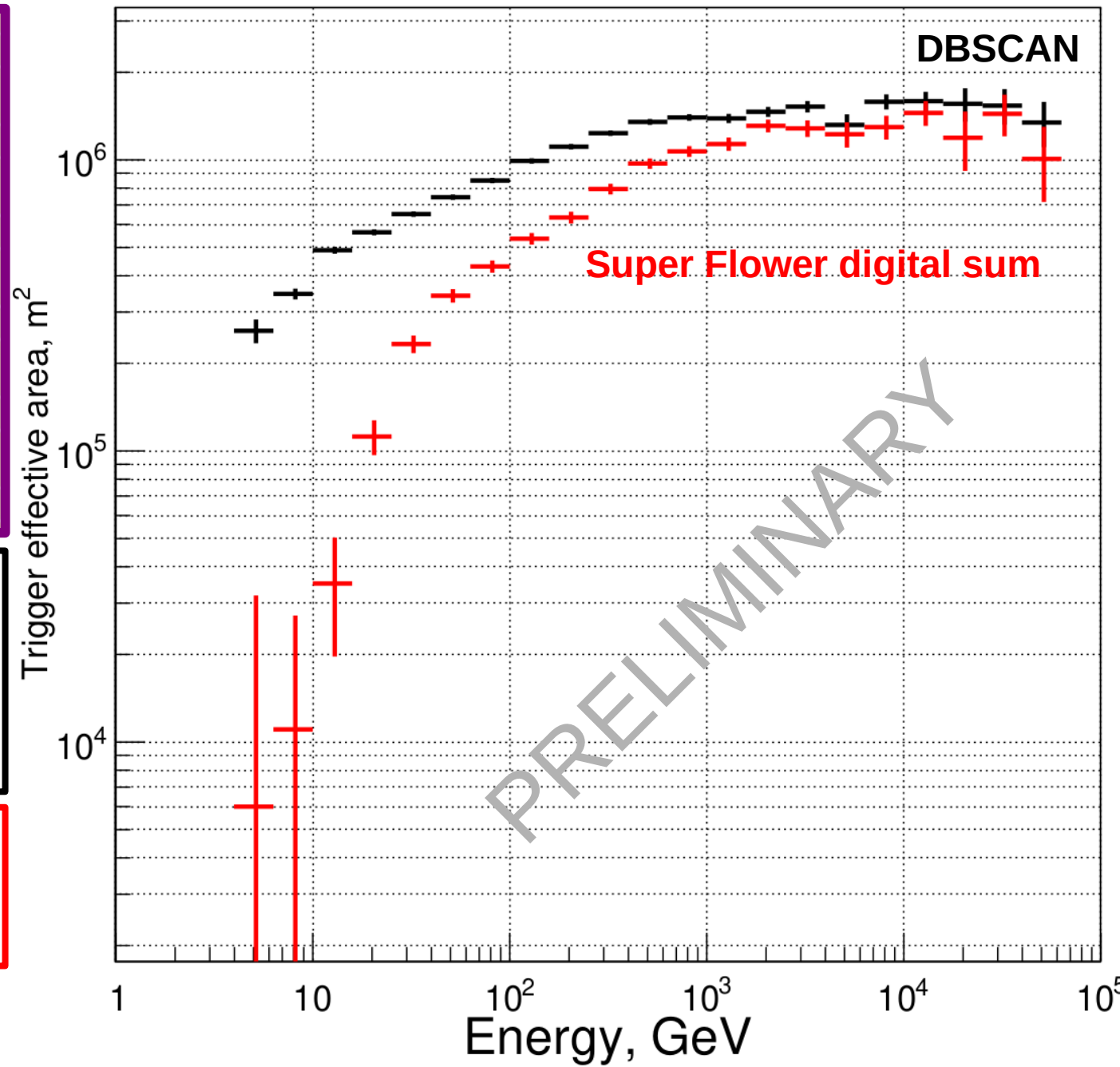
DBSCAN vs. super flower digital sum

Trigger effective area (on axis gammas)



We choose the super flower as a cluster more or less equivalent to "LST trigger".

DBSCAN is a highly promising algorithm.



Hardware implementation (preliminary feasibility study for FPGA)

Off line operation (Level 2 trigger)

DBSCAN would run on stereo triggered events, with latency of about **$\sim 3 \mu\text{s}$** .

Accelerating the DBSCAN clustering algorithm for low-latency primary vertex reconstruction

<https://indico.cern.ch/event/1106990/contributions/4998133/>

With 230 tracks (points) they got **$0.726 \mu\text{s}$** latency.
VU9P FPGA

Latency
FPGA = $0.726 \mu\text{s}$
CPU = $92.7 \mu\text{s}$
 $127\times$
Speedup!

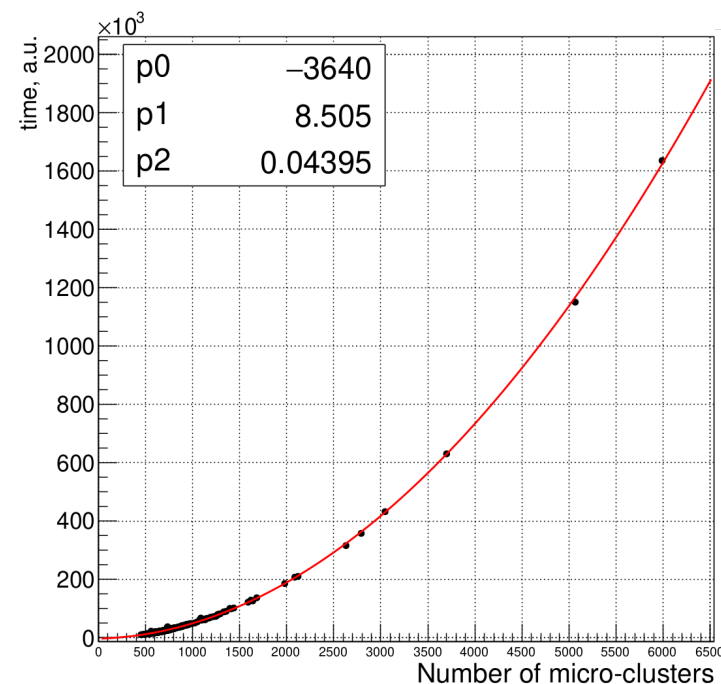
- Alex Tapper (Imperial College London)
- Andrew Rose
- Lucas Santiago Borgna (Imperial College (GB))
- Marco Barbone
- Robert John Bainbridge (Imperial College (GB))
- Wayne Luk

Real time (Level 1 trigger) ?

DBSCAN would run in real time at ~ 10 MHz,
latency of $0.01 \mu\text{s}$ is required in this case.

We have ~ 3 times less points (micro clusters), corresponds to $0.07 \mu\text{s}$ latency.

Possible algorithm optimization
- time axis is fully ordered.



Conclusion :-)



credit: CTA Consortium, Akihiro Ikeshita, Mero-TSK, International



Thank you very much for your attention