

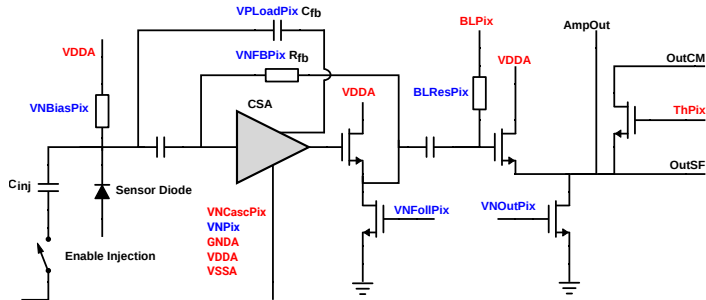
# DAC Optimisation

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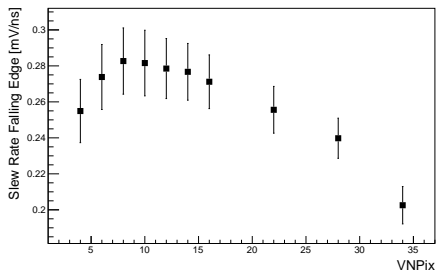
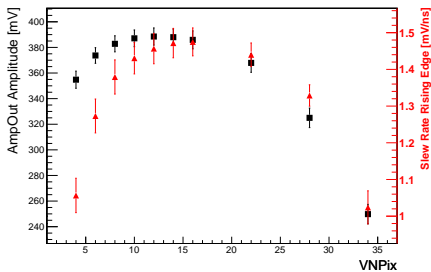
RD50 HV-CMOS 15/02/24

- MPW4 has 7 DACS controlling the analogue performance (excluding VPTRIM) with 6bit/64 possible values
- To optimise the settings we don't want to try out all  $4.4 \times 10^{12}$  combinations especially if the analogue FE doesn't work properly for most of them
- What to do?



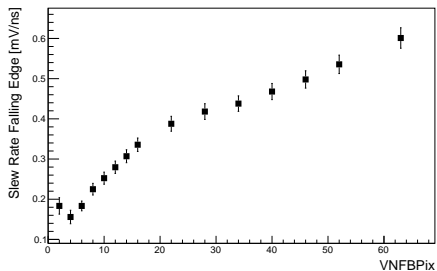
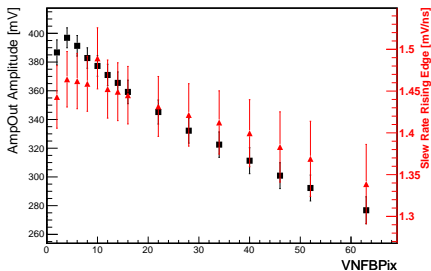
- Did a similar study for my Masters with MuPix8
- Very similar analogue FE
- Studied analogue output with a scope
- Measured amplitude and the slew rates for both flanks
- Measured every DAC w.r.t the default to get an idea of the impact

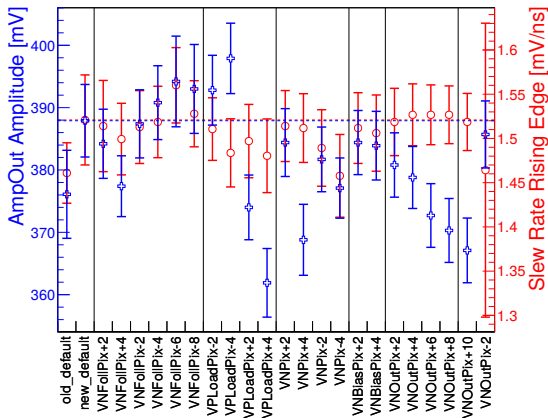
# Example VNPix



- Clear impact of DAC setting
- Only limited working range

# Example VNFBPix





- Take the "optimal" value from each DAC and start again from there
- Investigate in a reasonable step size around the new settings
- repeat until you are happy

- Not everything is accessible via the SFOUTBUFF as high pass and comparator can only be seen on the COMPOUTBUFF
- SFOUTBUFF is rather slow and will mask subtle changes
- What do we want to optimise for?
- Suggestion: signal ( $\mu$ ) and noise ( $\sigma$ ) from s-curve measurement + power consumption
- Dispersion of both and ToT might also be interesting
- Should also look at the chip-to-chip dispersion
- In principle one would also like to optimise the timing performance
- In practice a bit more difficult as a precise reference is needed and the 25 ns binning might be too coarse to resolve changes
- Suggest this is something to study at the testbeam and develop the lab setup later