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The testing and validation procedure of the PCBs of ME0 GEM detector for the phase 2 upgrade of the CMS detector

The CMS experiment at CERN is foreseen to receive a substantial upgrade of its outer-tracker detector and its front-end readout electronics, requiring higher granularity and readout bandwidth to handle the large number of pileup events in the High-Luminosity LHC during Long Shutdown-3.(LS3) The objective is to increase the integrated luminosity by a factor of 10 beyond the LHC's design value. The CMS just commissioned the Gaseous Electron Multiplier (GEM) detector, namely GE1/1, at the endcap during LS2. GE1/1 has already contributed to data collection during Run-3. Looking forward, CMS has outlined plans for further endcap upgrades, such as GE2/1 and ME0, as part of the LS3 upgrade for phase-2 of the LHC.

The ME0, a gas electron multiplier detector, consists of GEM detector assemblies located in the very forward region between the first endcap and endcap calorimeters. The ME0 detectors are expected to cover the pseudorapidity region between 2.0 and 3.0 and is proposed for the Phase-2 Muon System Upgrade for the CMS experiment to help increase the muon acceptance and to control the Level 1 muon trigger rate. A recent design iteration of this detector features GEM foils that are segmented on both sides, which helps to lower the probability of high voltage discharges. For this, it requires advanced two-layer print circuit boards (PCBs) for efficient signal readout and processing. Each ME0 detector is read-out by 24 VFAT3 chips, binary chips endowed with 128 channels, delivering essential trigger and tracking data. This data is subsequently relayed via a large PCB, known as the GEM Electronics Board (GEB) or Readout Board(ROB).The ROB is a two sided PCB that serves both as anode of the GEM chamber and the first stage of the signal readout chain. Copper strips facing the GEM chamber behave like electrodes on which charge is induced due to the electrons produced which are transmitted to the other side of the board through vias. Copper traces are present on this side, which route the signals produced, to the VFAT3 front-end ASIC through a HRS connector present on the ROB. This contribution will describe the design, mechanical properties and quality assurance testing of PCB-based readout systems to be used for ME0 detectors and verifies its suitability for HL-LHC.

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