# Electronic readout 1

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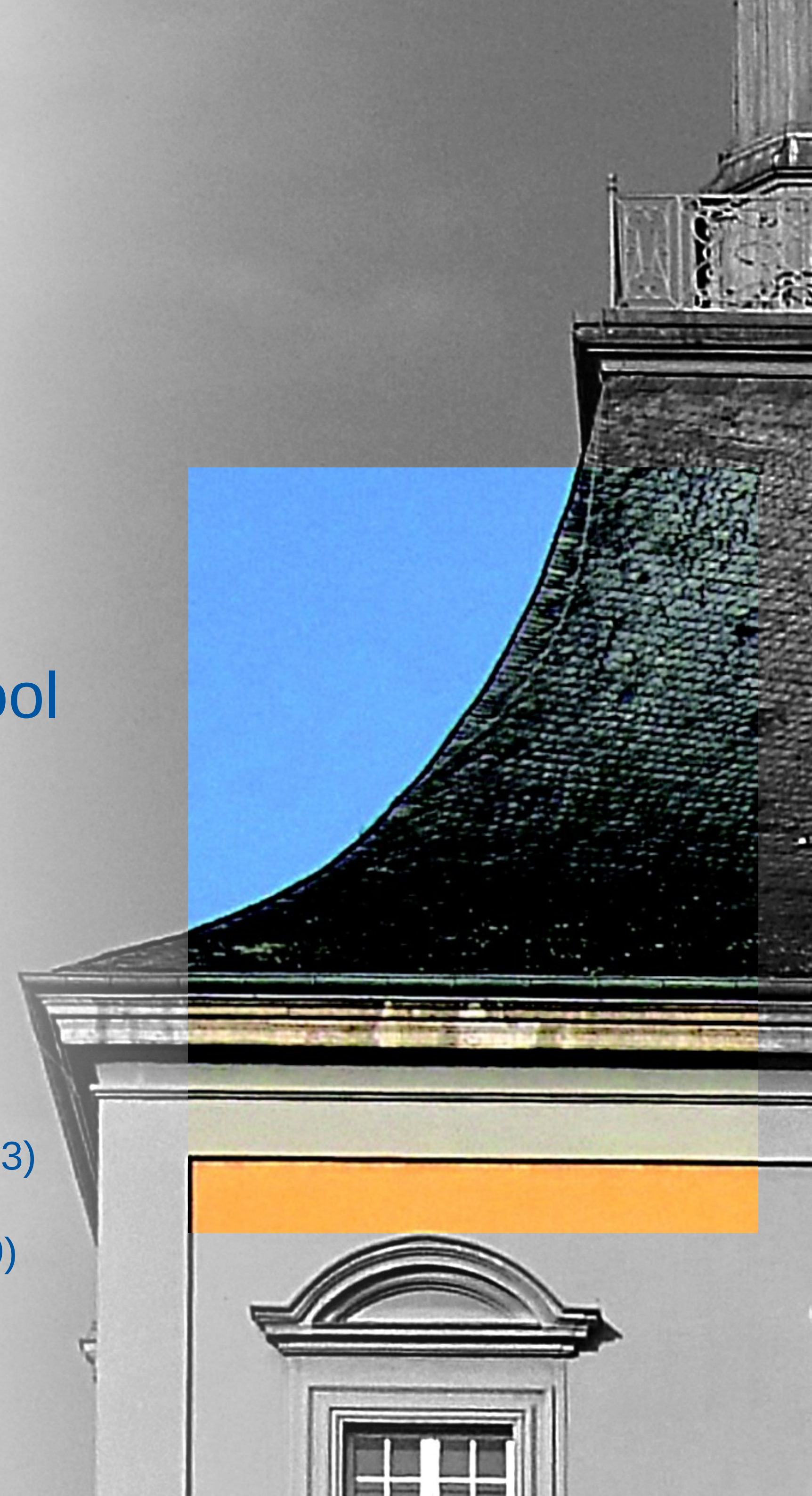
(University of Bonn)

DRD1 Gaseous Detector School

CERN 04.12.2024

With material from:
B. Ketzer & M. Lupberger
Lecture on *Physics of Particle Detectors* (2022/23)
and B. Ketzer
Lecture on Advanced Gaseous Detectors (2019)



# OUTLINE

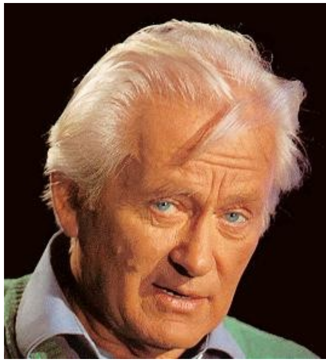
- Recap: Signal formation and Shockley-Ramo Theorem
- Segmented electrodes, readout structures
- Discrete electronic components
- Multi-channel readout, ASICs
- The readout chain, FPGA
- DRD1 common readout: SRS

# MOTIVATION/RECAP

Gaseous detector: Ionisation/excitation of gas atoms

- Ionisation separates $e^-$ from $A^+$
- Electric field ⇒ further separation, drift, (amplification)
- Moving charges induce signals on field electrodes
- Possibility to use theses signals to infer
  - Where
  - When
  - How strong

  the interaction with the detector medium was

**Nobel Prize 1992**
**to Georges Charpak**
*for his invention and development of particle detectors, in particular the multiwire proportional chamber*

NUCLEAR INSTRUMENTS AND METHODS 62 (1968) 262–268; © NORTH-HOLLAND PUBLISHING CO.

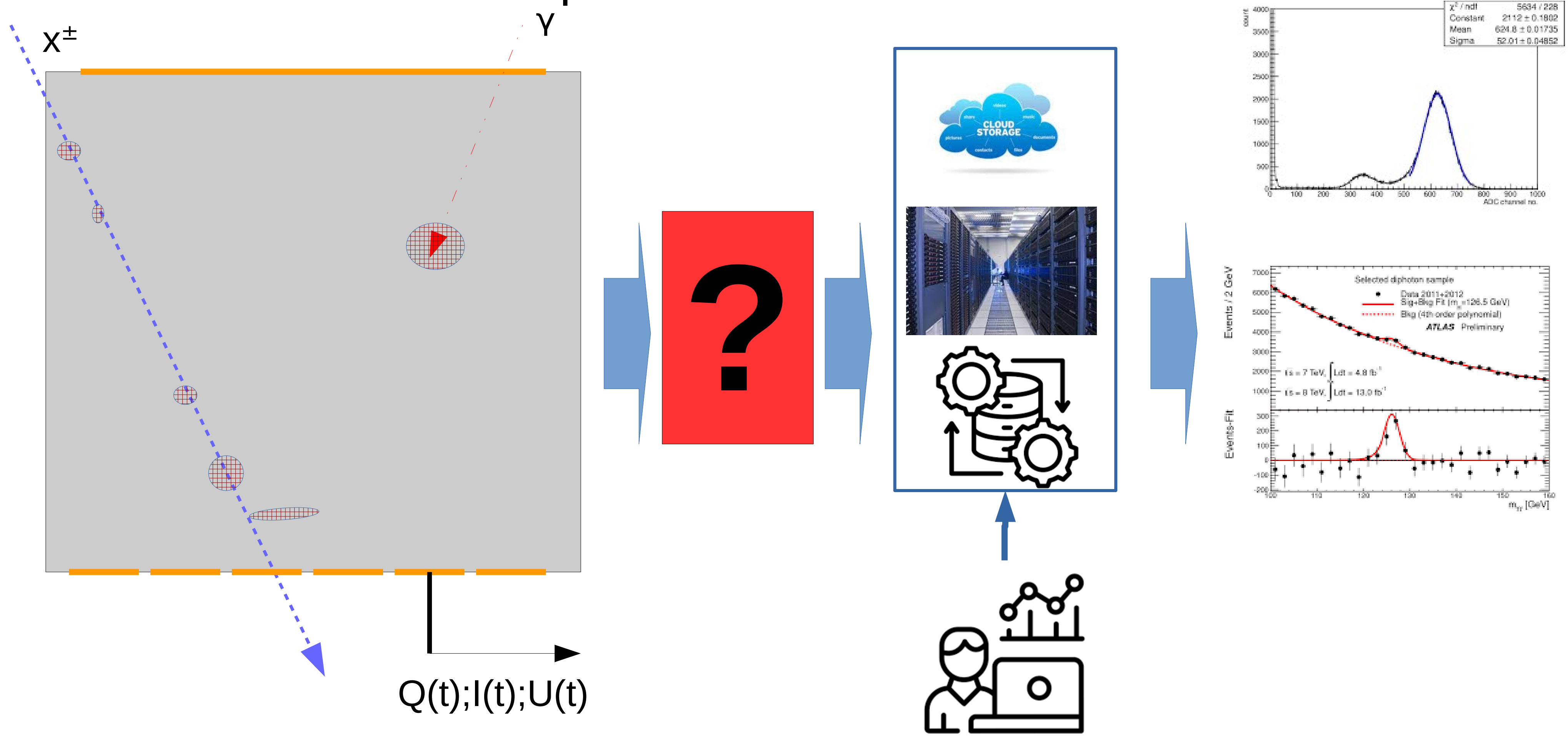
THE USE OF MULTIWIRE PROPORTIONAL COUNTERS
TO SELECT AND LOCALIZE CHARGED PARTICLES

G. CHARPAK, R. BOUCLIER, T. BRESSANI, J. FAVIER and Č. ZUPANČIČ
*CERN, Geneva, Switzerland*

Received 27 February 1968

# RECAP: SIGNAL FORMATION

## Electronic readout techniques




Data analyst

# RECAP: SHOCKLEY–RAMO THEOREM

Current I on given electrode i induced by moving charge

$$I_i(t) = \frac{q}{U_i}\boldsymbol{\nabla}\phi_i\left[\boldsymbol{x}_0(t)\right]\cdot\frac{\mathrm{d}\boldsymbol{x}_0(t)}{\mathrm{d}t} = -\frac{q}{U_i}\boldsymbol{E}_i\left[\boldsymbol{x}_0(t)\right]\cdot\boldsymbol{v}(t)$$

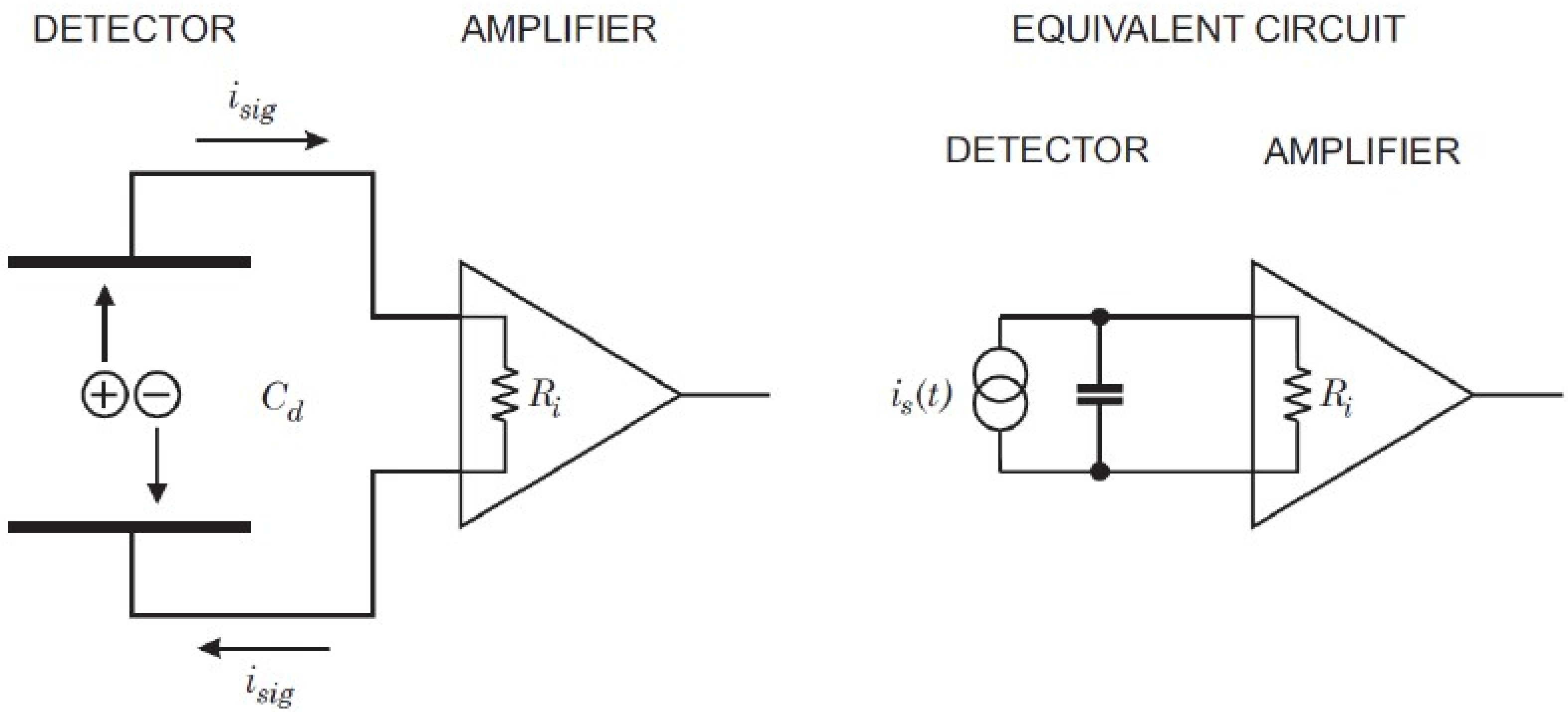
The current induced on a grounded electrode by a point charge $q$ moving along a trajectory $\boldsymbol{x}_0(t)$ is $I_i(t)$, where $\boldsymbol{E}_i(\boldsymbol{x}_0)$ is the electric field in the case where the charge $q$ is removed, electrode $i$ is set to voltage $U_i$, and all other electrodes are grounded.

- Convention: $U_i = 1$
- $\mathbf{E}_i(\mathbf{x}_0)$: Weighting field of electrode i at position $\mathbf{x}_0$
- $\mathbf{E}_i \neq \mathbf{E}_{det,el}$: Weighting field in general different to detector electric field
- $\hat{\mathbf{e}}_{\mathbf{Ei}} \neq \hat{\mathbf{e}}_{\mathbf{v}}$: Direction of weighting field different to charge trajectory

# ELECTRIC SIGNAL

A detector is a current source

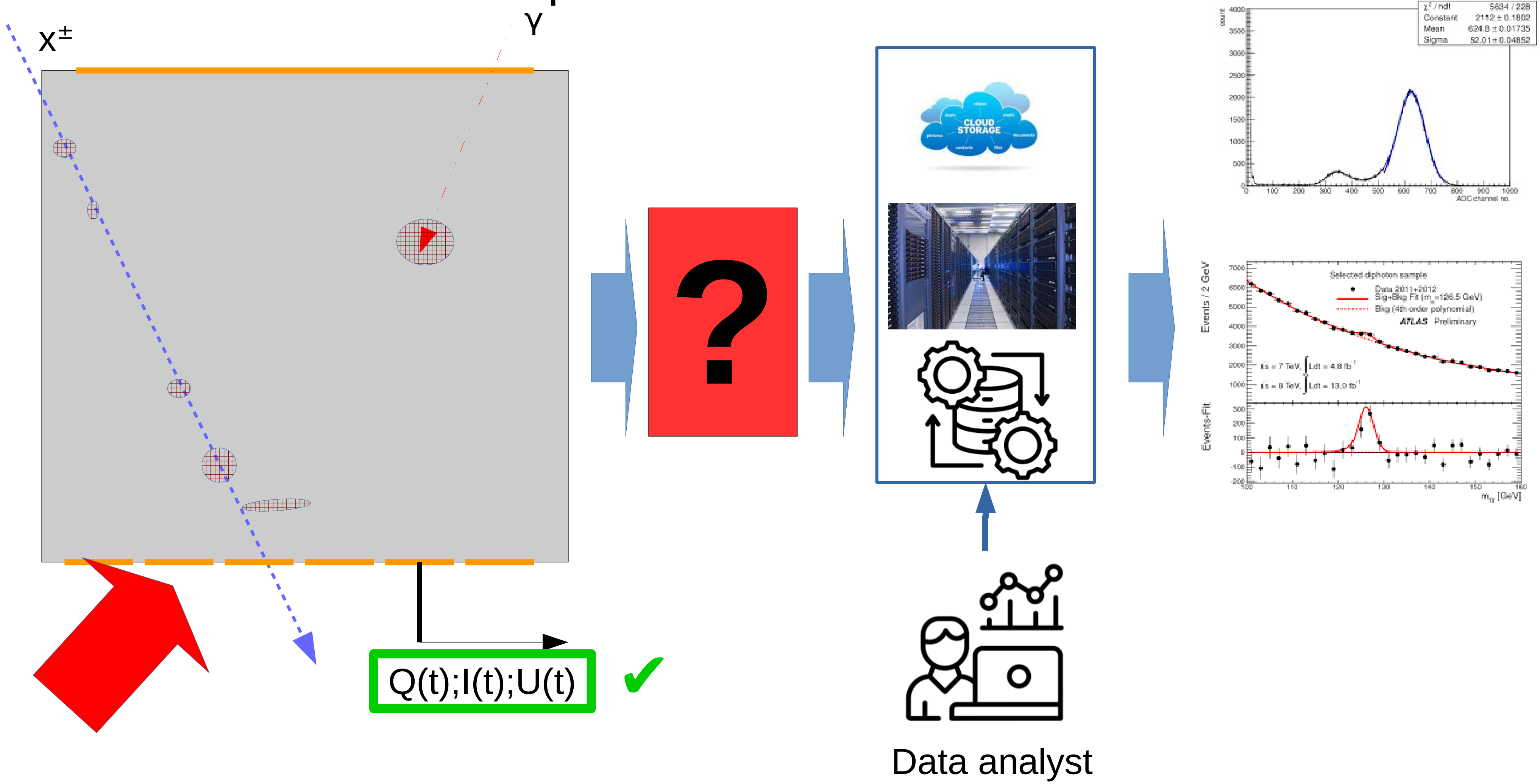
- delivers a current pulse independent of the load
- one can convert current into charge (integral) or voltage (via R or C)



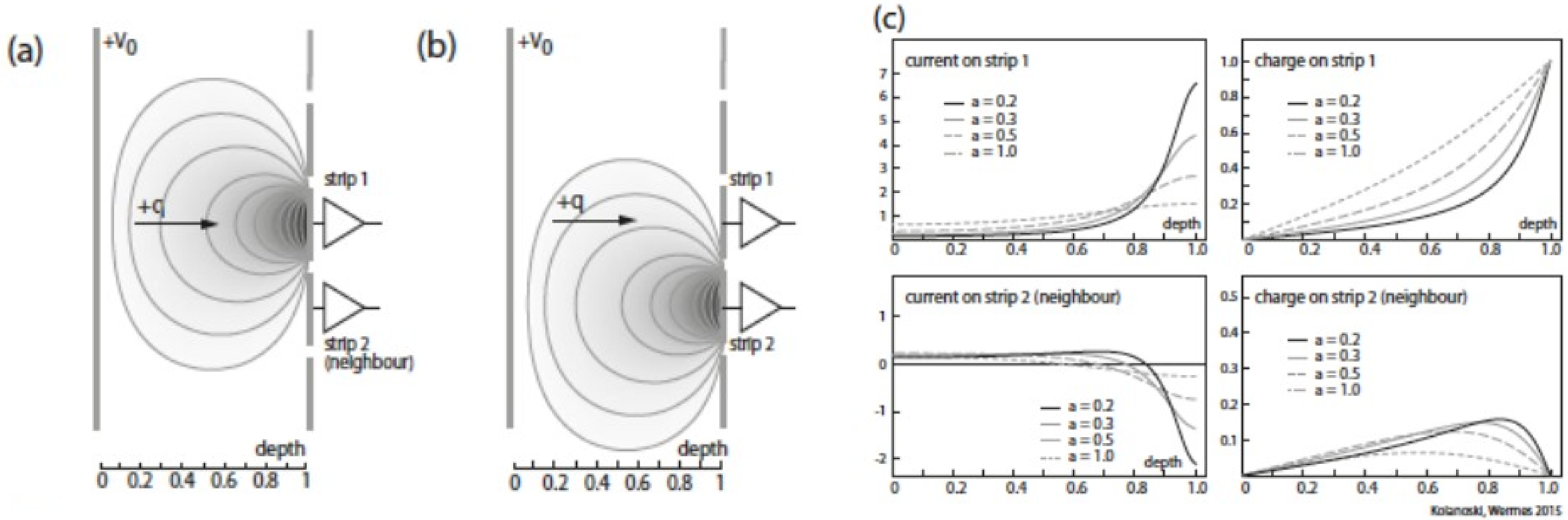

[H. Spieler, Semiconductor detector systems, Oxford, 2005]

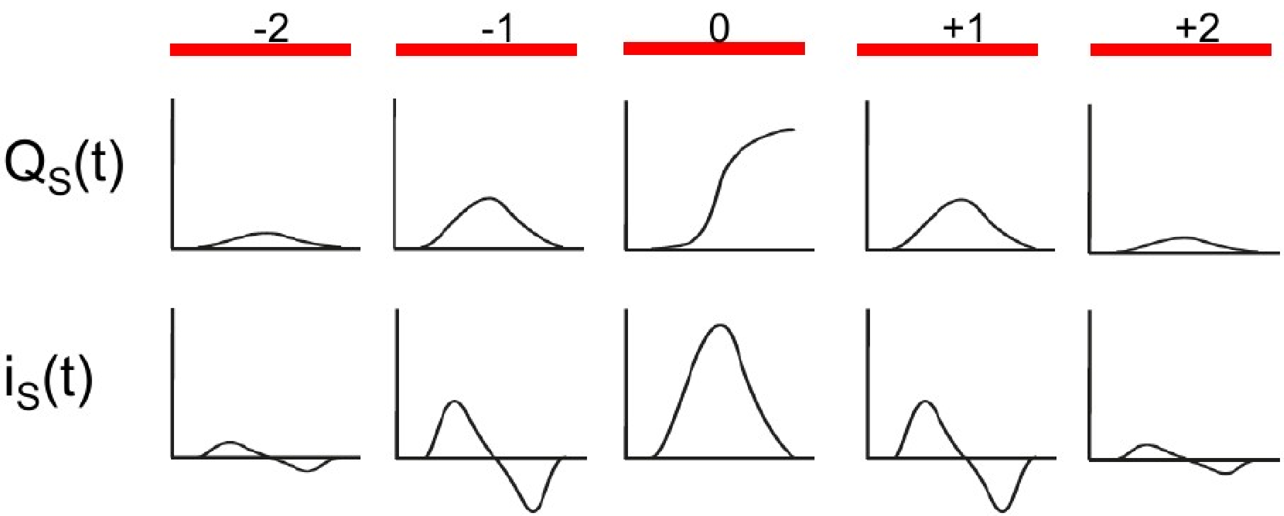
# ELECTRONIC READOUT OVERVIEW

Electronic readout techniques



# SEGMENTED ELECTRODS



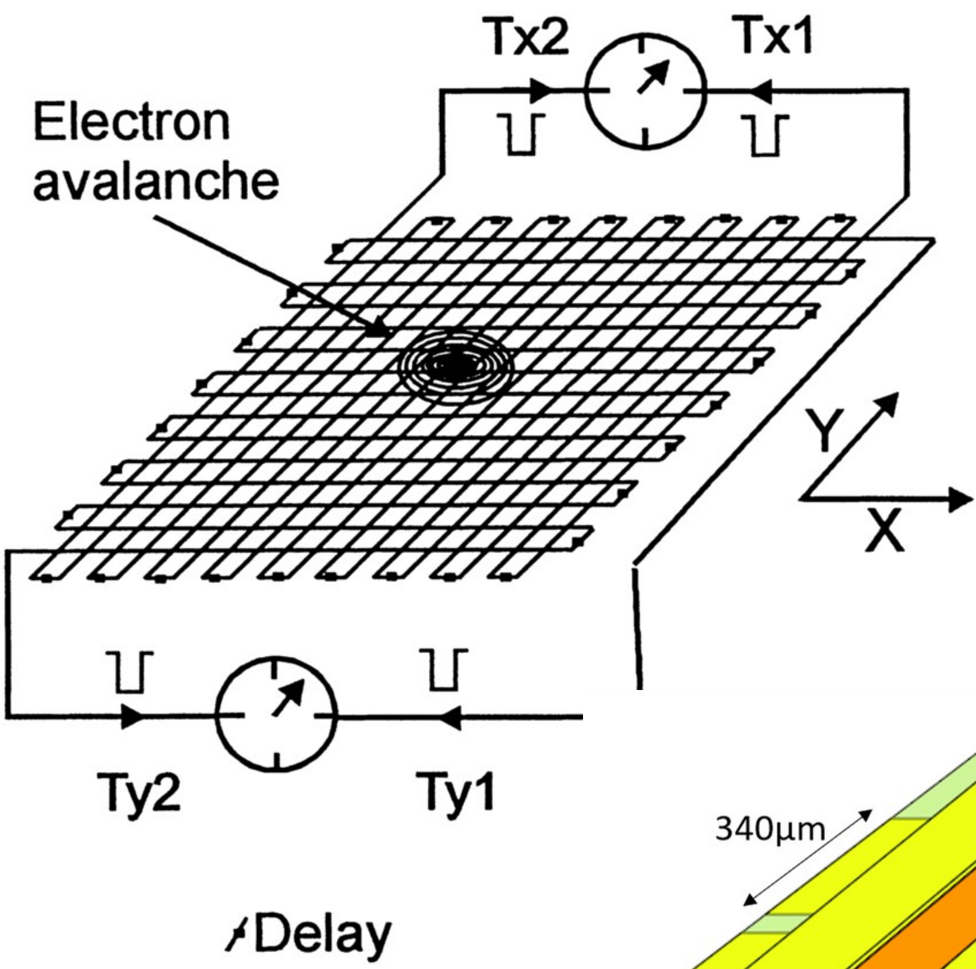
# SEGMENTED ELECTRODS

Why do we segment electrodes in a detector?

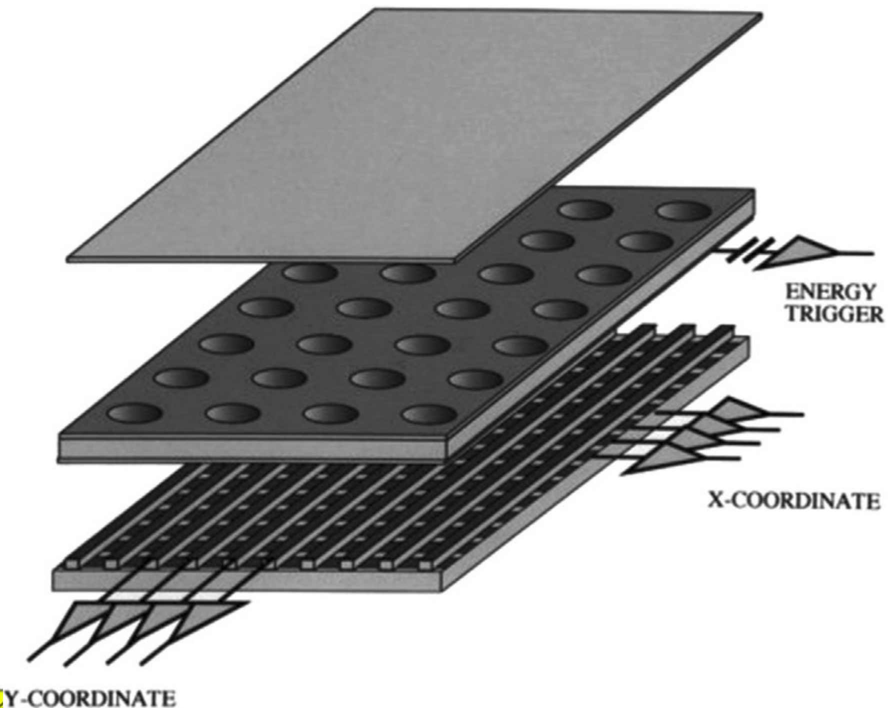
- We want to infer the ionisation position from the induced signal
  - ⇒ Get spatial position where a particle interacted with the detector
  - ⇒ Reconstruct particle trajectory
  - ⇒ Measure energy transferred to detector gas
    - ⇒ Measure energy of a photon
    - ⇒ For charged particle measeure dE/dx to identify particle type
- Spatial resolution
- Rate capability
- Detector occupancy
- Hit/Track ambiguities
- # of readout channels ⇒ electronics cost

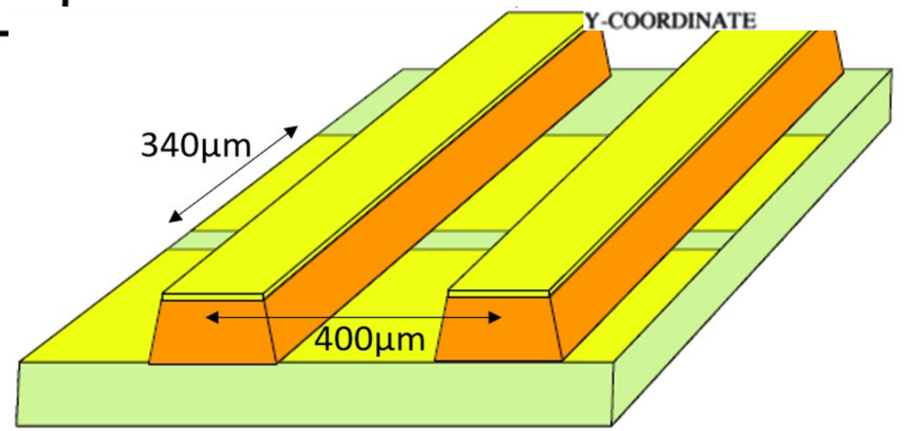
# SEGMENTED ELECTRODS: STRIPS

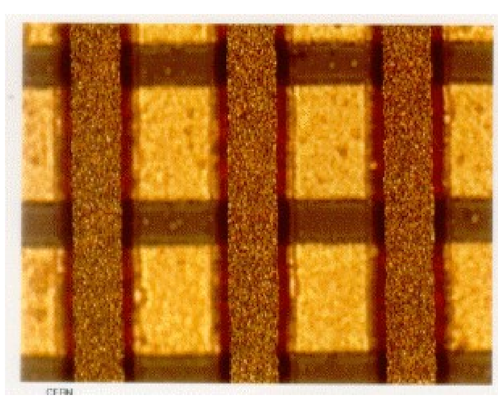
Delay line strips: 2 readout channels




x-y readout: n+m readout channels

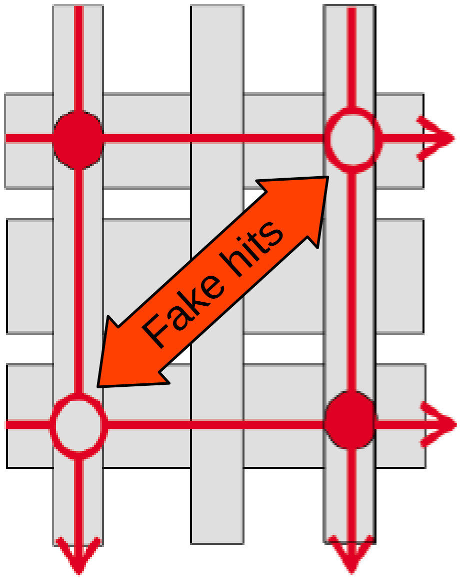


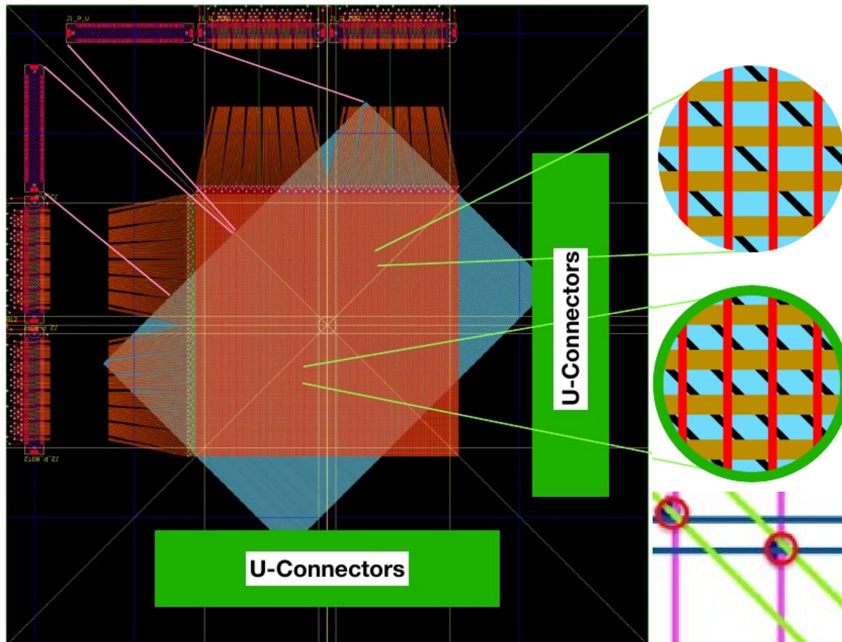



# SEGMENTED ELECTRODS: STRIPS

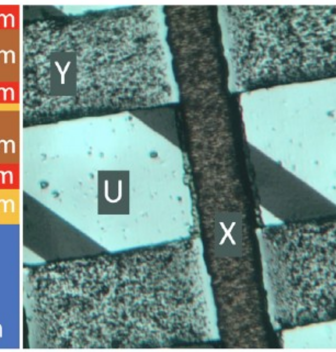
x-y-u readout: l+n+m readout channels, suggested by F. Sauli, ongoing work bei K. Flöthner

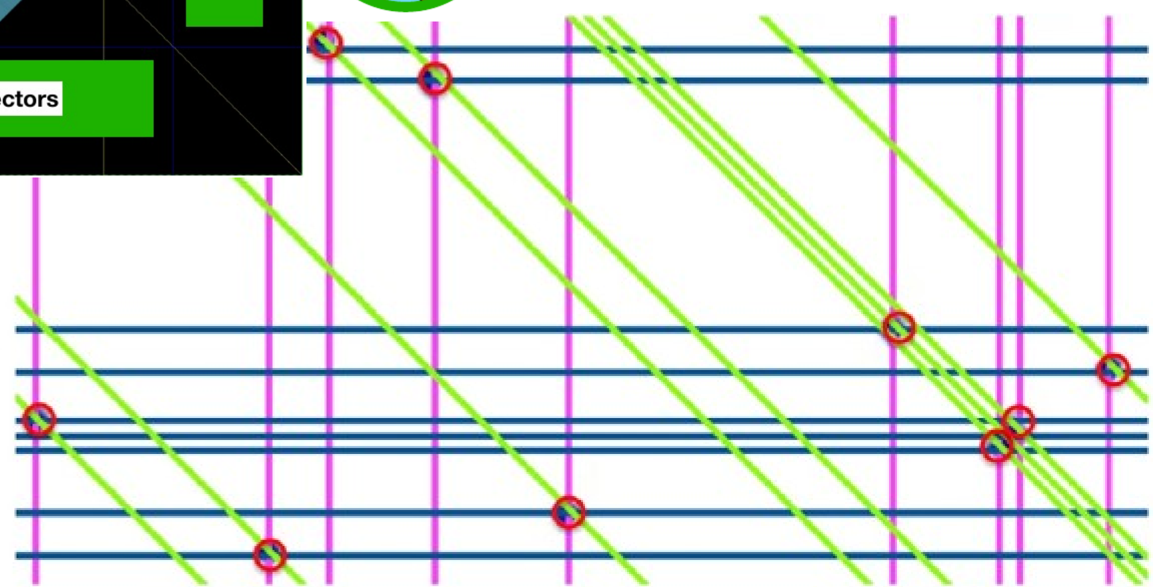



Hit ambiguity in x-y



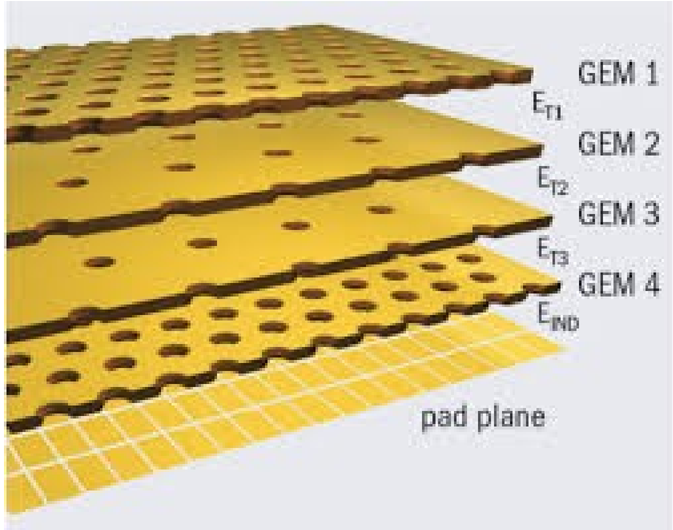


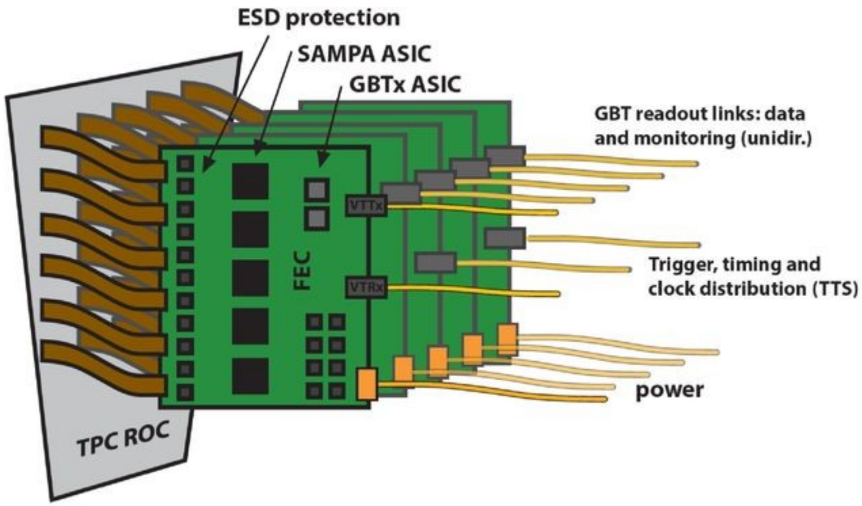


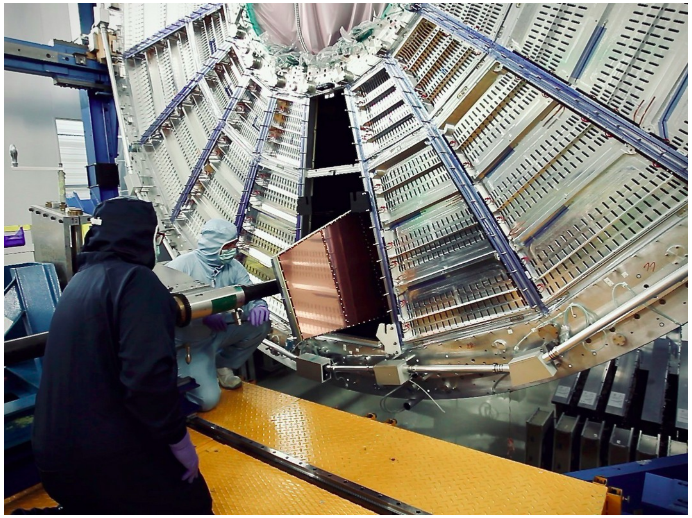



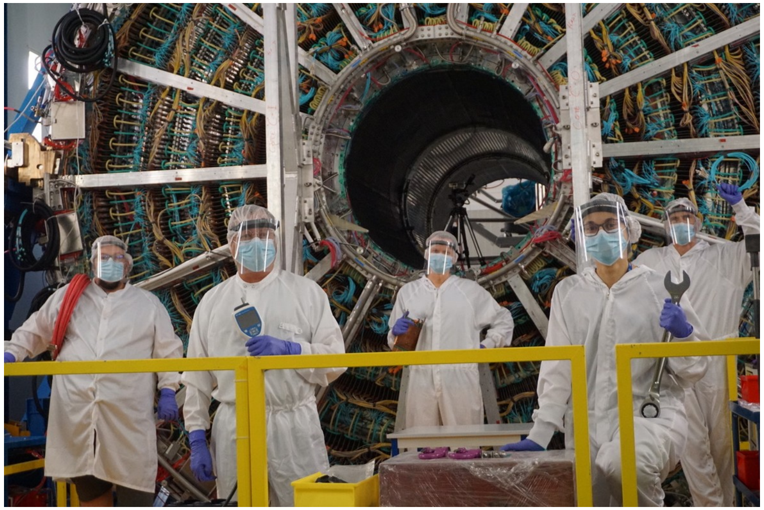
# SEGMENTED ELECTRODS: PADS

pad readout: n*m readout channels, external electronics





# SEGMENTED ELECTRODS: PADS

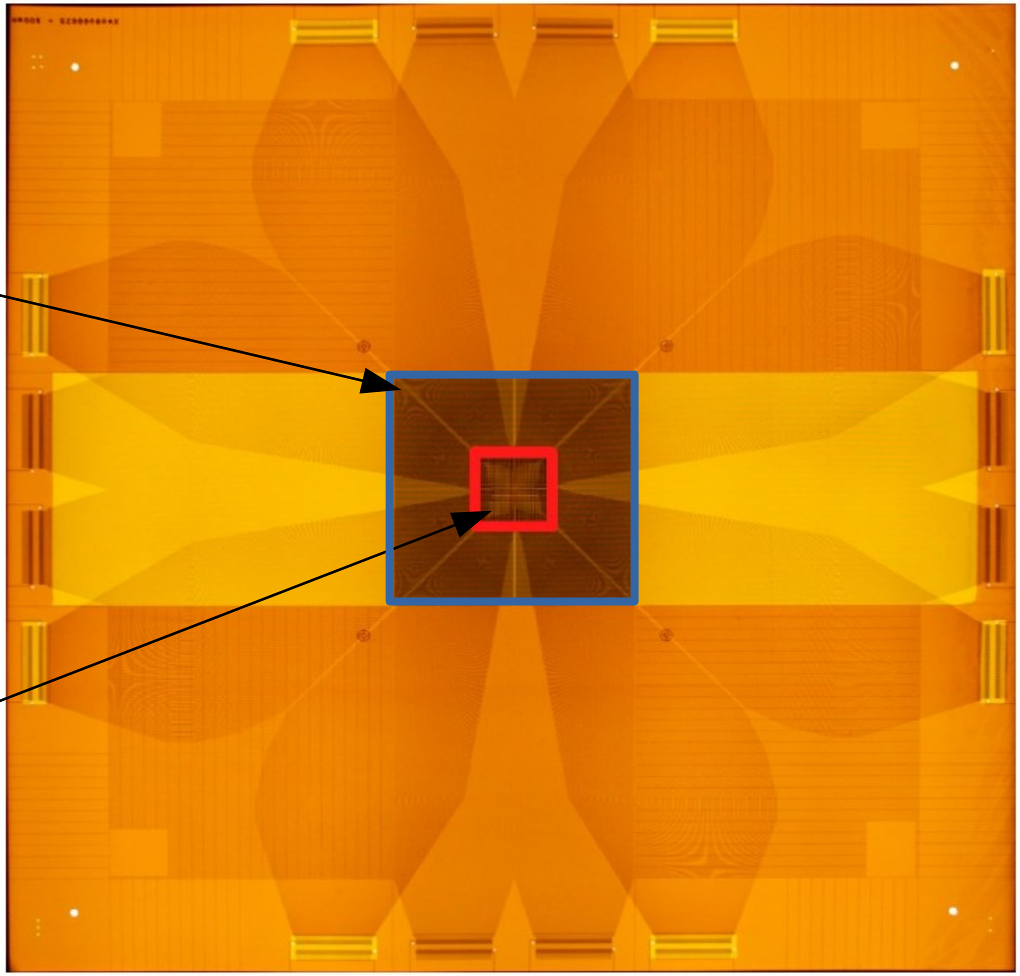
Pad + strip readout combined: COMPASS Pixel-GEM (pads in center, split strips around)

**Active area: $100 \times 100\,\mathrm{mm}^2$**

- 2 planes with each 512 strips
- Pitch: $400\,\mu\mathrm{m}$

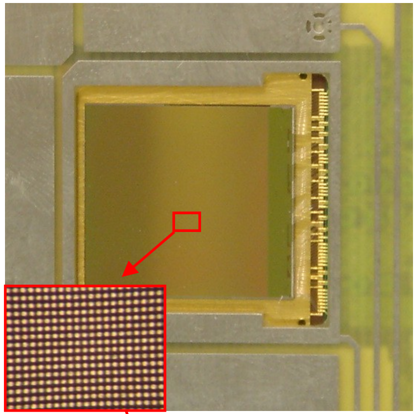
**Center: $32 \times 32\,\mathrm{mm}^2$**

- $32 \times 32$ quadratic pixel

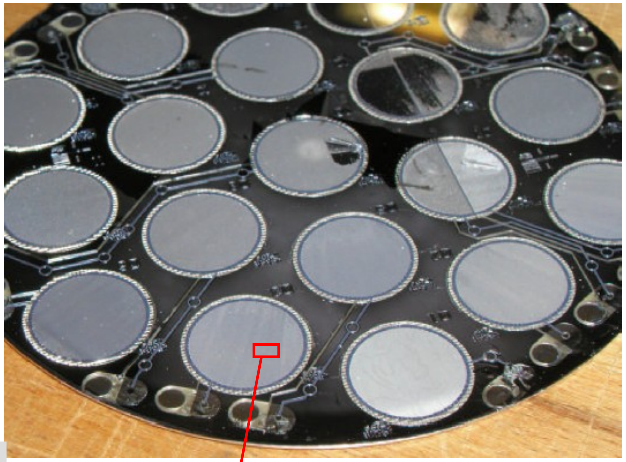


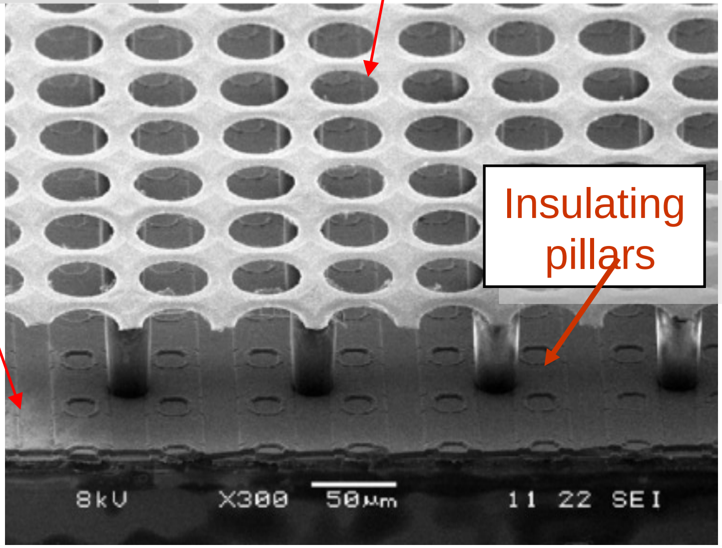
# SEGMENTED ELECTRODS: PIXELS

pad readout: n*m readout channels, integrated electronics = Pixel | GridPix

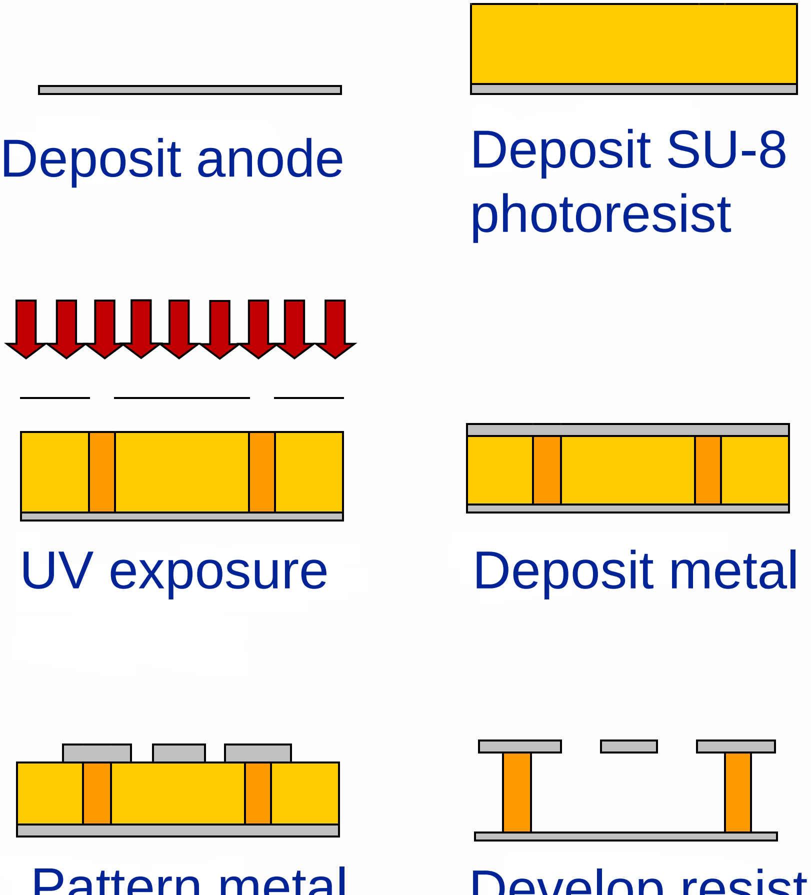


**MediPix2 / TimePix: 65k pixels, 55µm**
[X. Llopart et al., TNS 49, 2279 (2002)]

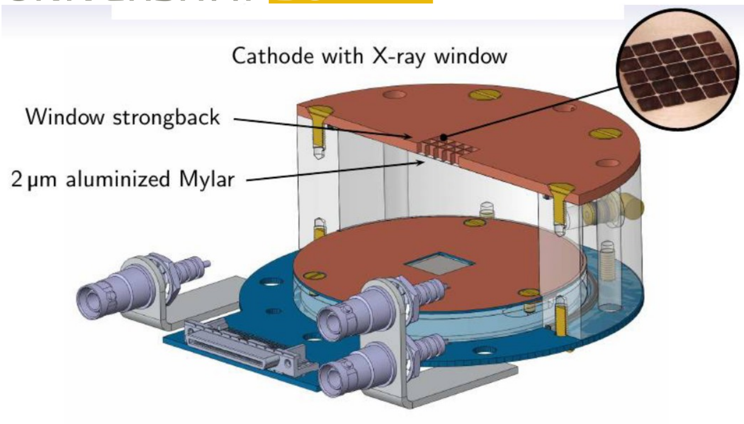


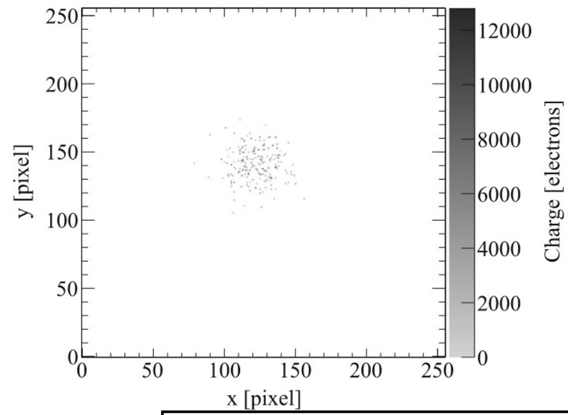


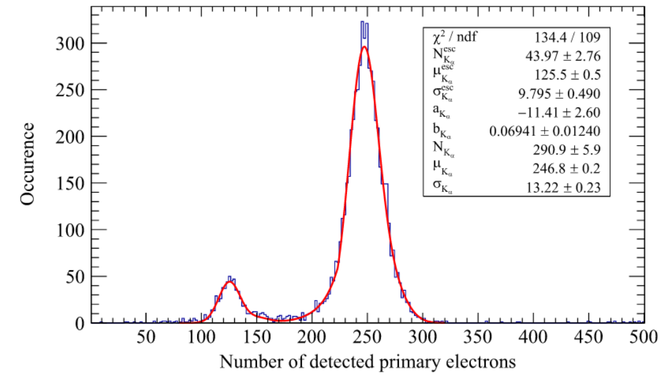

Integrated Micromegas and Pixel Sensor
(Si wafer post-processing & MEMS)
[J. Timmermans, VCI 2007]



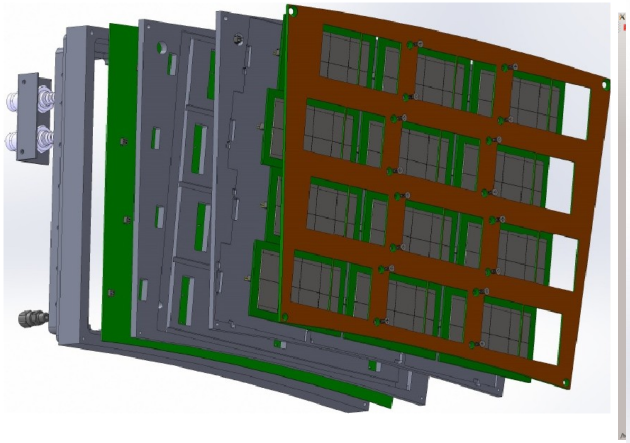
# GRIDPIX & THE PIXEL-TPC

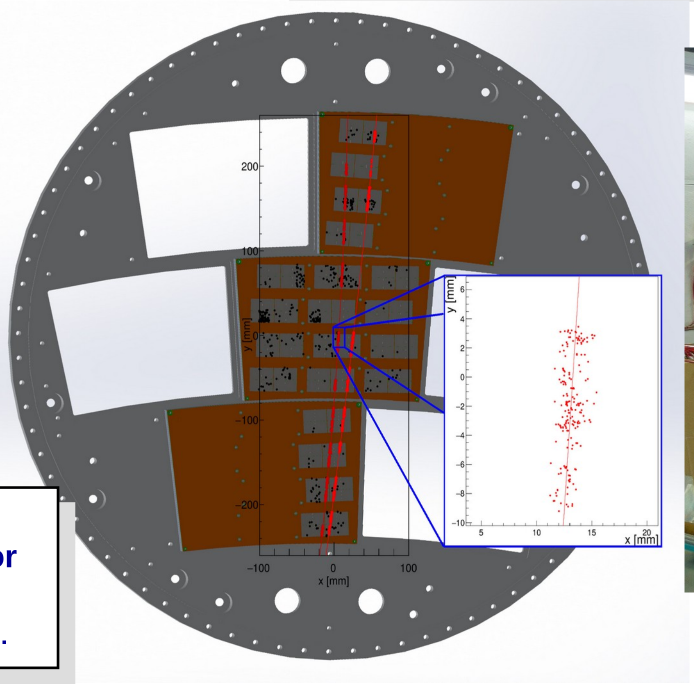


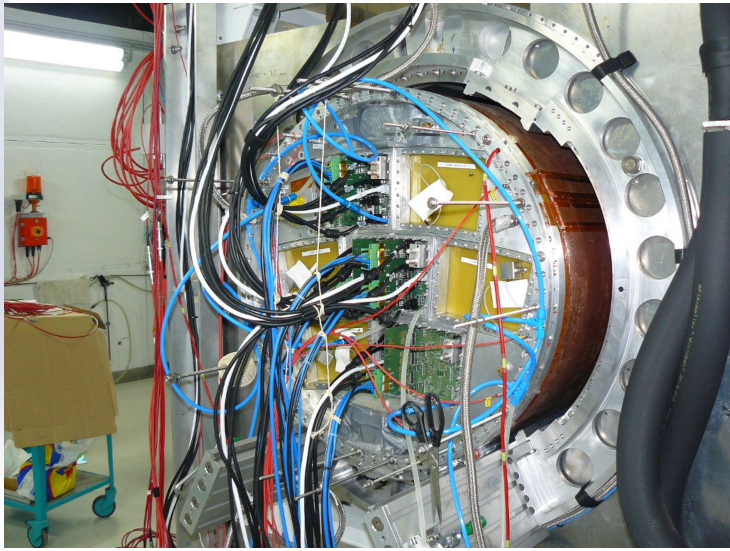




**A GridPix-based X-ray detector for the CAST experiment**
[C. Krieger, J. Kaminski, M. Lupberger, K. Desch, NIMA 867 (2017) 101]



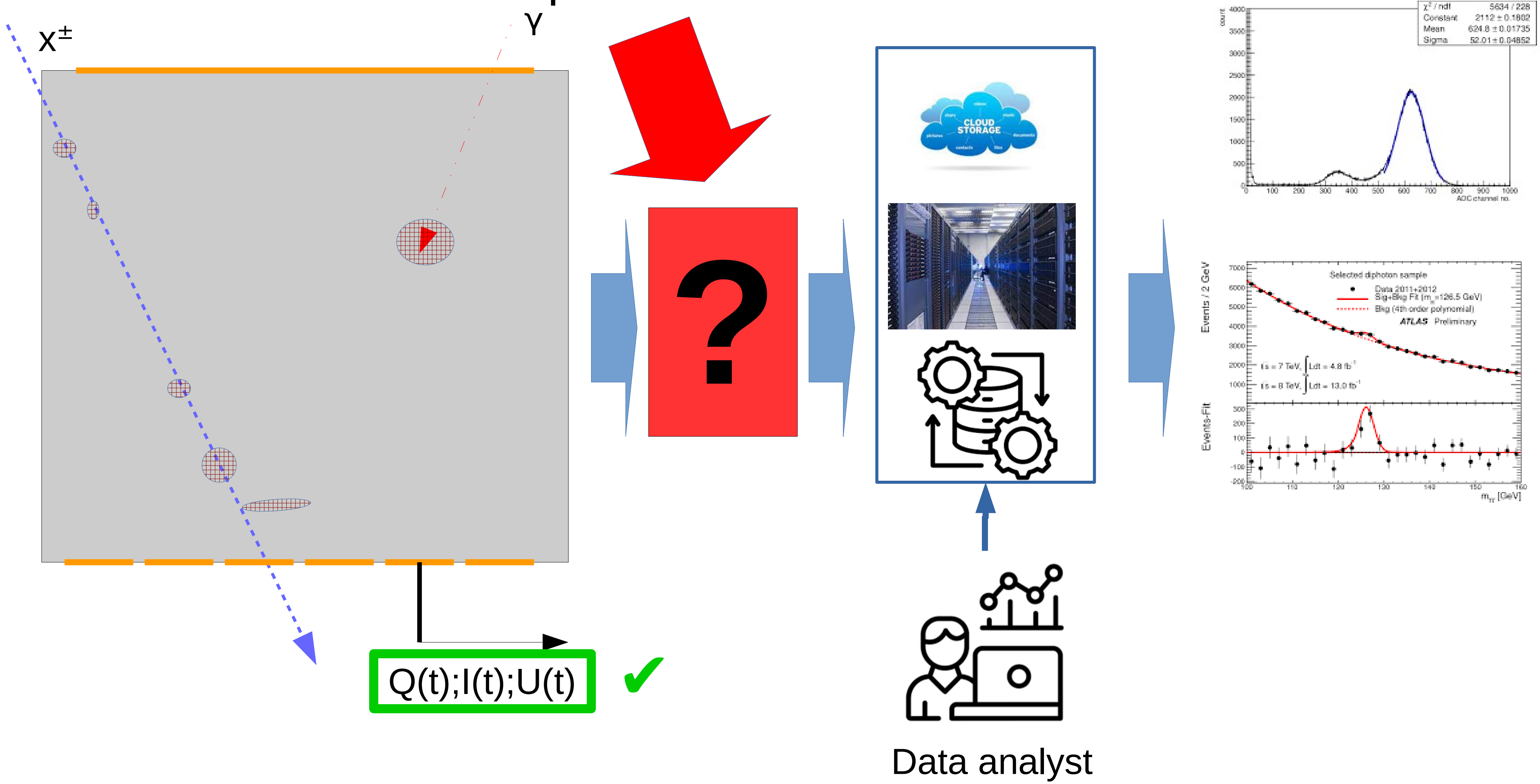


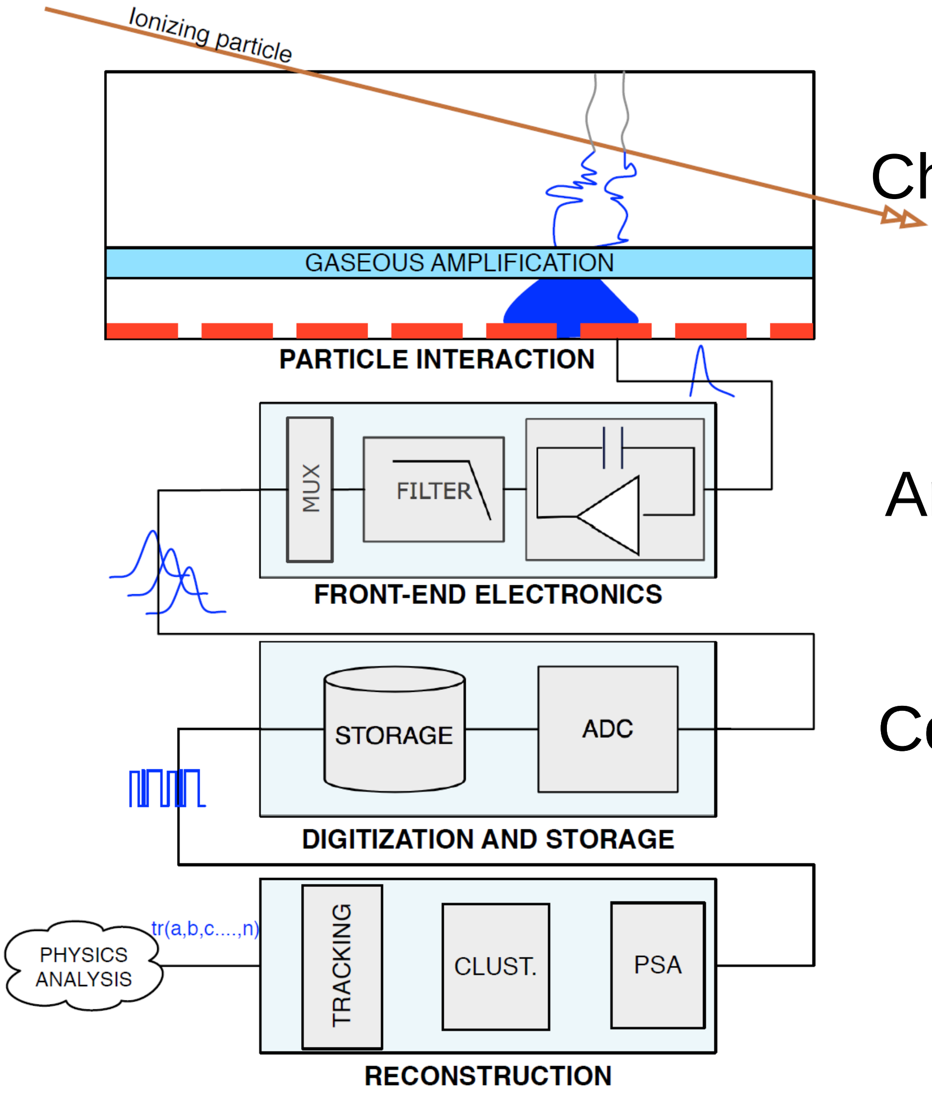
**Toward the Pixel-TPC: Construction and Operation of a Large Area GridPix Detector**
[M. Lupberger et al., M. Lupberger et al.
EEE Trans. Nucl. Sci 64.5 (2017) 1159-1167.
]

# ELECTRONIC READOUT OVERVIEW

## Electronic readout techniques



# ELECTRONIC READOUT OVERVIEW



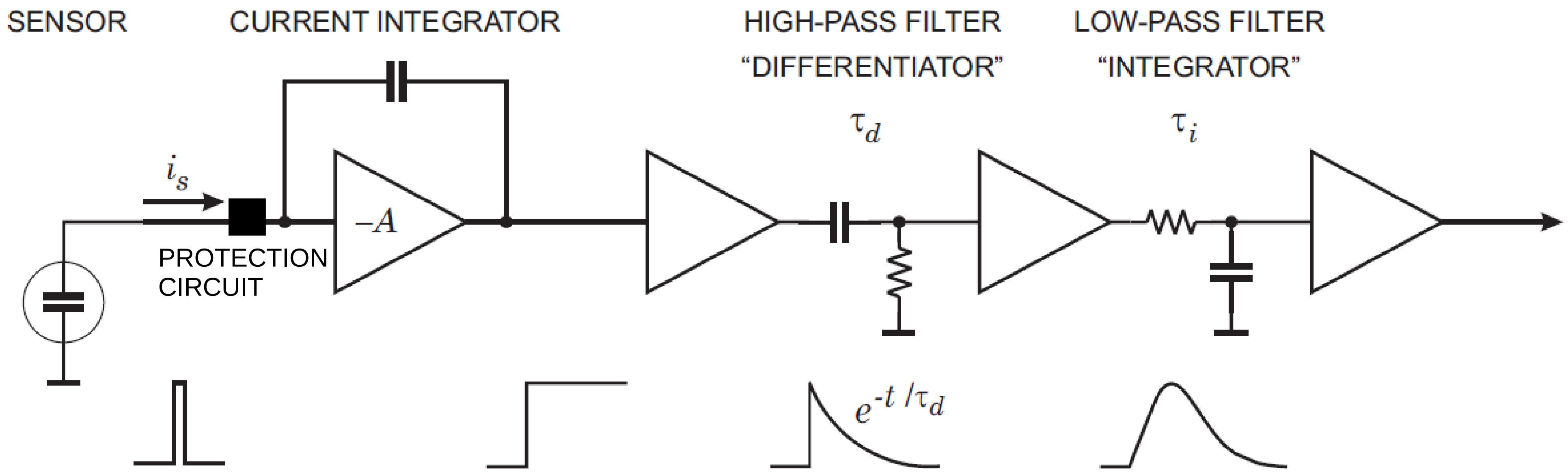

Charge induction

Analogue electronics

Conversion to digital

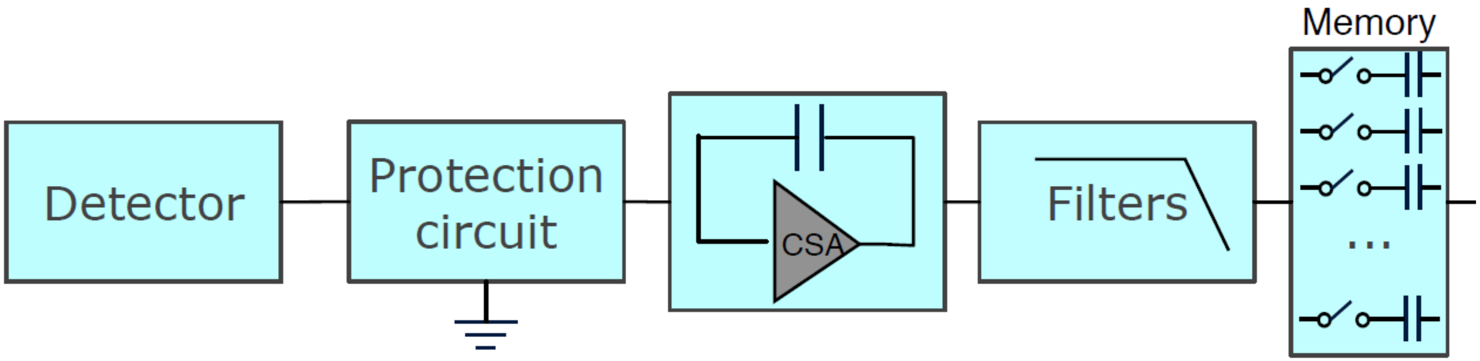
[M Vandenbroucke, PhD thesis, TUM, 2012]

# Example analogue readout chain




[H. Spieler, Semiconductor Detector Systems, Oxford 2005]

# ANALOGUE ELECTRONICS




Purpose of pulse processing:

1. Acquire electrical signal from detector, typically a short current pulse
2. Optimise time response of the system to enhance:
- Minimum detectable signal (yes/no) → S/N ratio
- Energy measurement → Linearity
- Event rate → Dead time/Throughput
- Time of arrival (timing) → Time-invariance/Stability
- Insensitivity to sensor pulse shape → Linearity
3. Digitize signal and store for subsequent analysis

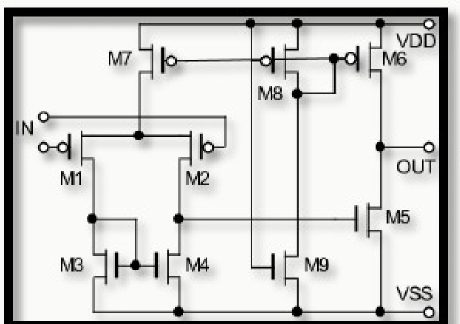
Layout of such a system heavily depends on application!

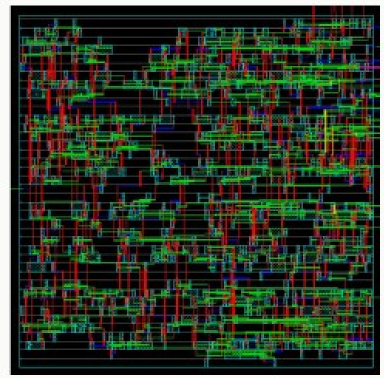
# MULTI-CHANNEL READOUT

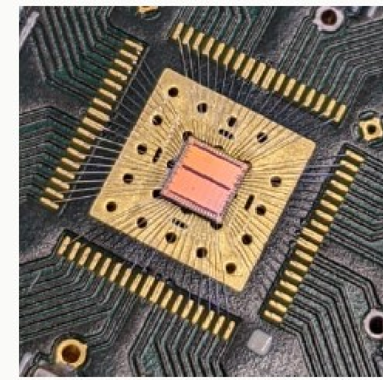
## Application Specific Integrated Circuit (ASIC)

From: Introduction to ASIC design / A. Walsemann / FTD Electronics Seminar, Bonn

```
    ff_proc: process (clk)
    begin
      if (clk = '1' and clk'event) then
        q <= d;
      end if;
    end process ff_proc;
```





Floorplan

↓

Placement

↓

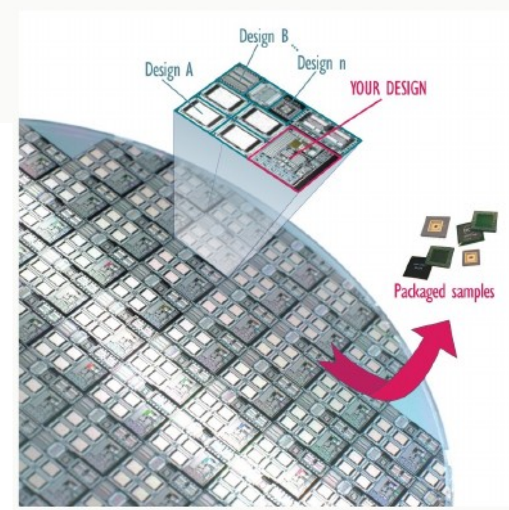
Clock-tree Synthesis

↓

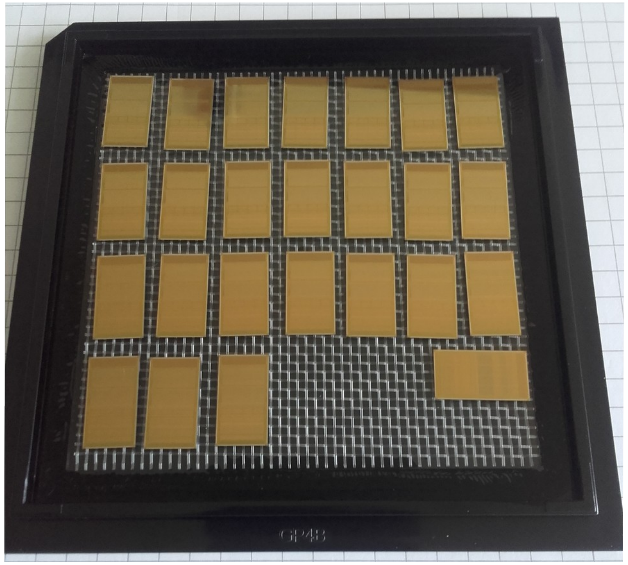
Signal Routing

↓

Optimization

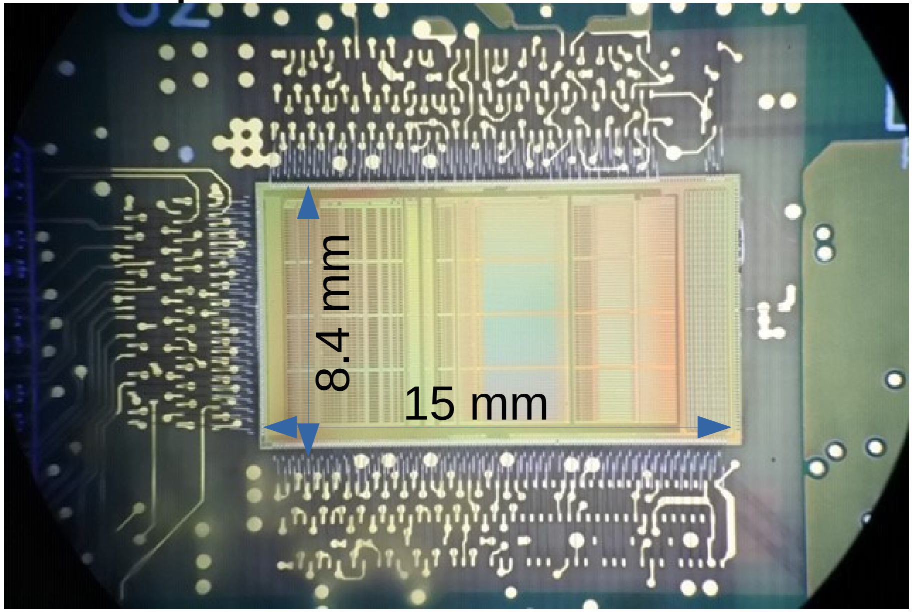


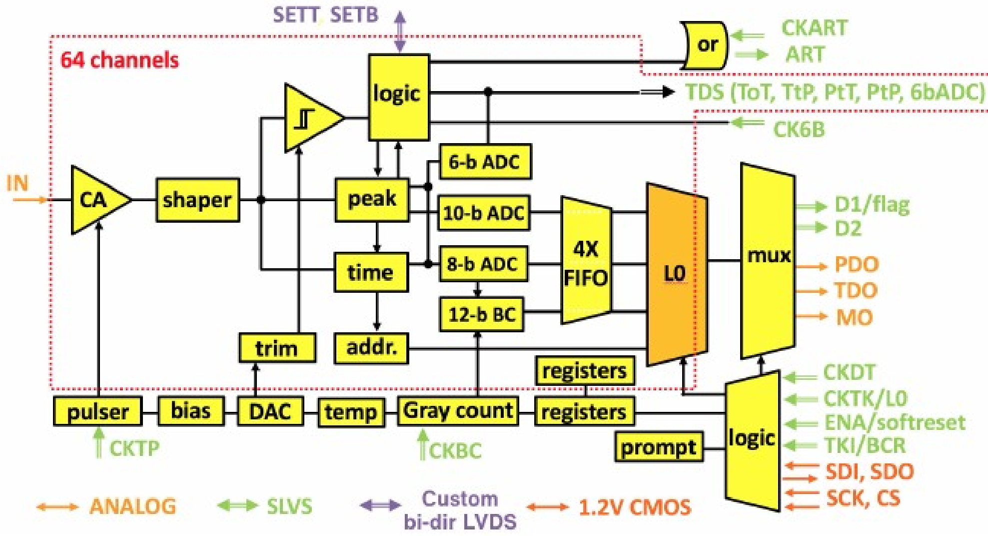
# MULTI-CHANNEL READOUT: STRIPS



## Gaseous detector readout

- High rates and large #channels → little space
  ⇒ discrete components → integrated circuit (IC)
- Application Specific Integrated Circuits (ASIC)
- ASIC connected to strips/pads
  Example: VMM3a



# MULTI-CHANNEL READOUT: STRIPS

UNIVERSITÄT BONN

## The VMM front-end ASIC - **Evolution**


- **Mixed-signal**
- 2-phase readout with external ADC
- **peak** and **timing** information
- neighbouring readout
- sub-hysteresis **discrimination**
- few timing outputs


- Mixed-signal
- **Continuous** readout
- Current-output peak detector
- **Increased** range of **gains**
- **Three ADCs** per channel
- FIFOs, **serialised data with DDR**

- Serialised ART with DDR
- Additional timing modes
- **64 timing outputs**
- Additional functions and fixes

**VMM3a - Production Version !**


~10mW/channel

- **LVL0 pipeline** and buffering for ATLAS
- **SEU-tolerant logic**
- **Revised front-end** for high charge and capacitance (2nF, 50pC, fast recovery)
- SLVS signals
- Reset controls
- **Timing at threshold**
- Timing ramp optimisation
- Ion **tail suppressor** (fast recovery)
- Int. Pulser range extension
- ART synchronisation to BC clock
- **VMM3a fixed open bugs** from VMM3 and introduce some stability fixes on the ADCs and Front-end

BGA 400, 1mm


- ***The VMM was designed at BNL G. De Geronimo in collaboration with IFIN-HH S. Martoiu (L0) (recent version VMM3a, at DG Circuits on behalf of BNL)***
- ***It is fabricated in the 130nm Global Foundries 8RF-DM process (former IBM 8RF-DM)***

U.S. DEPARTMENT OF ENERGY

3

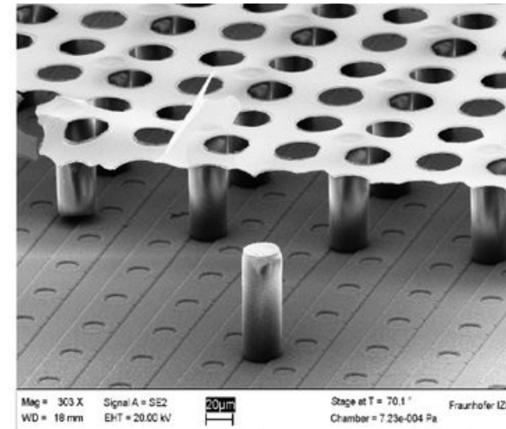
BROOKHAVEN NATIONAL LABORATORY

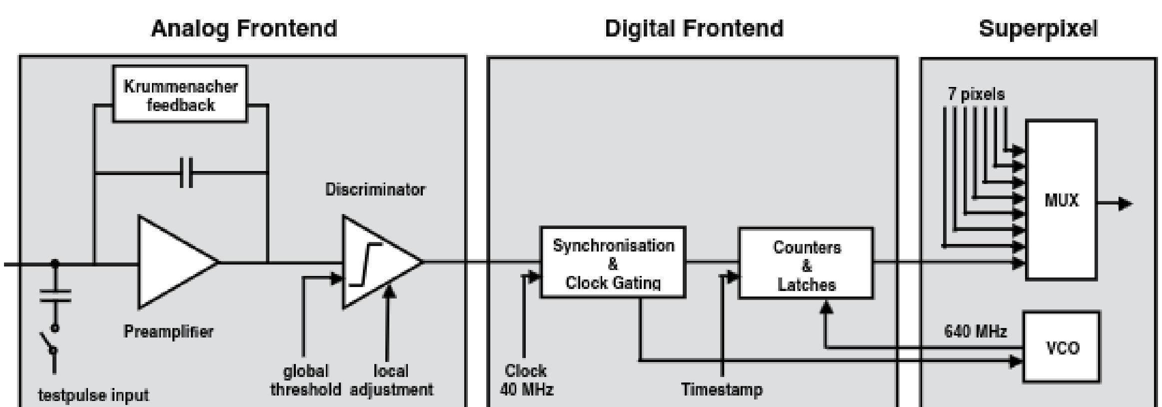
From: George Iakovidis, Presentation given at the RD51 Meeting 2021

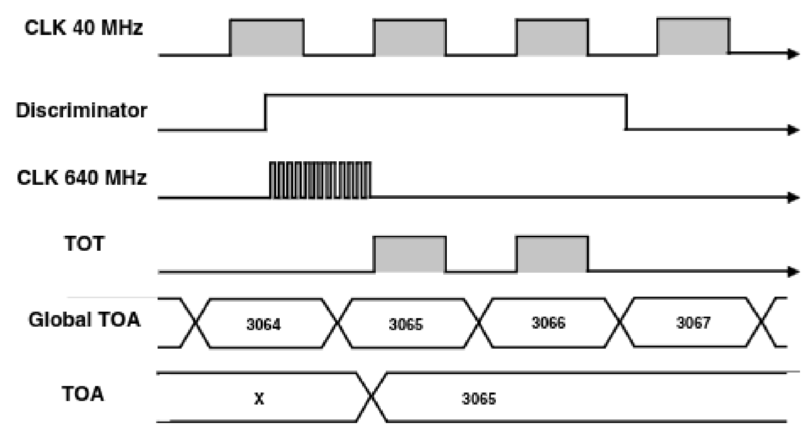
# MULTI-CHANNEL READOUT: PIXEL

## Gaseous detector readout

- High rates and large #channels → little space
  ⇒ discrete components → integrated circuit (IC)
- Application Specific Integrated Circuits (ASIC)
- Example of fully integrated gaseous detector:
  GridPix = Timepix(3)ASIC + Micromegas

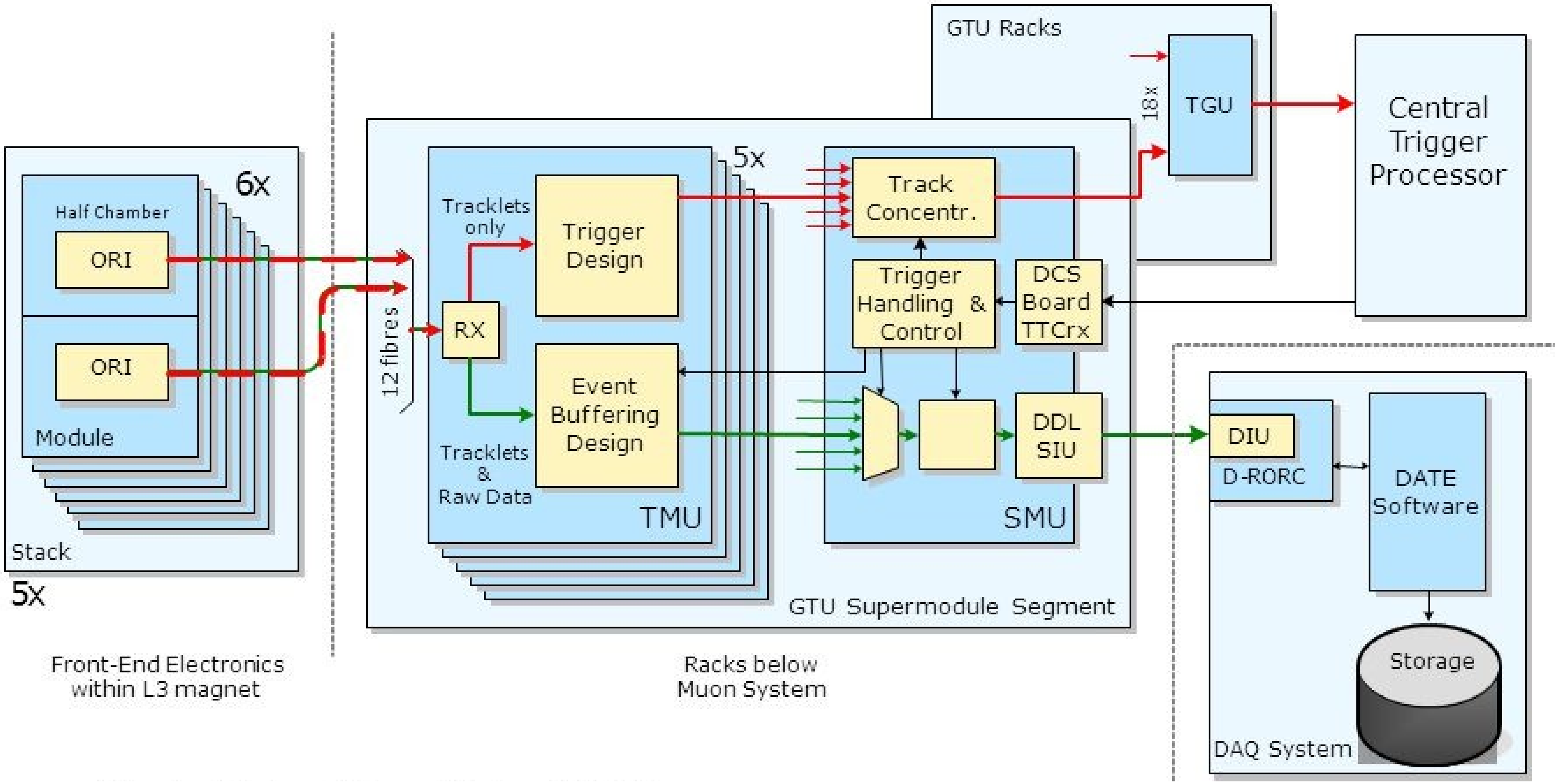




# UP THE READOUT CHAIN

General readout chain (Example: ALICE muon system)



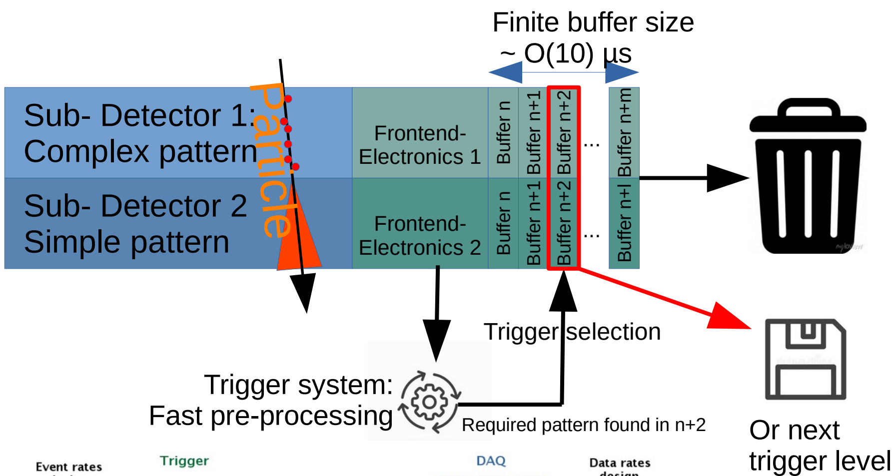

Fronted

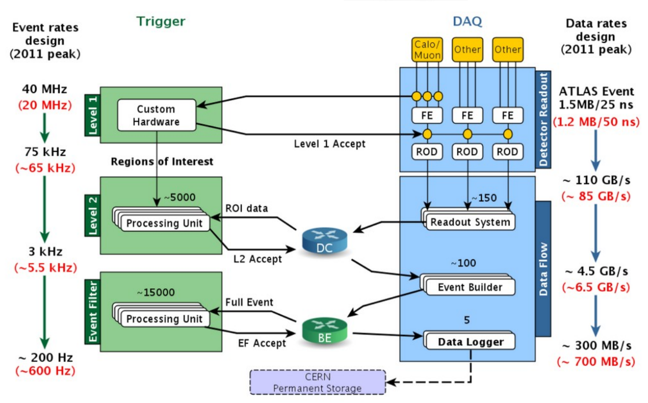
Concentrator

Storage

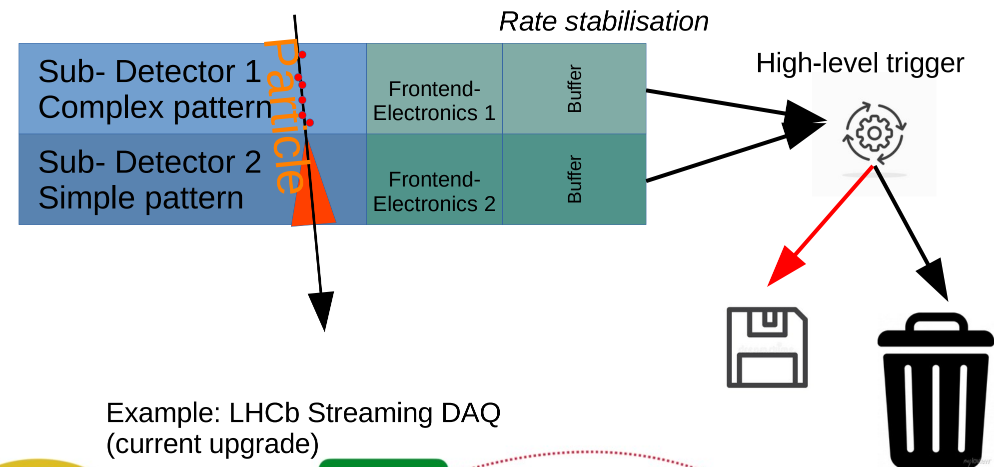
# UP THE READOUT CHAIN

## Triggered vs streaming DAQ

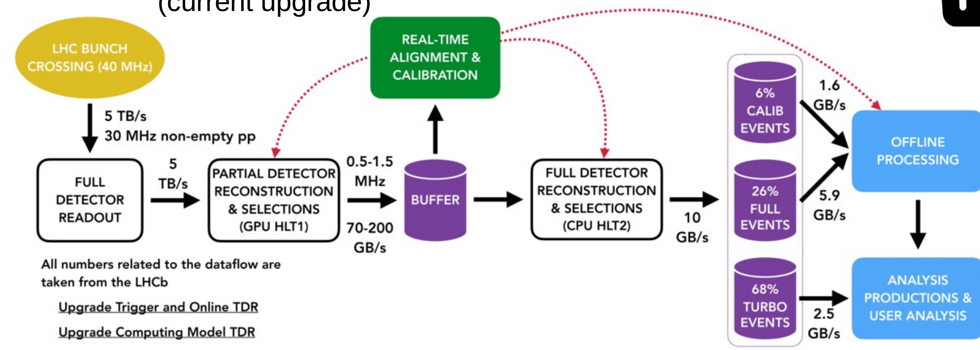



Example:
ATLAS TDAQ
(original)




Example: LHCb Streaming DAQ
(current upgrade)




Both need fast, high-troughput parallel-processing
→ FPGA

# UP THE READOUT CHAIN: FPGA

From: A. Zibell, M. Lupberger, RD51 electronics school 2012

FPGA : Field Programmable Gate Array
→ can be reprogrammed at any time (unlike ASICs)
→ array of logic gates

- A gate implements a basic logic function, like OR, AND, NAND, etc...
- Any logic function, complex or not, can be built from a number of interconnected „gates“.
- With enough gates (even of a single type) it is possible to build up any type of digital circuitry (even processors)

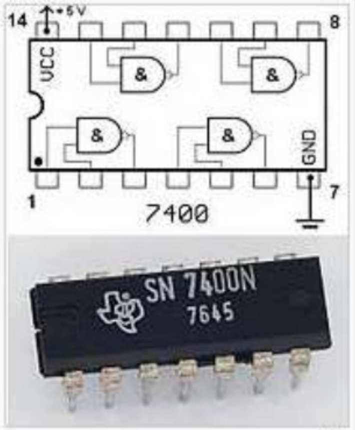
| INPUT | | OUTPUT |
|---|---|---|
| A | B | A NAND B |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A NOR B |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A OR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A AND B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| INPUT | OUTPUT |
|---|---|
| A | NOT A |
| 0 | 1 |
| 1 | 0 |

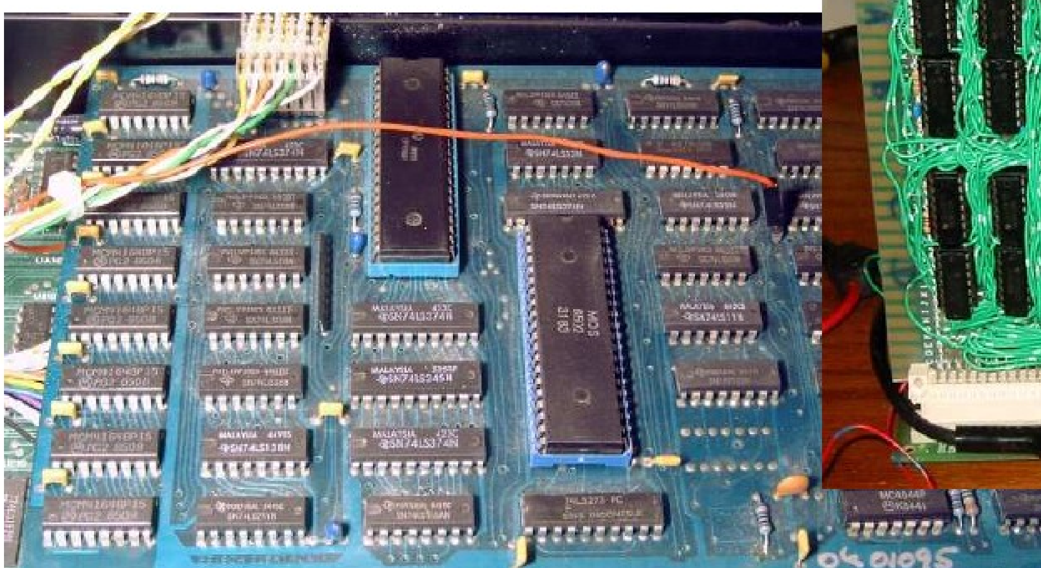


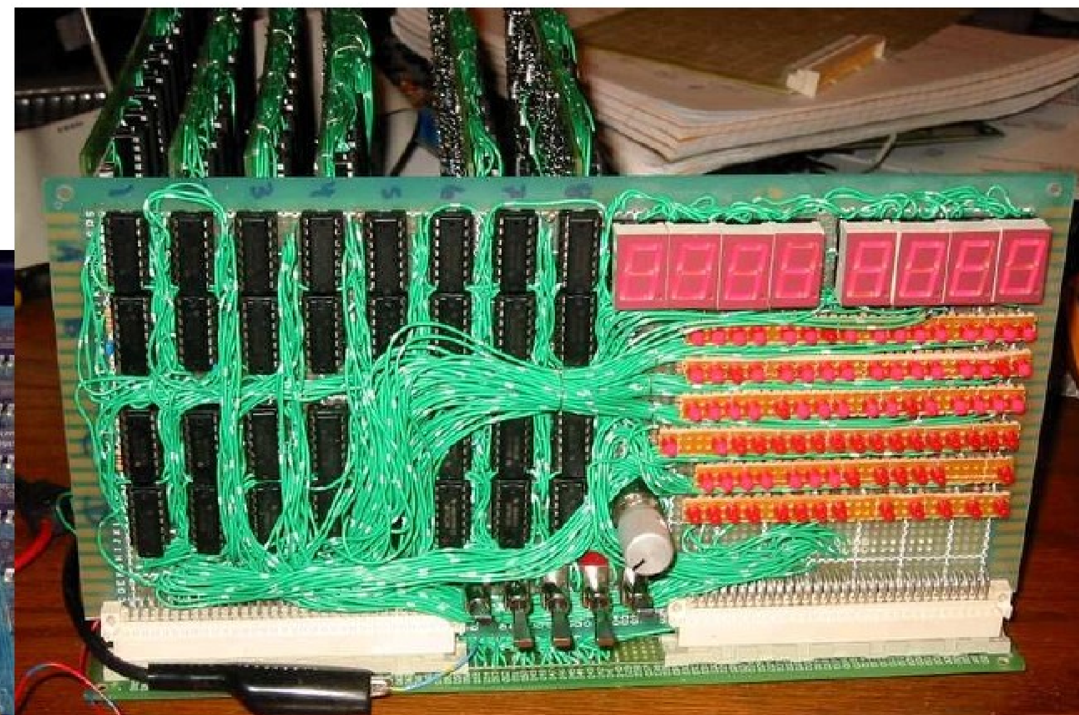

The 7400 chip, containing four NANDs. The two additional pins supply power (+5 V) and connect the ground.

# UP THE READOUT CHAIN: FPGA

From: A. Zibell, M. Lupberger, RD51 electronics school 2012

Digital electronics in the 70's
- Use of may logic gate chips, to perform complex operations
- Wire routing difficult and prone to errors
- Limited functionality due to available board space





# UP THE READOUT CHAIN: FPGA

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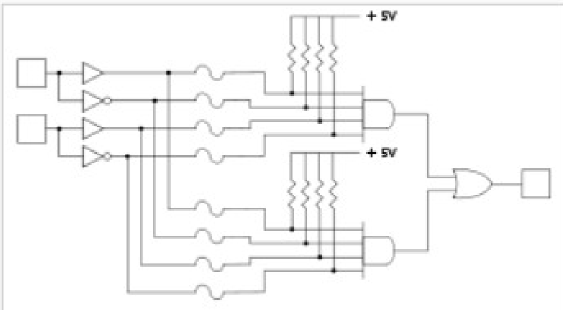
From: A. Zibell, M. Lupberger, RD51 electronics school 2012

## Evolution of logic density

- Chips, that contain several (different) logic gates that were cascadable
- Programmable Array Logic by burning fuses (PAL, late 70‘s):
  One-time-programmable interconnection of „dozens of logic gates“
- Generic Array Logic (GAL, 1985)
  Replaces several PALs, re-programmable
- Complex Programmable Logic Device (CPLD)
  Contain hundreds of logic gates, hundreds of pins
- FPGAs
  Contain many thousand (or million) logic gates and much more...




Simplified programmable logic device

A simplified PAL device. The programmable elements (shown as a fuse) connect both the true and complemented inputs to the AND gates. These AND gates, also known as product terms, are ORed together to form a sum-of-products logic array.


Lattice GAL 16V8 and 20V8

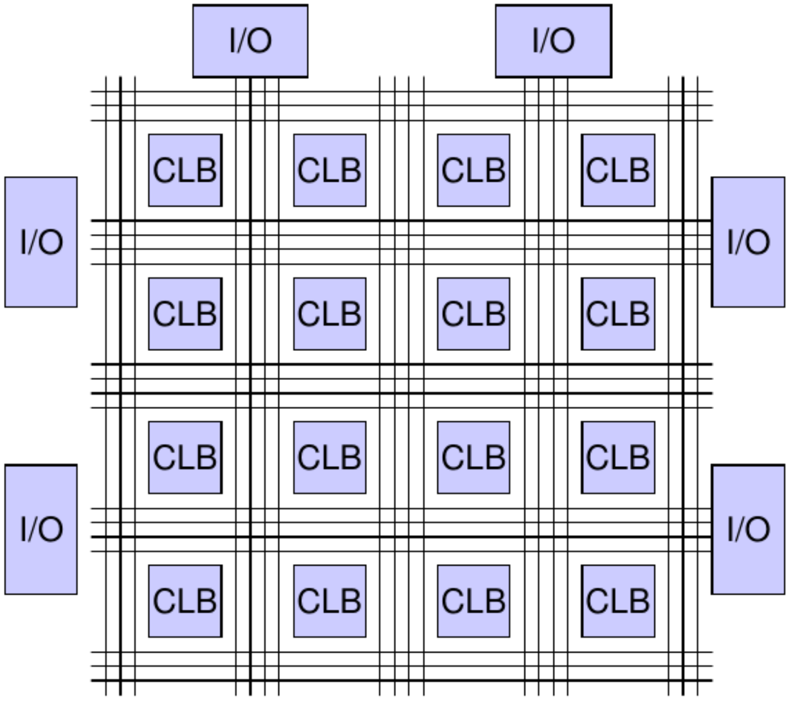

An Altera MAX 7000-series CPLD with 2500 gates.

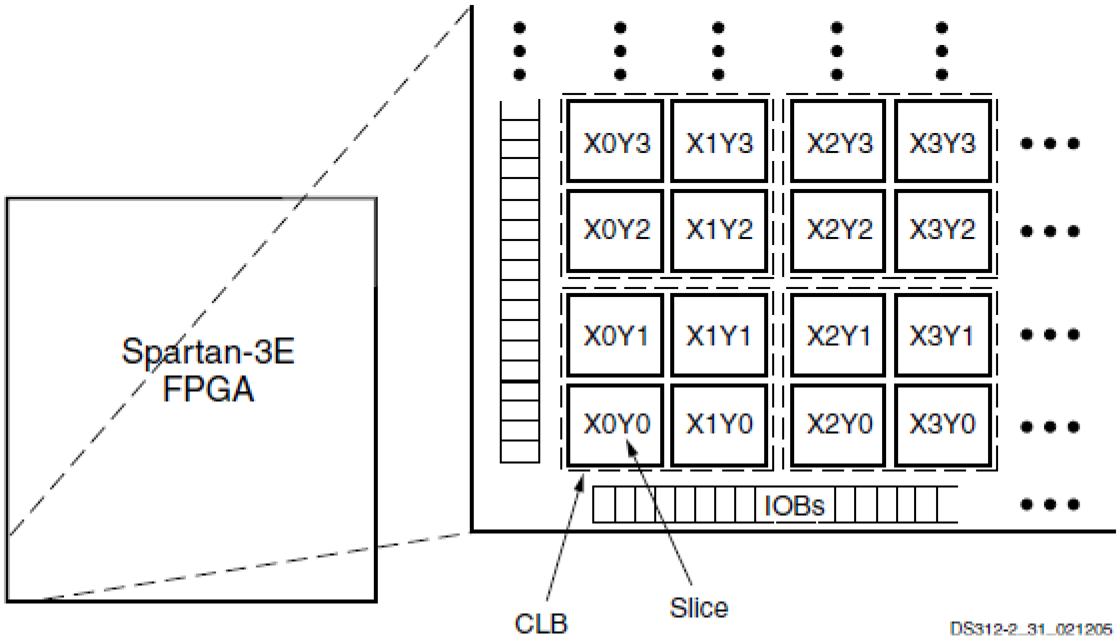
# UP THE READOUT CHAIN: FPGA

From: A. Zibell, M. Lupberger, RD51 electronics school 2012

## FPGA Layout

- Contains a very (!) large number of „Configurable Logic Blocks“ (CLB)
- Programmable interconnection matrix propagates signals in between blocks
- I/O blocks connect to the world outside of the FPGA
- Modern FPGAs contain much more powerful components!



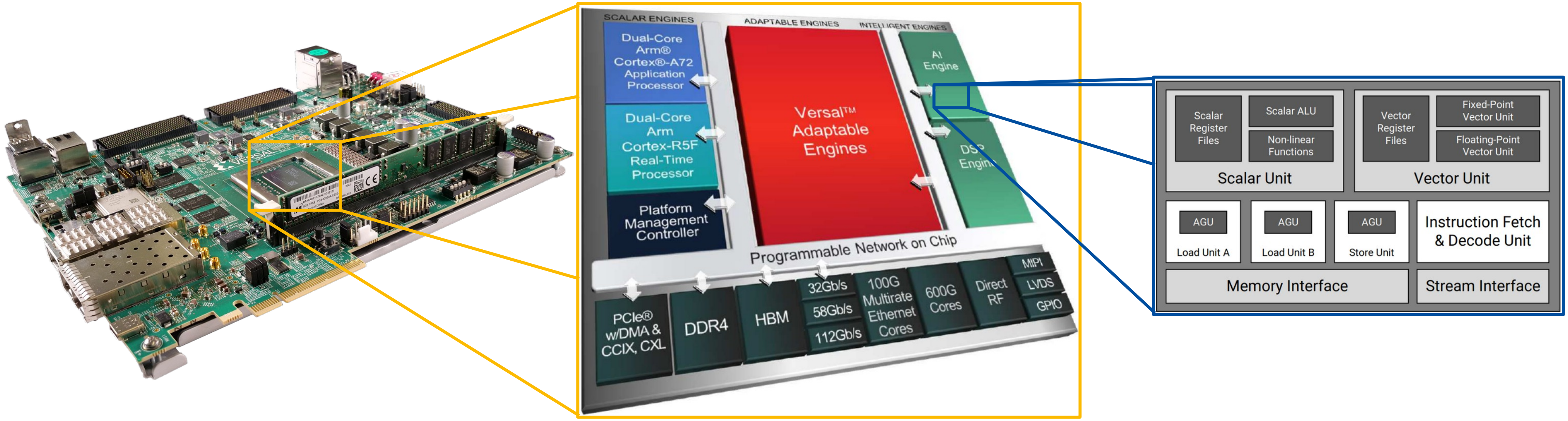



# UP THE READOUT CHAIN: FPGA

From: A. Zibell, M. Lupberger, RD51 electronics school 2012

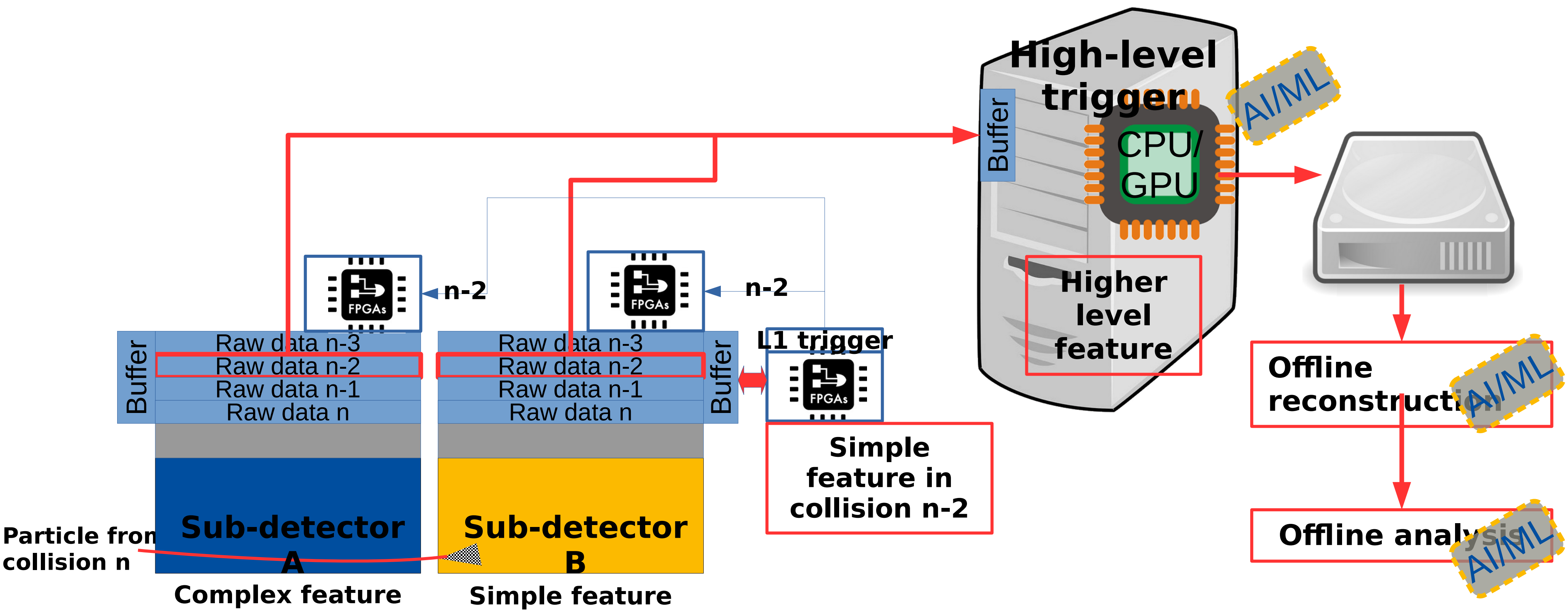
## Latest Technology: AMD Versal AI

- 400 AI processors (“AI engines”)
- FPGA (“Adaptable Engines”): 2k DSPs, nearly 2M logic cells
- Arm CPU, Arm RPU (“Scalar Engines”)



# UP THE READOUT CHAIN

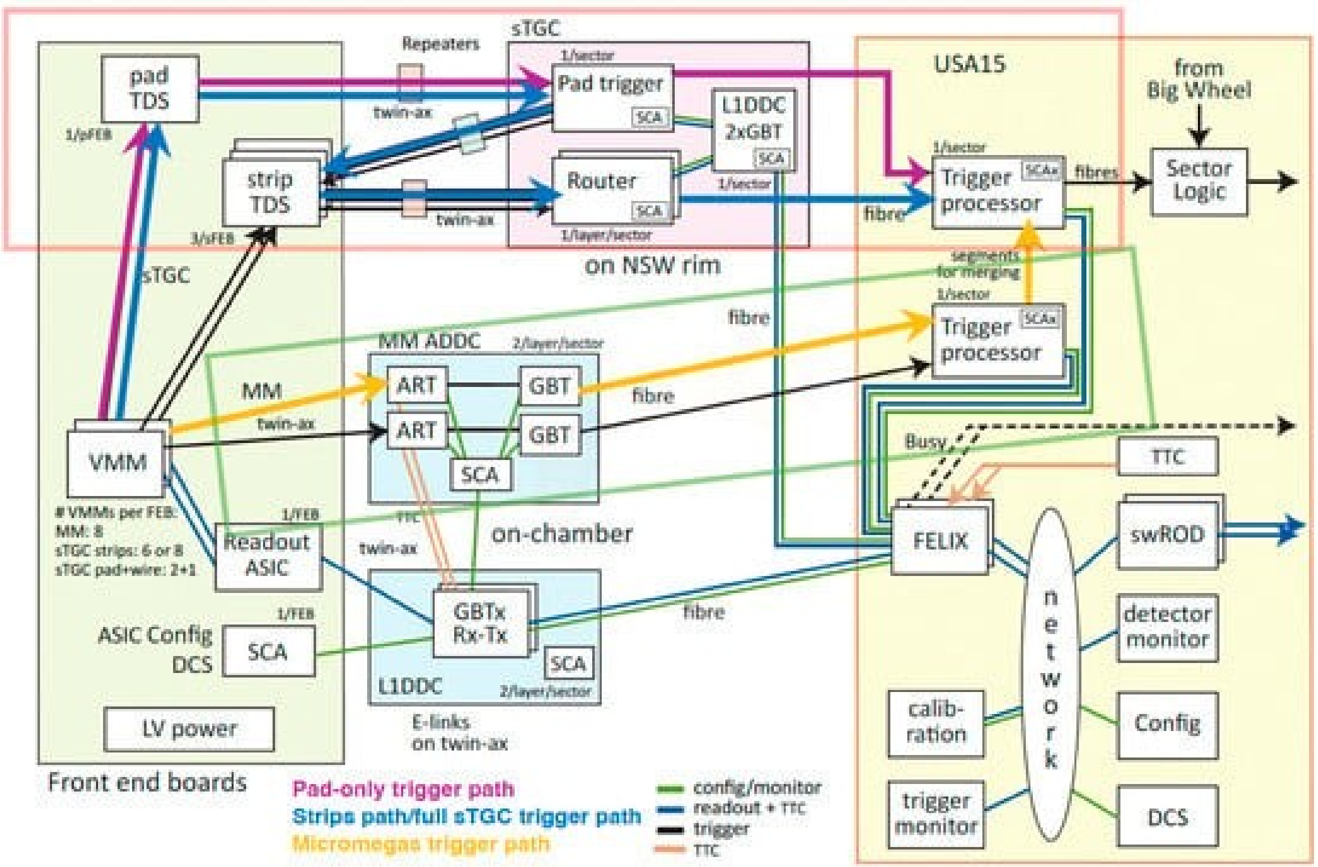
Machine learing in the readout chain

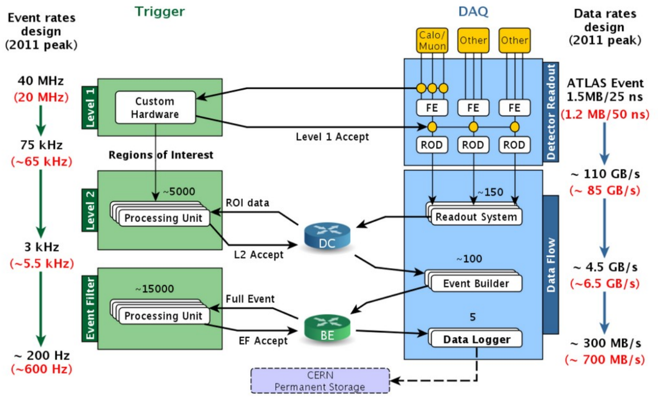



Trend: Move AI to detector

# UP THE READOUT CHAIN

## Example: ATLAS NSW electronics in TDAQ



# DRD1 COMMON READOUT: SRS

2011 IEEE Nuclear Science Symposium Conference Record N43-5

## Front-end electronics for the Scalable Readout System of RD51

S. Martoiu, *Member, IEEE,* H. Muller, and J. Toledo

***Abstract*– Recent developments in micro-pattern gas detector technologies have considerably broadened the interest in this type of detectors, extending their application field from high-energy physics to nuclear, astrophysical, geophysical, medical or industrial applications, to name just a few. Historically, for the wide range of gas amplification schemes available, there has been an almost equally wide amount of electronic readout solutions, tailored on just one application, making it rather difficult for newcomers to employ the technology. Developed within RD51 Collaboration for the Development of Micro-Pattern Gas Detectors Technologies, the Scalable Readout System (SRS) is intended as a general purpose multi-channel readout solution for a wide range of detector types, and detector complexities, as well as for different experimental environments.**

### II. The SRS Concept

The Scalable Readout System is designed around a bivalent scalability concept, which refers to both applications range and system size. Not limited to a single detector technology, the system needs to respond to a wide range of detector requirements, in terms of sensitivity, time resolution, event rate capability, trigger concept, radiation or magnetic tolerance, etc. In the same time the SRS concept has to allow the integration of small prototype detectors, as well as large area detectors in a wide range of experimental environments.

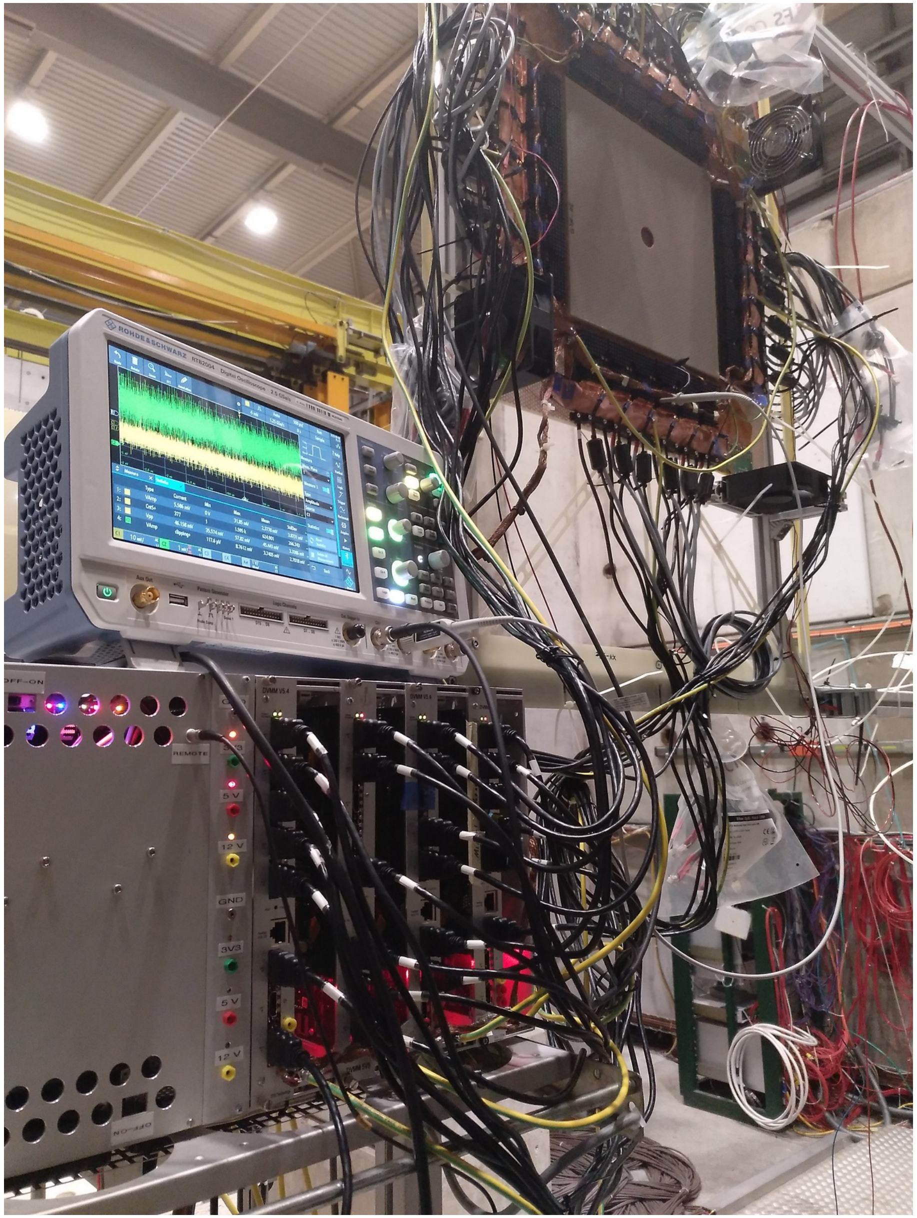
*A. Application-Range Scalability*

# WHAT IS SRS

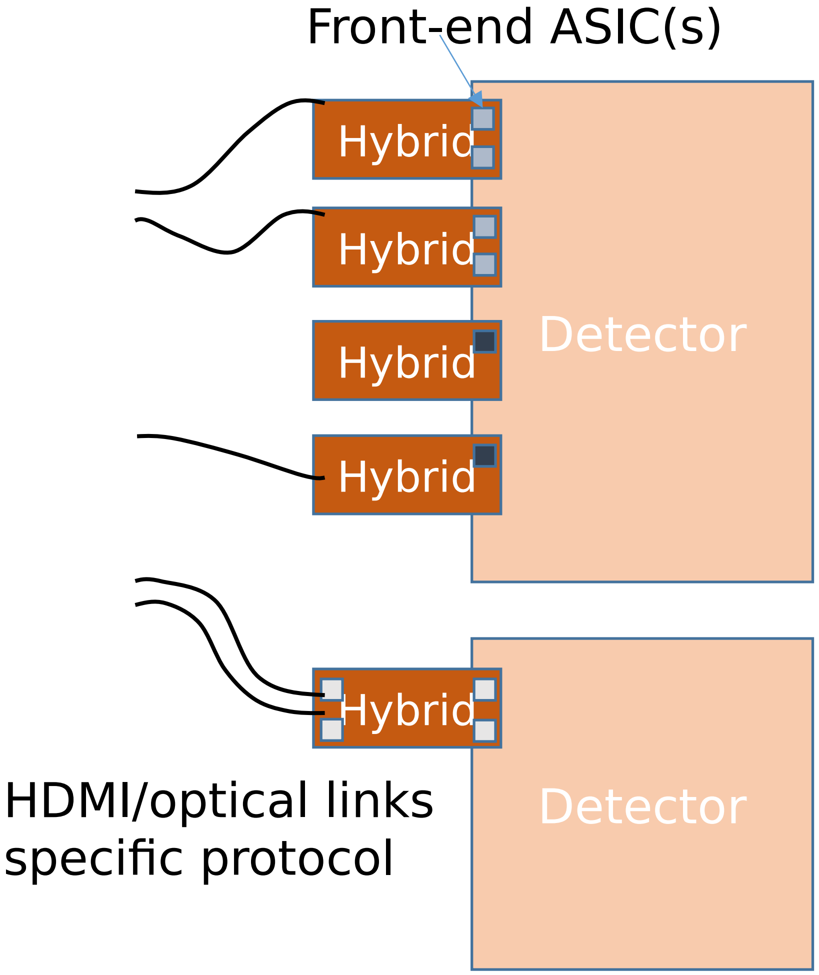
Scalable Readout System:

- A generic readout system for laboratory and detector instrumentation
- Developed and supported by the RD51 Collaboration since 2009 (Inventor: H. Müller)
- Standardised multi-purpose data acquisition system
- Different front-end chips supported
- Constantly extended, improved, adapted to needs from community by community
- Exceptional common long-term project of RD51

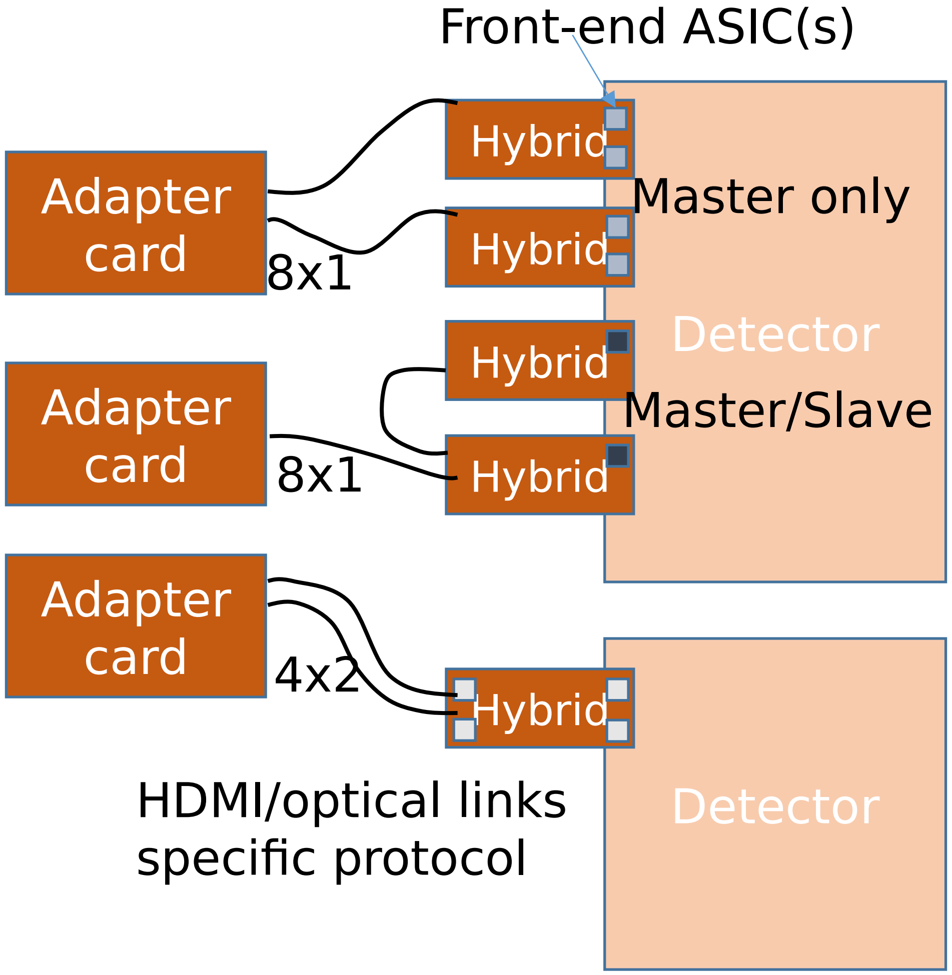
⇒ used in many MPGD groups for R&D
and also some (upcoming) experiments



# WHAT IS SRS

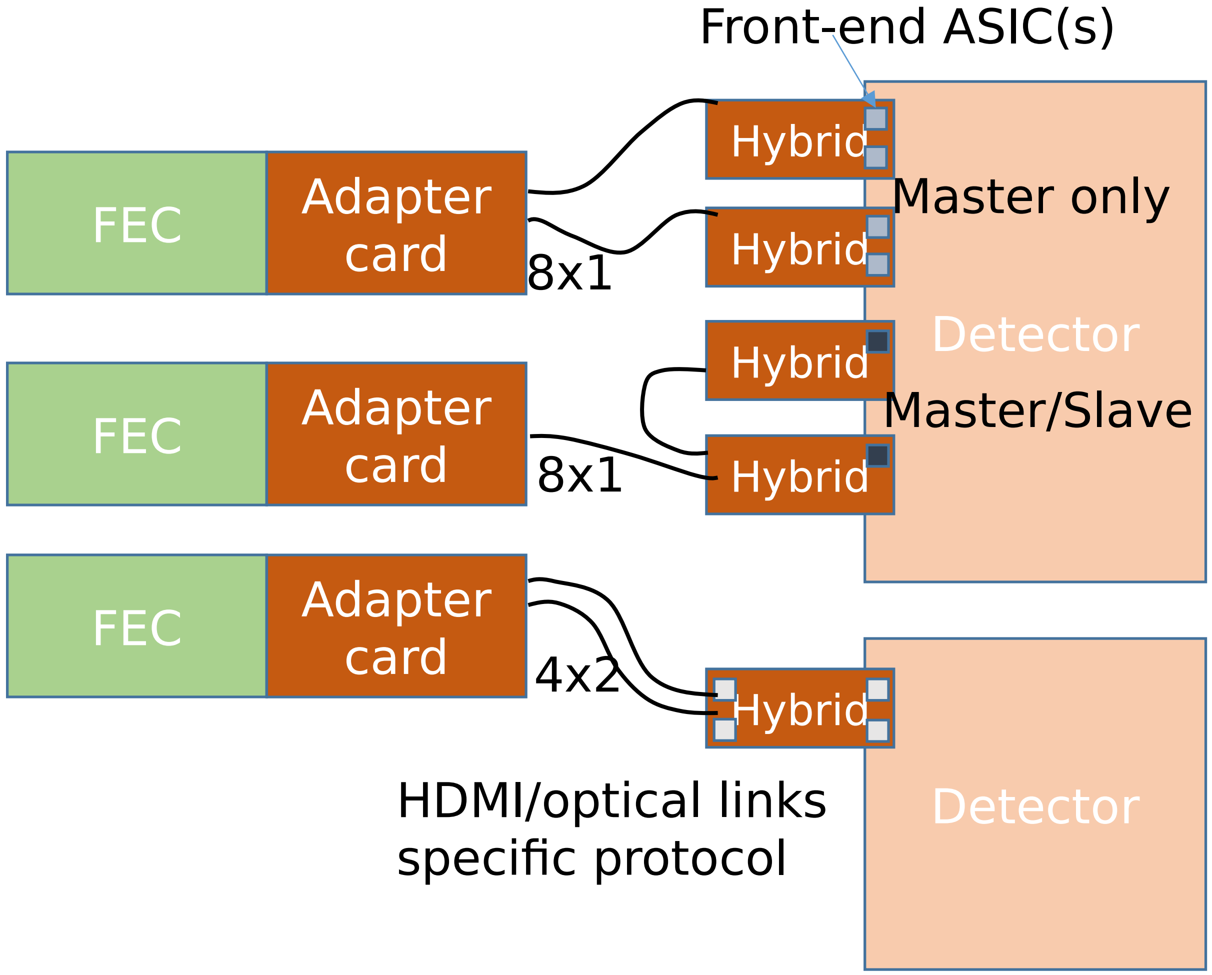

Front-end ASIC(s)
Hybrid
Hybrid
Hybrid
Hybrid
Detector
Hybrid
Detector
HDMI/optical links
specific protocol

# WHAT IS SRS



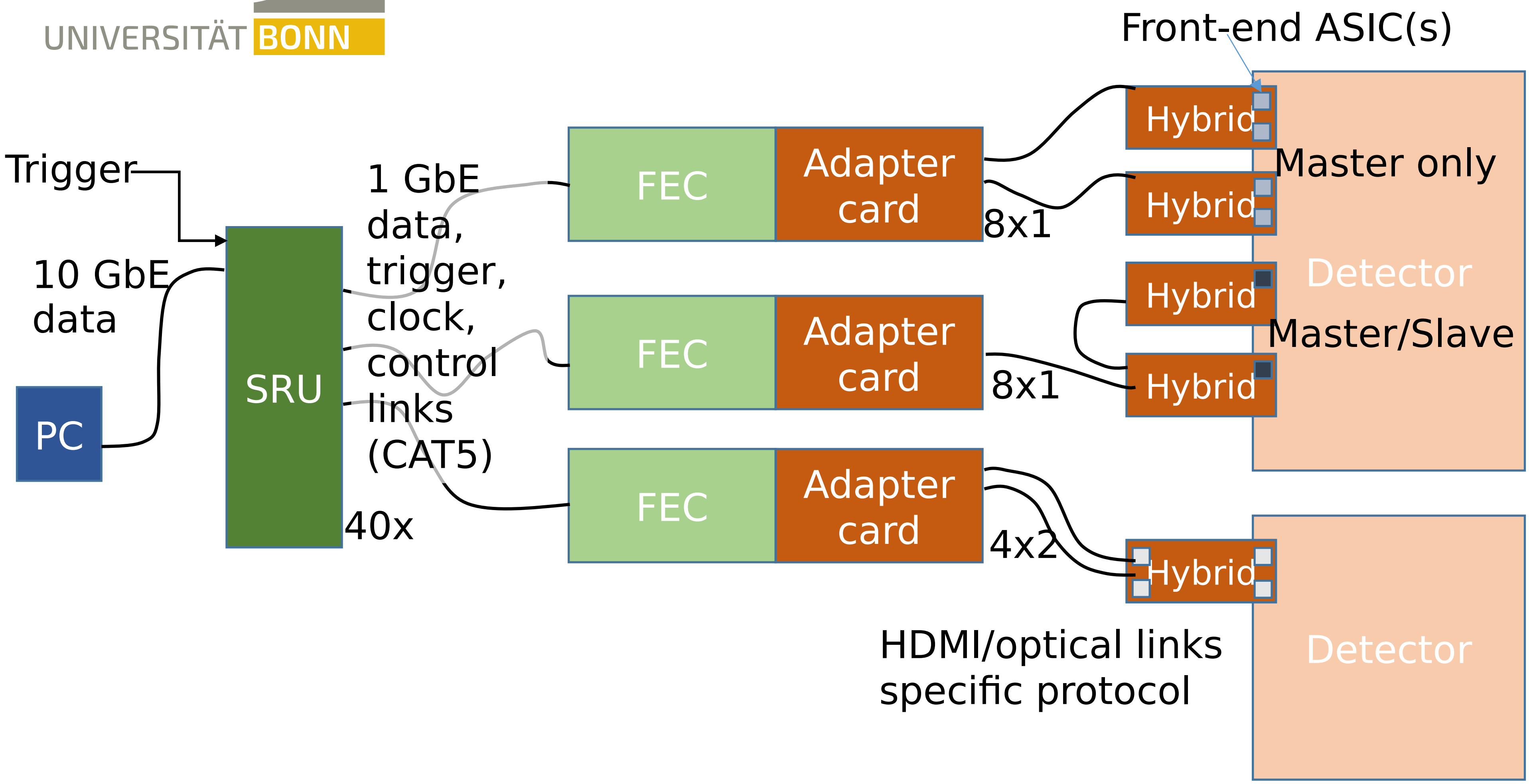
Front-end ASIC(s)
Adapter card
Hybrid
Hybrid
Master only
8x1
Detector
Adapter card
Hybrid
Master/Slave
Hybrid
8x1
Adapter card
4x2
Hybrid
Detector
HDMI/optical links
specific protocol

# WHAT IS SRS

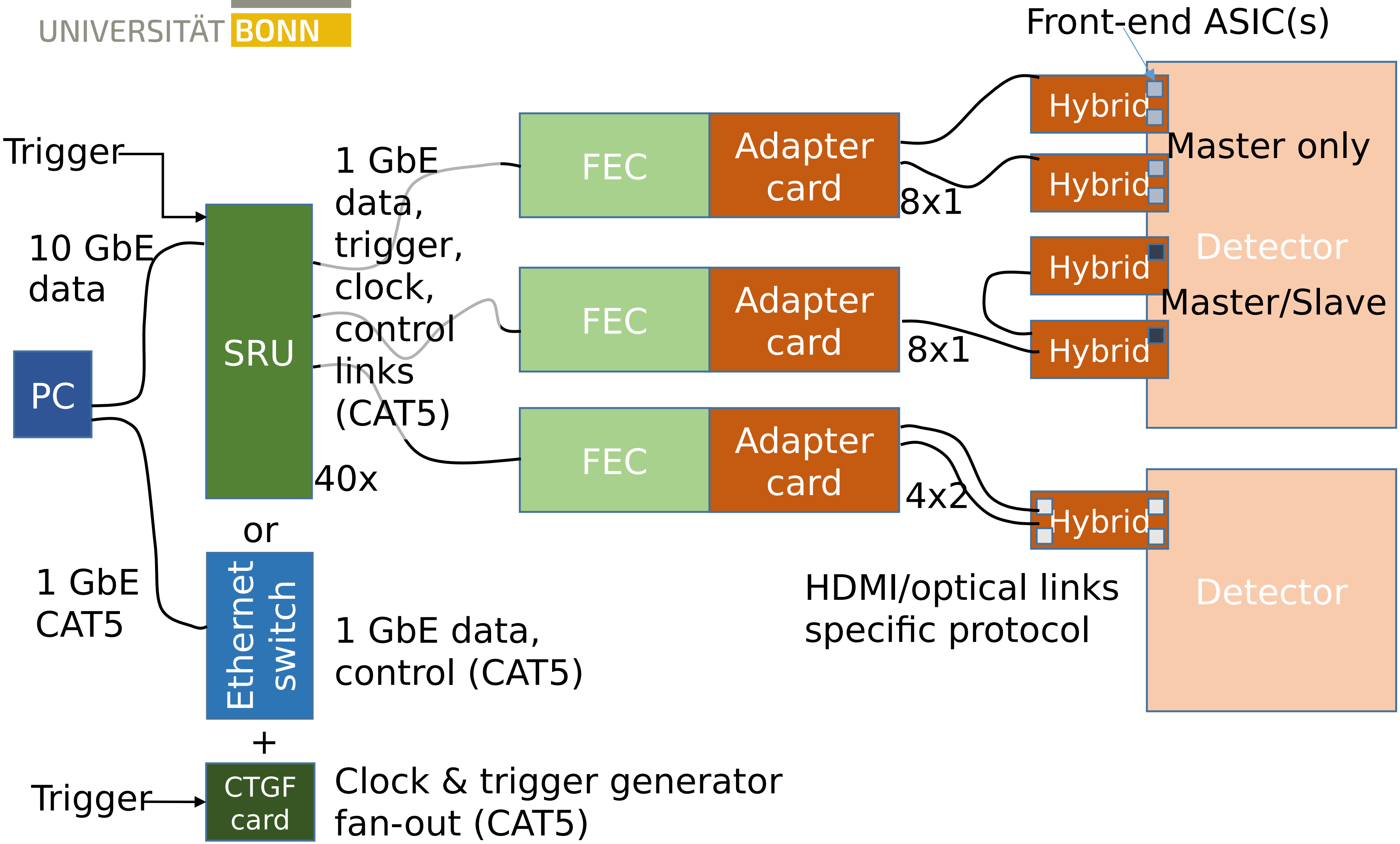


Front-end ASIC(s)
FEC
Adapter card
8x1
Hybrid
Hybrid
Master only
Detector
FEC
Adapter card
8x1
Hybrid
Hybrid
Master/Slave
FEC
Adapter card
4x2
Hybrid
Detector
HDMI/optical links specific protocol

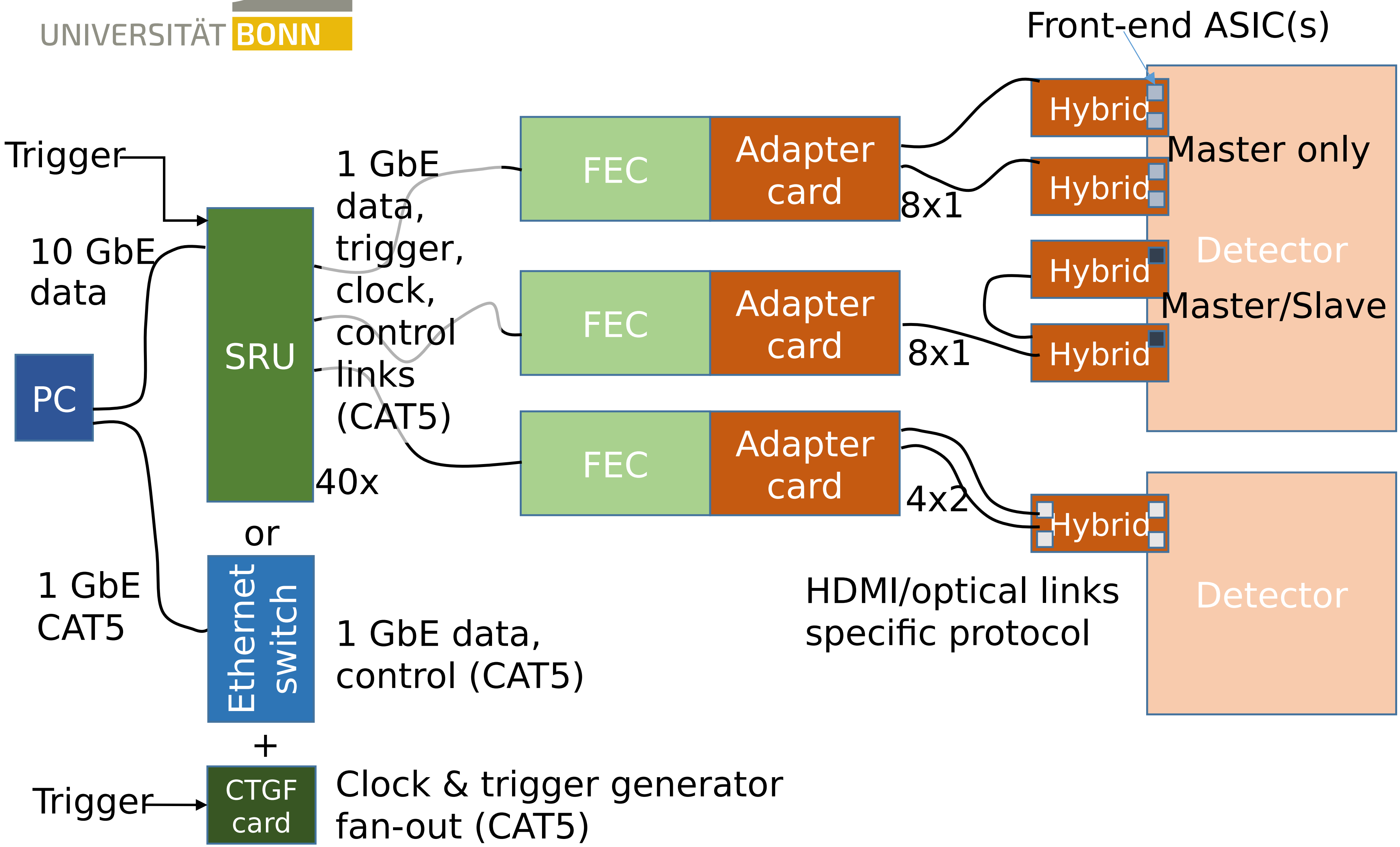
# WHAT IS SRS


Front-end ASIC(s)
Trigger
10 GbE data
PC
SRU
1 GbE data, trigger, clock, control links (CAT5)
40x
FEC
Adapter card
FEC
Adapter card
FEC
Adapter card
8x1
8x1
4x2
Hybrid
Hybrid
Hybrid
Hybrid
Hybrid
Master only
Detector
Master/Slave
Detector
HDMI/optical links specific protocol

# WHAT IS SRS


Front-end ASIC(s)
Trigger
10 GbE
data
PC
SRU
1 GbE
data,
trigger,
clock,
control
links
(CAT5)
40x
FEC
Adapter
card
FEC
Adapter
card
FEC
Adapter
card
8x1
8x1
4x2
Hybrid
Hybrid
Hybrid
Hybrid
Hybrid
Master only
Detector
Master/Slave
Detector
or
1 GbE
CAT5
Ethernet
switch
1 GbE data,
control (CAT5)
HDMI/optical links
specific protocol
+
Trigger
CTGF
card
Clock & trigger generator
fan-out (CAT5)

# WHAT IS SRS

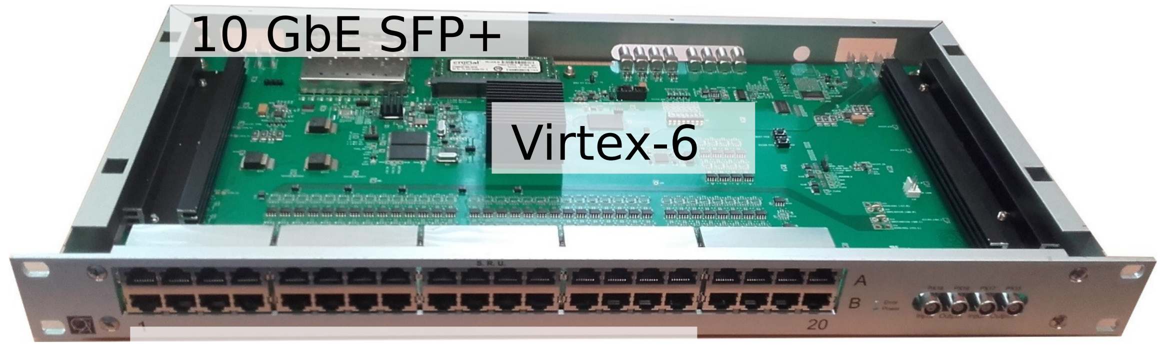



Example AVP25 (strip readout) up to:

82k ch/SRU 2048 ch/FEC 128 ch/hybrid + (master/slave)

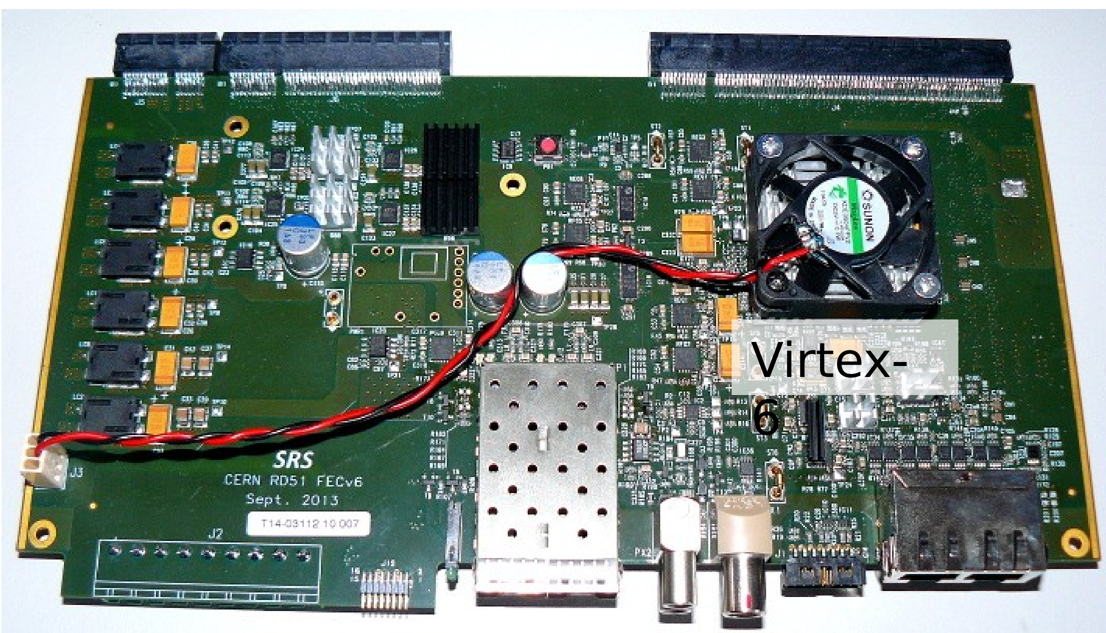
# WHAT IS SRS

SRU



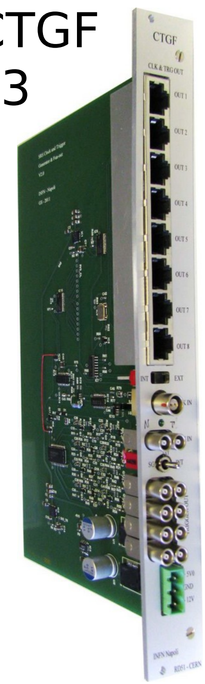

40x DDTC from FECs

FECv6 (2013)




1 GbE or DDTC to SRU

CTGF v3



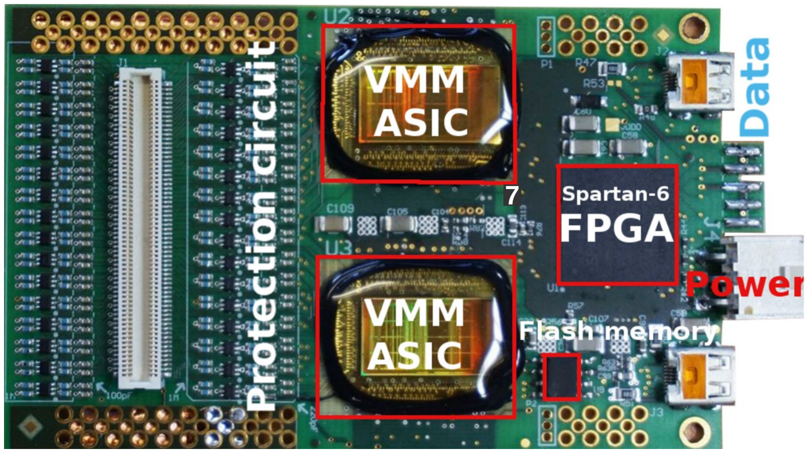
FECv3 (2010)

# SRS AND FRONT-END ASICS

Different ASICs are implemented in SRS:
- APV25 (past backbone in MPGD R&D)
- Beetle
- VFAT
- Timepix
- SiPMs


Implementation of ASIC in SRS requires:
Hybrid, adapter card, FEC FPGA firmware


Recently:
- Timepix3
- VMM (new backbone in MPGD R&D)




Ongoing:

SAMPA

# SRS VMM - DETAILS

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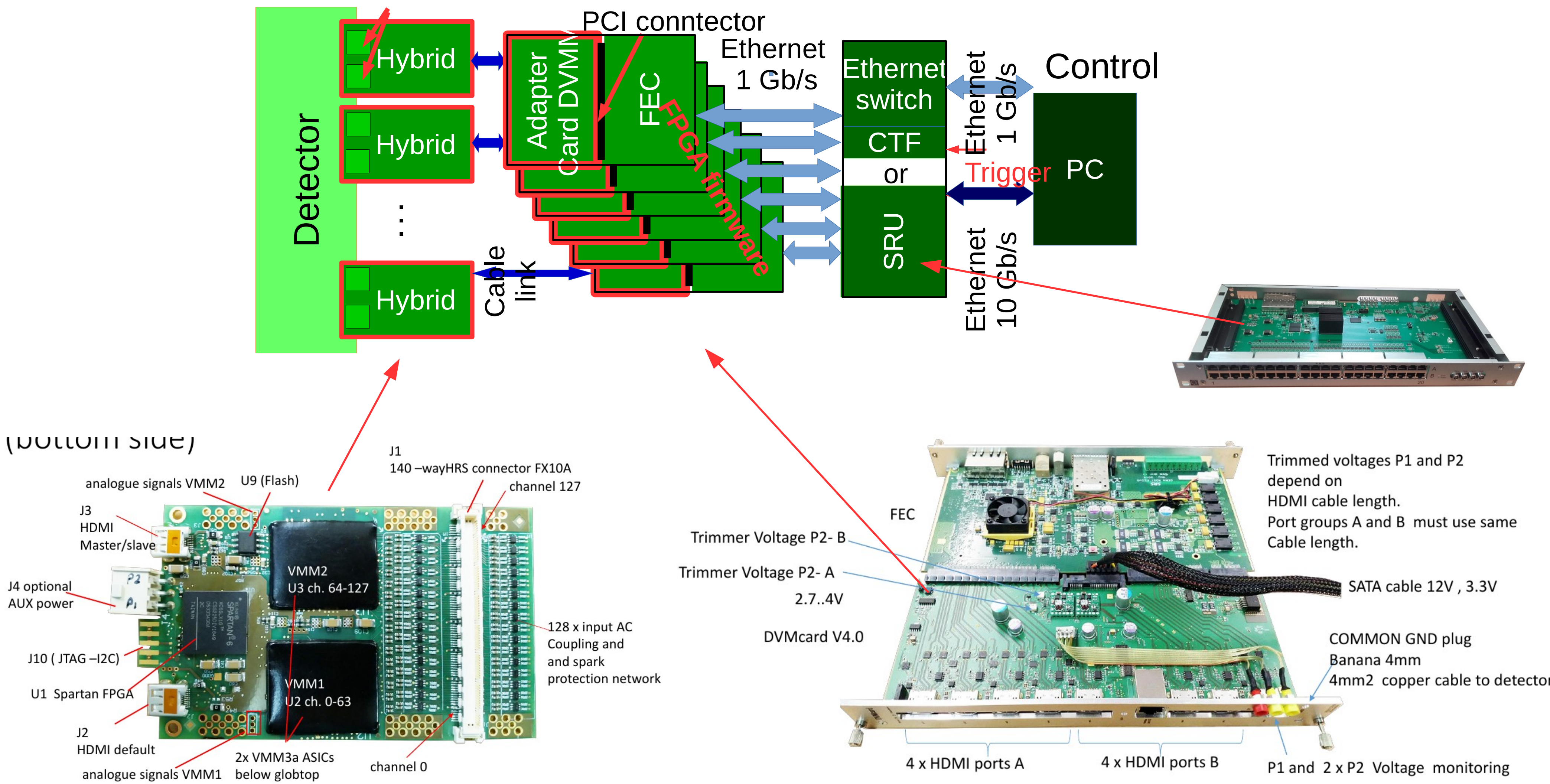
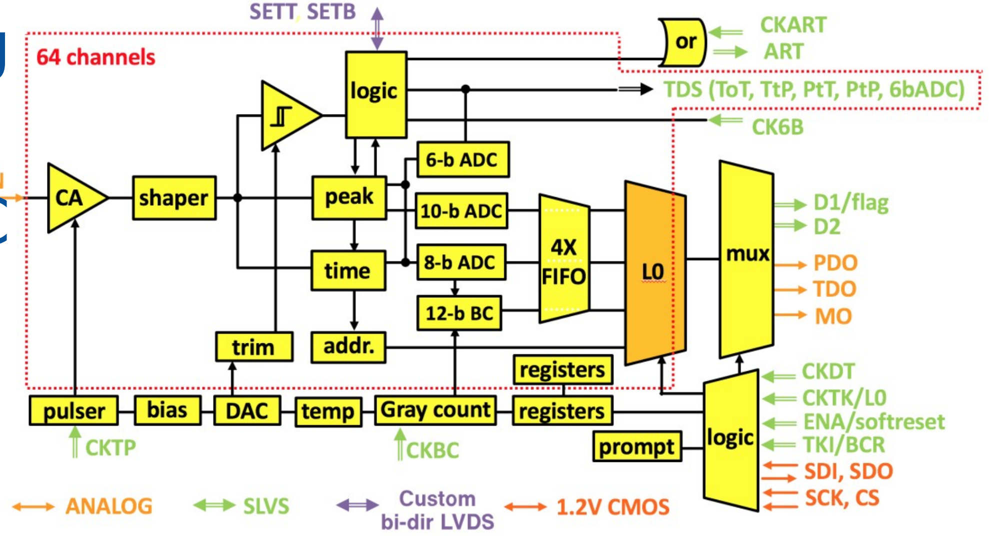
## System overview – readout chain



# VMM FRONT-END ASIC

Developed for the ATLAS NSW upgrade by BNL

- 130 nm CMOS technology
- 64 input channels, each w/ preamplifier, shaper, peak detector, several ADCs
- Pos. & neg. polarity sensitive
- Digital block w/ neighbouring logic, FIFO, multiplexer
- Adjustable gain 0.5-16 mV/fC
- Adjustable shaping time from 25 ns – 200 ns
- Input capacitance from few pF – 1 nF



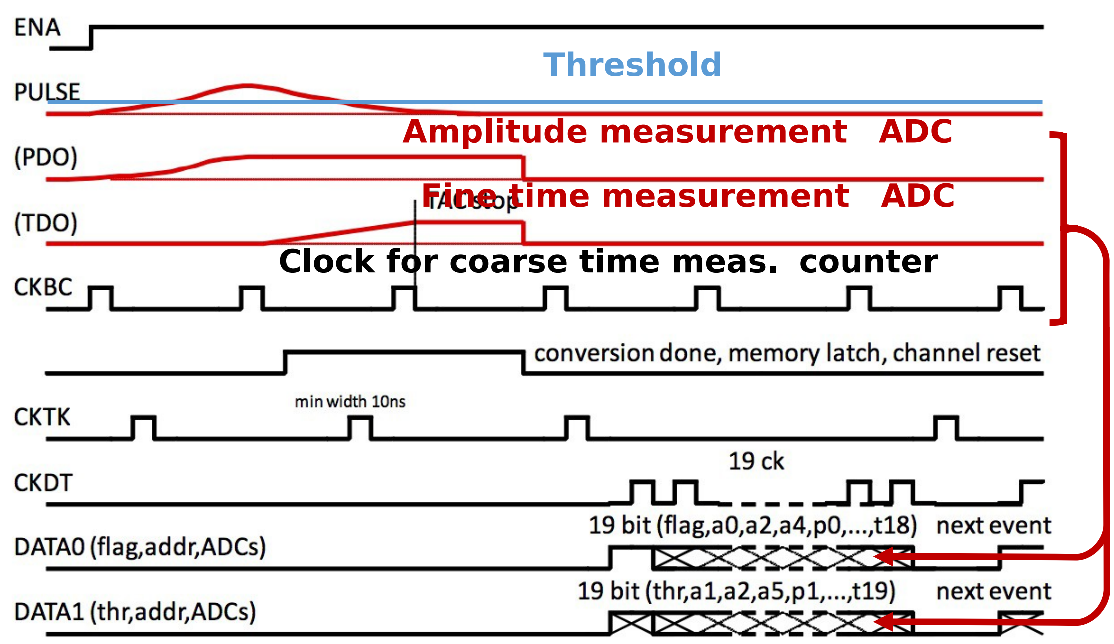
# VMM FRONT-END ASIC

Developed for the ATLAS NSW upgrade by BNL

- Internal test pulser with adjustable amplitude
- Global threshold & adjustment per channel
- Self-triggered, zero suppressed
- 38 bit per hit

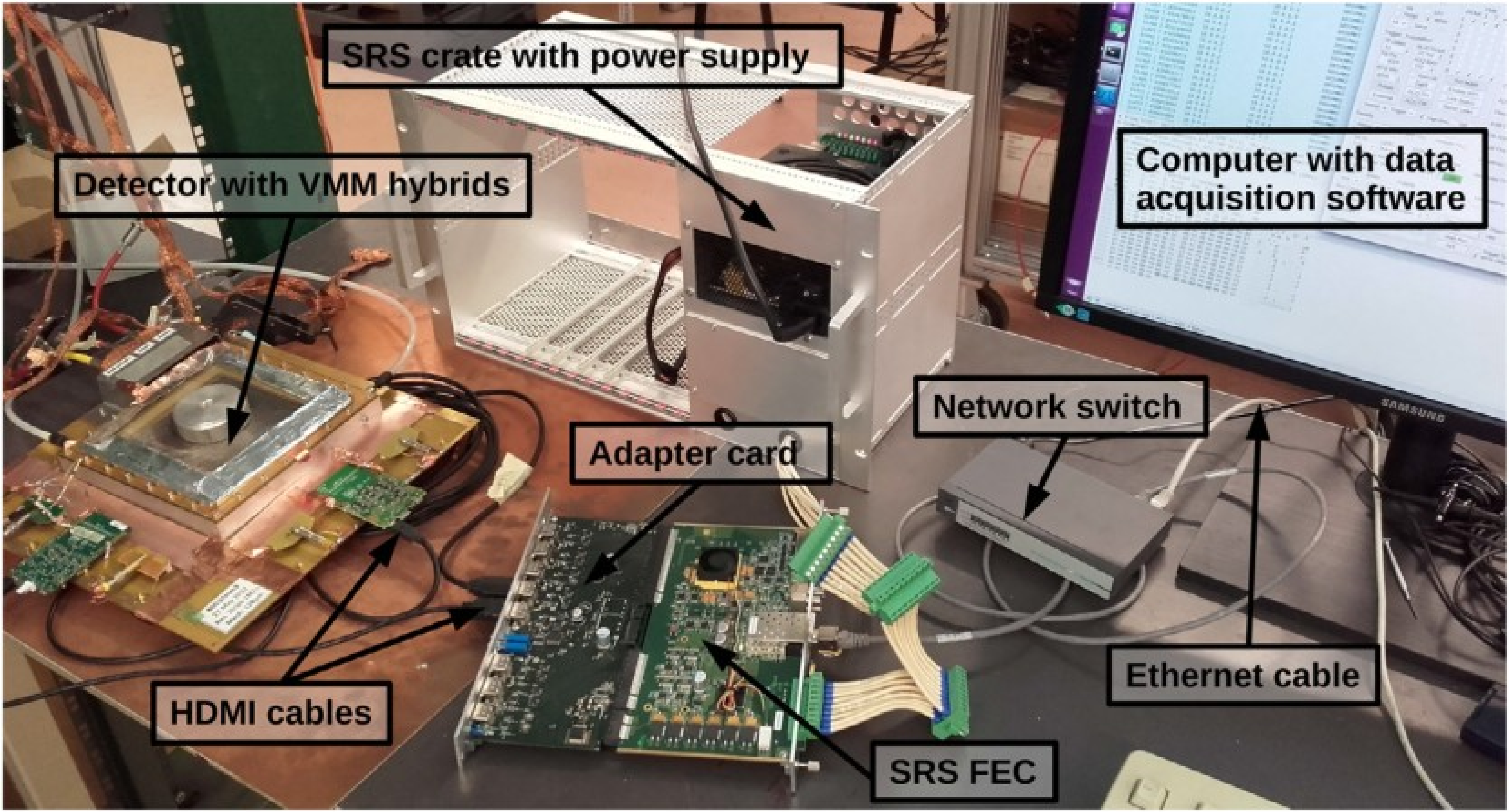
  (if input charge goes over threshold)

  1. Event flag (1 bit)
  2. Over threshold flag (1 bi
  3. Channel number (6 bit)
  4. Signal amplitude (10 bit
  5. Arrival time (20 bit)



# SRS VMM – DETAILS

## System overview – readout chain



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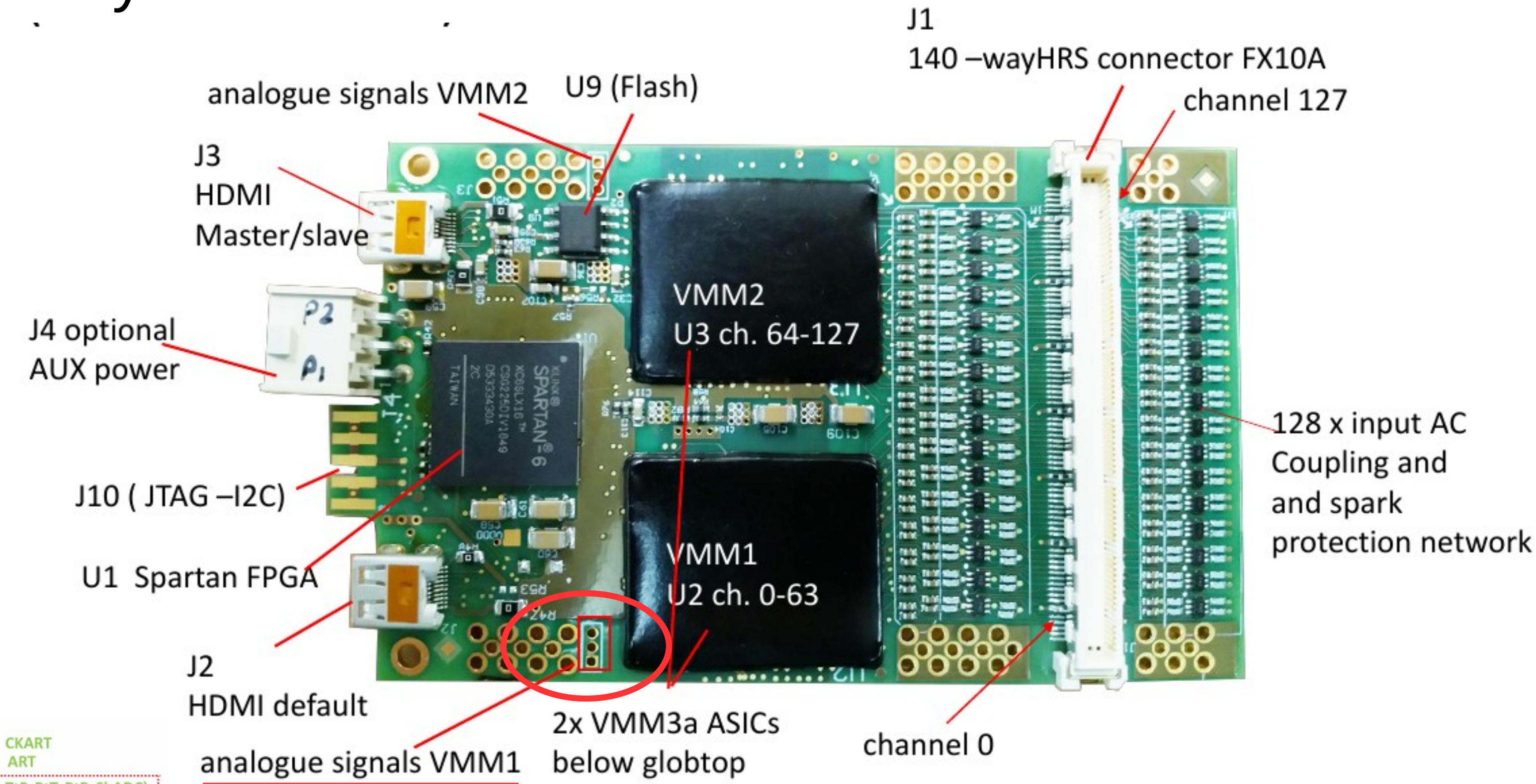
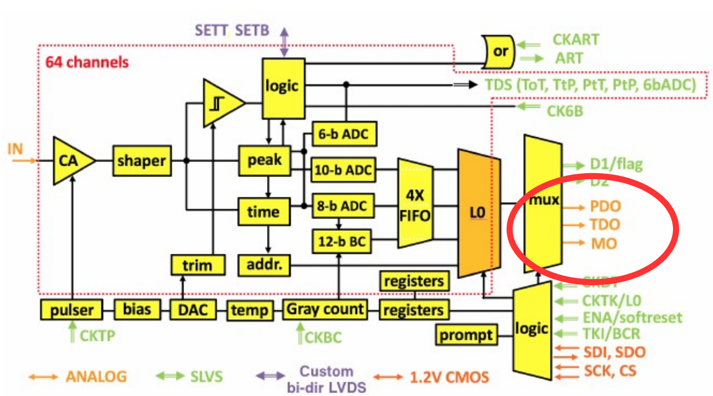
# SRS VMM – DETAILS

## System overview – Hybrid = VMM front-end board



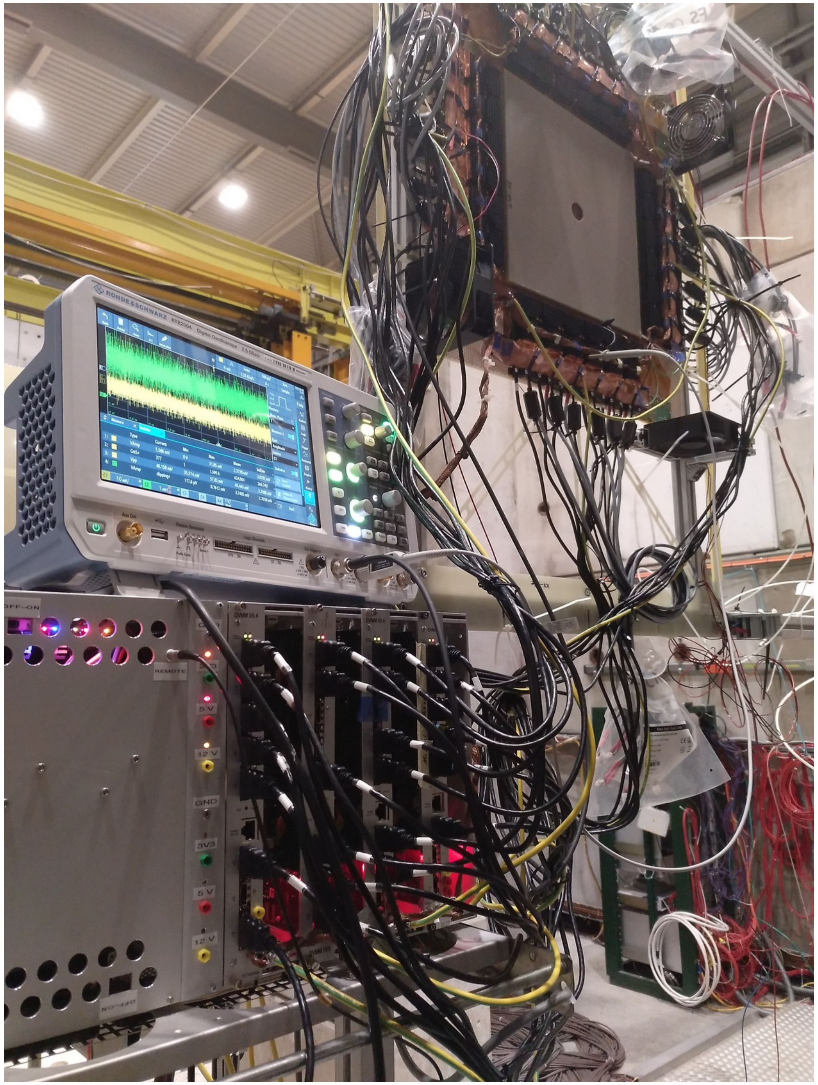



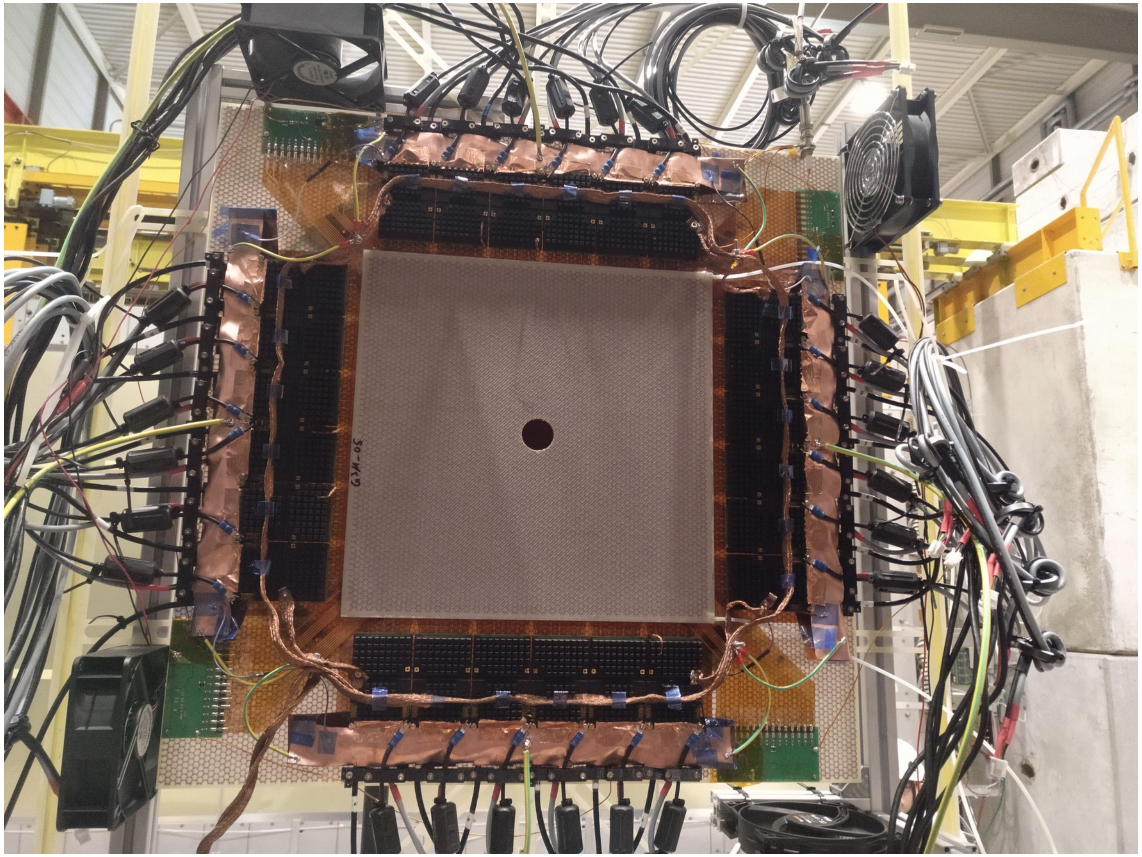

Programmable MO (Monitoring, analogue level) output:

- Global temperature sensor
- Bandgap voltage
- Pulser DAC
- Global threshold DAC
- Channel: individual threshold,baseline = shaper output

# SRS VMM – IN ACTION

## 30x30 cm² GEM detector test at the AMBER experiment





- 24 VMM hybrids, 4 SRS FECs, 1 10Gb/s switch
- 2 MHz muon beam on 3GEM detector with strip readout
- ~200 Mb/s of data when beam is on
- Found working point for detector for physics run

# OUTLOOK

Many subjects to work on in DRD1 electronics

- Readout structures
- ASIC development and testing
- Integration of ASICs in readout system
- FPGA programming
- Further development of the SRS
- New technologies (ML, GridPix, x-y-z readout, ...)
- Many other projects to facilitate detector development

Questions?