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Advancing in 65nm CMOS for lepton colliders: From single pixel structures to integrated matrices

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Monolithic active pixel sensors (MAPS) are attractive candidates for the next generation of vertex and tracking detectors for future lepton colliders. Especially an only recently accessible 65 nm CMOS imaging technology, that allows for higher logic density at lower power consumption compared to currently used imaging processes, is of high interest. Intensive simulation and characterisation of prototypes have proven the feasibility of further investigating the chosen technology.
The contribution is going to highlight the advancements of the prototypes going from a few analog pixels to a fully integrated chip with a 64x16 pixel matrix, including different readout modes. Characterisation highlights of a 4 pixel analog test structure featuring a charge sensitive amplifier during test beam and laboratory studies, including efficiency, time resolution and charge calibration are going to be presented. The same analog pixel cell is also included in the H2M chip, which explores the capabilities of a digital on top design approach. The design and readout modes of H2M are introduced together with the DAQ system based on Caribou.
Detailed characterization results will be presented both from laboratory and test beam campaigns, including threshold equalisation and charge calibration. Efficiencies of above 99% are determined. It is concluded that the technology is feasible to tackle many of the challenges of lepton collider experiments.

Primary experiment

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