Upgrade of the Belle II Vertex Detector with Depleted Monolithic CMOS Active Pixel Sensors

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on behalf of the Belle II VTX collaboration

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Outline

1. The Belle II Experiment
2. The current Vertex Detector (VXD)
3. Proposal for vertex detector upgrade: VTX
4. The TJ-Monopix2 chip
5. The OBELIX sensor : **O**ptimized **Bel**le II p**IX**el sensor
6. Conclusions

VTX collaboration

CPPM, Marseille
HEPHY, Vienna
IFCA (CSIC-UC), Santander
IFIC (CSIC-UV), Valencia
IGFAE, Santiago de Compostela

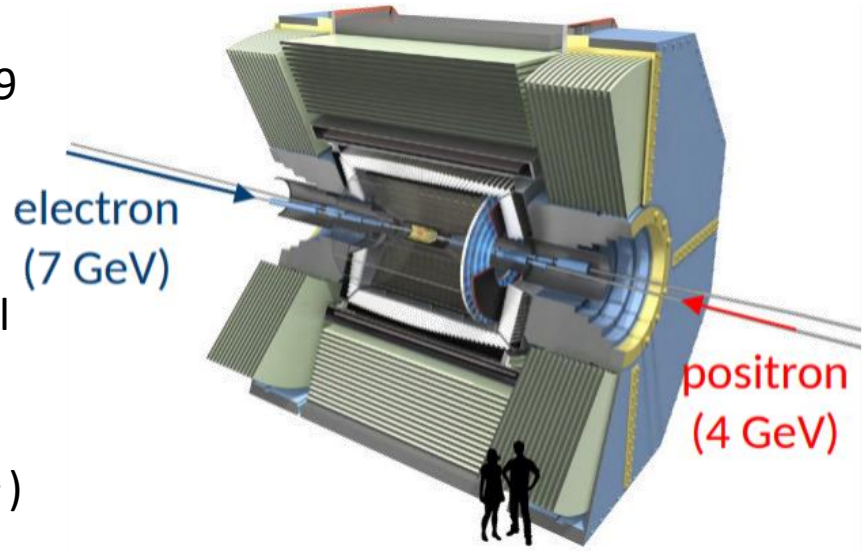
IJCLab, Orsay
INFN & University of Pavia
INFN & University of Pisa
IPHC, Strasbourg
IPMU, Kashiwa

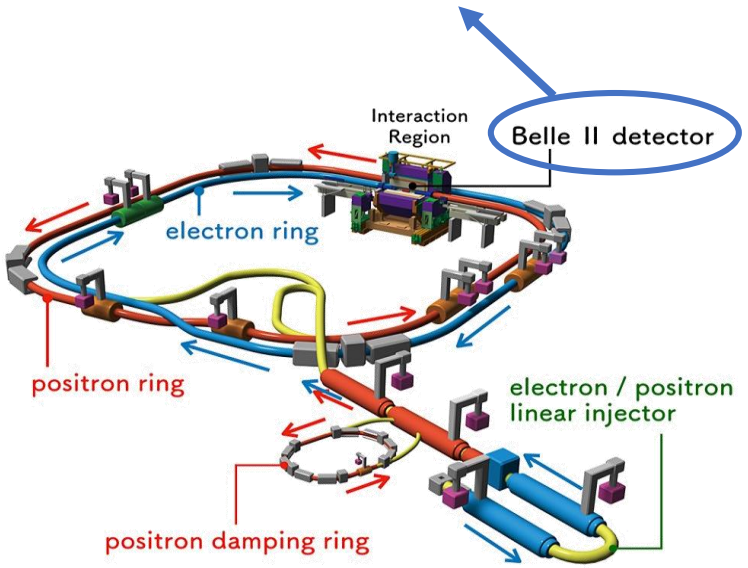
Jilin University
KEK, Tsukuba
KIT, Karlsruhe
Queen Mary University of London
RAL, Oxford

University of Bergamo
University of Bonn
University of Dortmund
University of Göttingen
University of Tokyo

The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba, Japan / started operation in 2019
- Asymmetric e^+- e^- collider at 4 / 7 GeV and $\sqrt{s}$ = 10.58 GeV
- Luminosity frontier experiment, exploring new physics beyond Standard Model
- **Targets for the upgrade:**
  - Instantaneous luminosity of **6×10^{35} cm^{-2}s^{-1}** (word record **0.51×10^{35} cm^{-2}s^{-1}**)
  - Integrated luminosity of **50 ab^{-1}** (currently **0.43 ab^{-1}**)
- **Consequences:**
  - Machine related beam background will increase with high luminosity
  - Efficiency, resolution and performance of data tracking could degrade with higher occupancy from background
  - Note that extrapolation to this target luminosity has large uncertainty and limited safety margins





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The Belle II Upgrade Motivations

- An upgrade of the Belle II detector (and of the Interaction Region) is required:
  - To cope with the higher luminosity provided by the SuperKEKB accelerator
  - To improve detector robustness against high backgrounds
  - To provide larger safety factors for running at higher luminosity
  - To increase longer term subdetector radiation resistance
  - To improve overall physics performance

- A **long shutdown** is foreseen around 2032 and provides the opportunity to install an upgraded detector

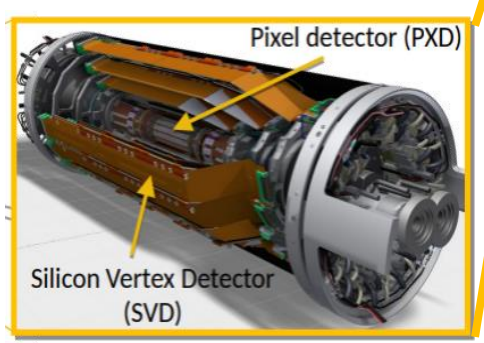
⇒ **A new vertex detector concept VTX is proposed**

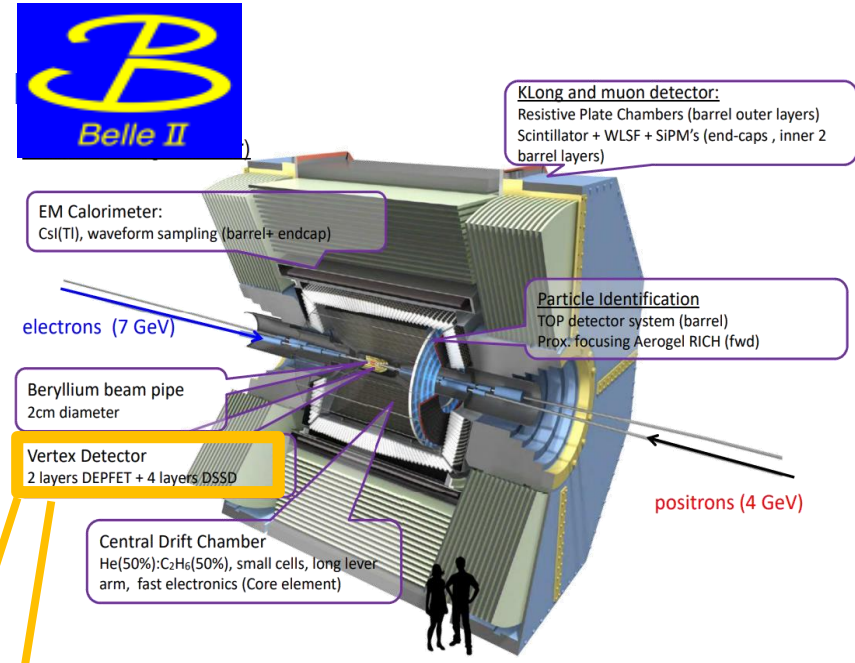
The Current Vertex Detector (VXD)

- Current VXD performance is good and operating with low background occupancy < 1 %

- Two different subdetectors compose the current VXD:
  - Pixel Detector (**PXD**) ⟶ *talk by B.Spruck (on Thursday)*
    - Two layers of DEPFET pixel sensor
    - Material budget: 0.25 % X_0 / layer
    - Pixel pitch: 50 to 75 µm
    - Integration time of 20 µs

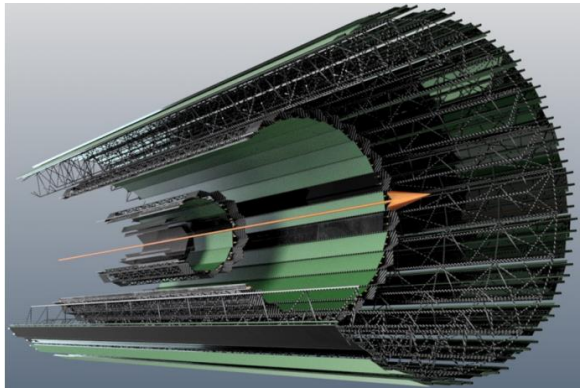
  - Silicon Vertex Detector (**SVD**) ⟶ *talk by K.Ravindran (on Thursday)*
    - Four layers of double sided silicon strip sensor
    - Material budget: 0.75 % X_0 / layer
    - Up to 12 cm long strips
    - Time resolution of 3 ns

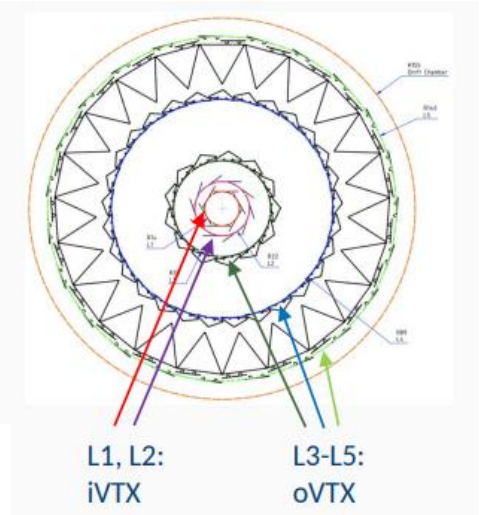




The VTX Upgrade proposal

- A new fully pixelated CMOS detector to replace the VXD ⇒ VTX
- Improved tracking resolution and space-time granularity
- Reduced material budget ≈ 2% X_0 instead of 3.8% X_0 (sum of all layers)
- 5-6 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (**DMAPS**) process
- L1 and L2 (iVTX)
  - All silicon ladders
  - Several cooling options under evaluation, based on power consumption and chip temperature limits
- L3 to L5 (oVTX)
  - Carbon fiber support frame
  - Cold plate with liquid cooling



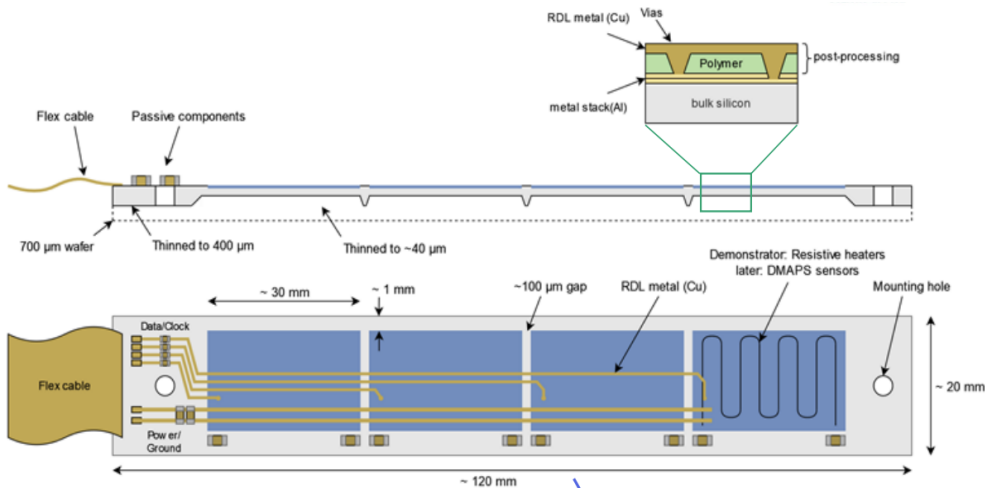


	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	17	40	31	
# Sensors	4	4	7	16	2 x 24	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	% X_0

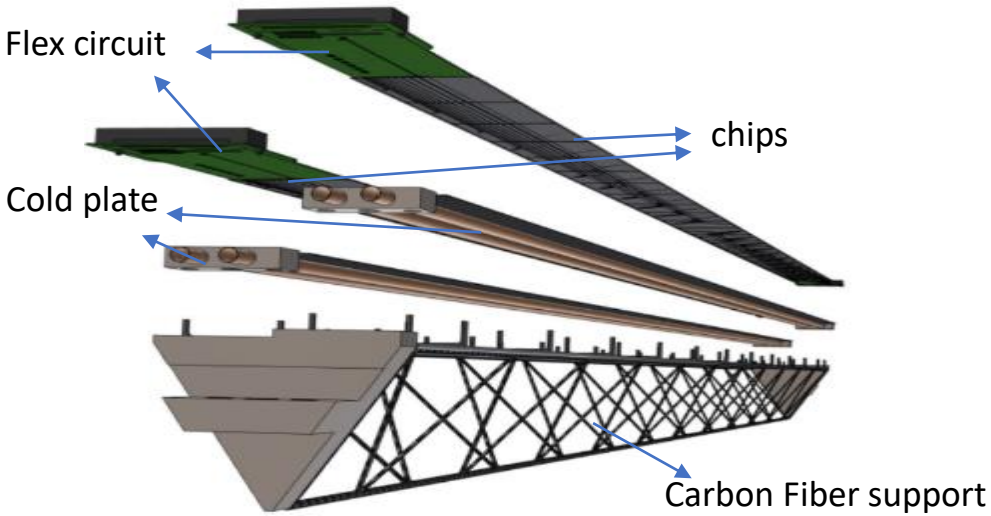
Baseline for VTX layers

The VTX detector mechanics

- iVTX Inner Layers Concept:
  - 4 contiguous sensors diced as a block from the wafer
  - Flex print cables
  - Redistribution layer for interconnection
  - Heterogeneous thinning for thinness and stiffness



Schematic view of the iVTX ladder design

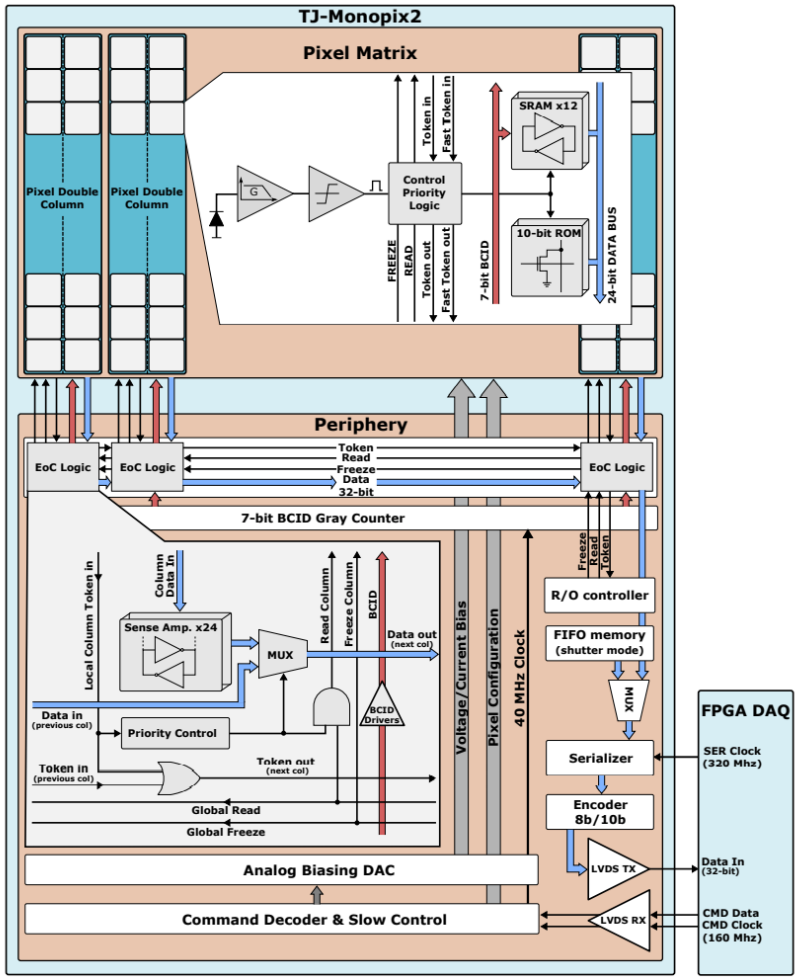


Exploded view of the oVTX

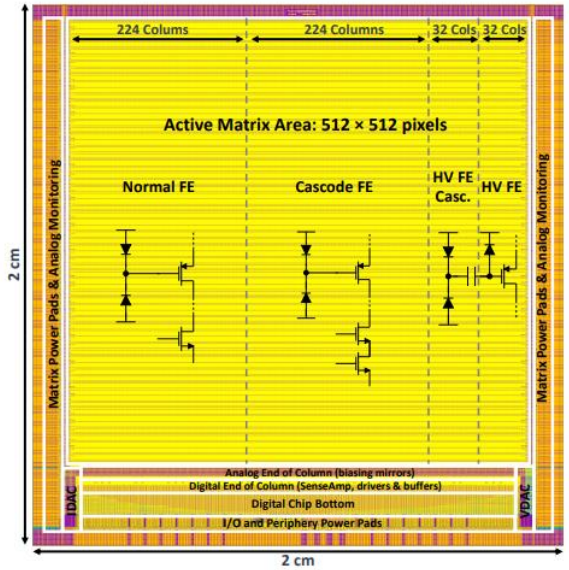
- oVTX Outer Layers Concept:
  - Ladder structure design inspired by ALICE ITS2, composed of:
    - Carbon Fiber support structure
    - Cold-plate with pipes for liquid coolant circulation
    - Chip and Flex circuit for power and signal glued on top

- A same monolithic CMOS pixel sensor chip for all layers : **Optimized Belle II pIXel sensor (OBELIX)**

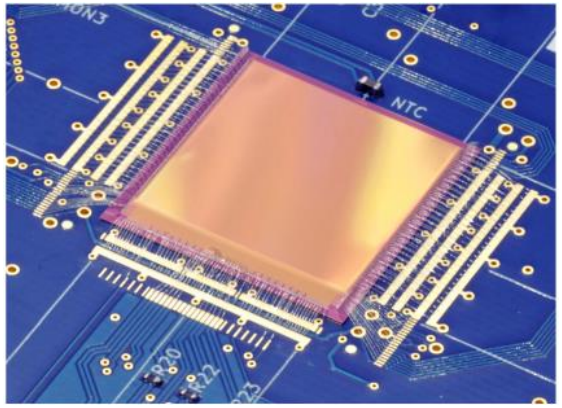
The TJ-Monopix2 (TJMP2) as prototype



Chip architecture of TJMP2



Layout of TJMP2 sensor: divided in 4 regions with different FE



TJM2 sensor bonded on a test board

- Developed for ATLAS experiment
  - FE derived from ALPIDE
  - 4 FE flavors with differences in the amplifier and detector input coupling (AC or DC)
  - Column-drain R/O architecture
- DMAPS **Tower Semiconductor 180 nm CMOS**
- 2×2 cm² chip: 512×512 pixels
- Pixel pitch: 33.04×33.04 µm²
- Expected from design (simulations):
  - ~ 100 e− min threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - Power: ~ 1 µW/pixel

Base-line option for OBELIX design

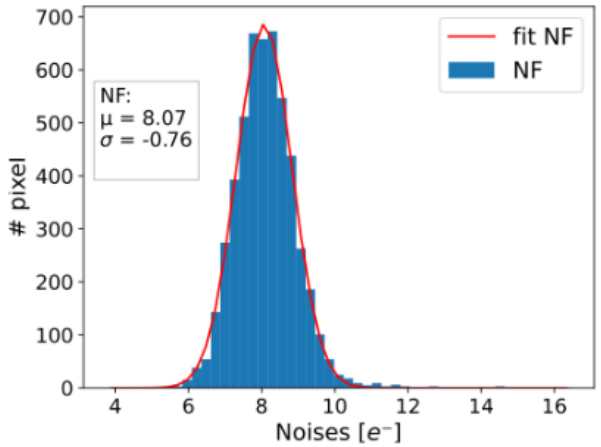
The TJMP2 Testing

- Characterisation of TJMP2 (all FE flavors) to validate key performance is crucial for OBELIX design

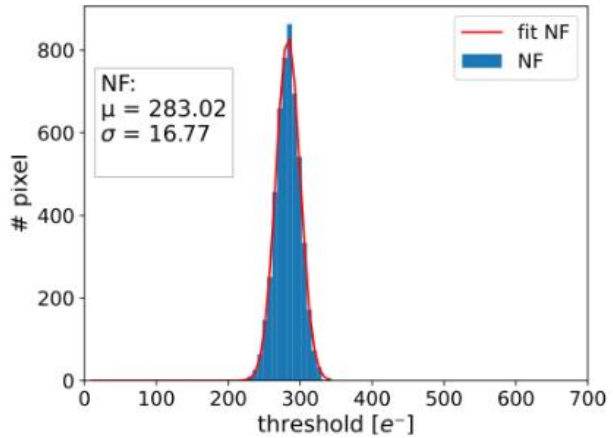
- **Characterisation on bench**:
  - Threshold scans (lowest value, dispersion)
  - Noise testing
  - ToT (Time Over Threshold) calibration

- Control and data acquisition system based on the BDAQ53 setup

TJMP2 setup DAQ inherited from RD53 collaboration



Noise distribution



Threshold distribution

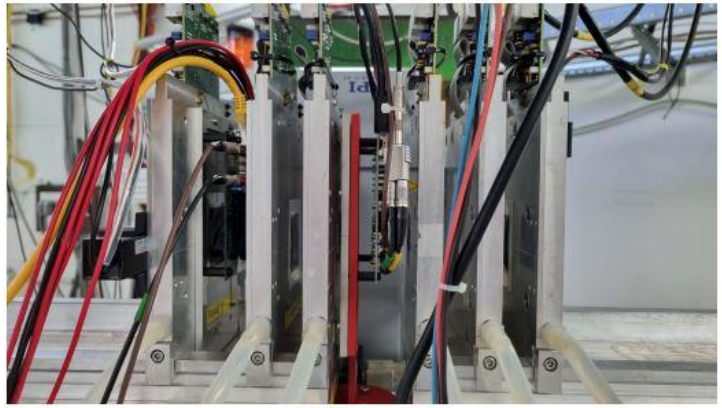
- Typical settings for operational threshold:
  - Thresholds between 200 to 300 e−
  - Average noise varies from 7 to 8 e−

- Time Over Threshold (ToT) calibration, Fe55

- Comparison with measurement and simulations
  - Measurement from monitoring pixels of the analog output signal after the FE amplifier

The TJMP2 Testing

- **Characterisation @DESY**:
  - Efficiency/Resolution measurements
  - Radiation hardness (NIEL and TID irradiation campaigns in progress)
- **Several test beam campaigns (3-5 GeV e-)**
  - **July 2022:** Non-irradiated chips
    - High threshold (500 e-)
    - Hit efficiency ~ 99.54% and position resolution ~ 9 µm
  - **July 2023:** Irradiated chips with 24MeV protons at $5x10^{14}$ n_{eq}/cm^2
    - Lower threshold ~ 250-300 e-
    - Good performance and high efficiency
  - **July 2024:** Irradiated chips at $5x10^{14}$ n_{eq}/cm^2, TID of 100 Mrad
    - TID 100Mrad: both DC and AC cascode efficiency 99.9%
    - NIEL $5x10^{14}$ n_{eq}/cm^2 : good efficiency but temperature influence
      - DC cascode efficiency > 99.5% but ~ 3% of masked pixels
      - AC cascode efficiency ~ 98.5%



Setup for testbeam @Desy

FE amplifier	Coupling	Efficiency [%]
Normal	DC	99.99
Cascode	DC	99.79
Normal	AC	98.11
Cascode	AC	99.13

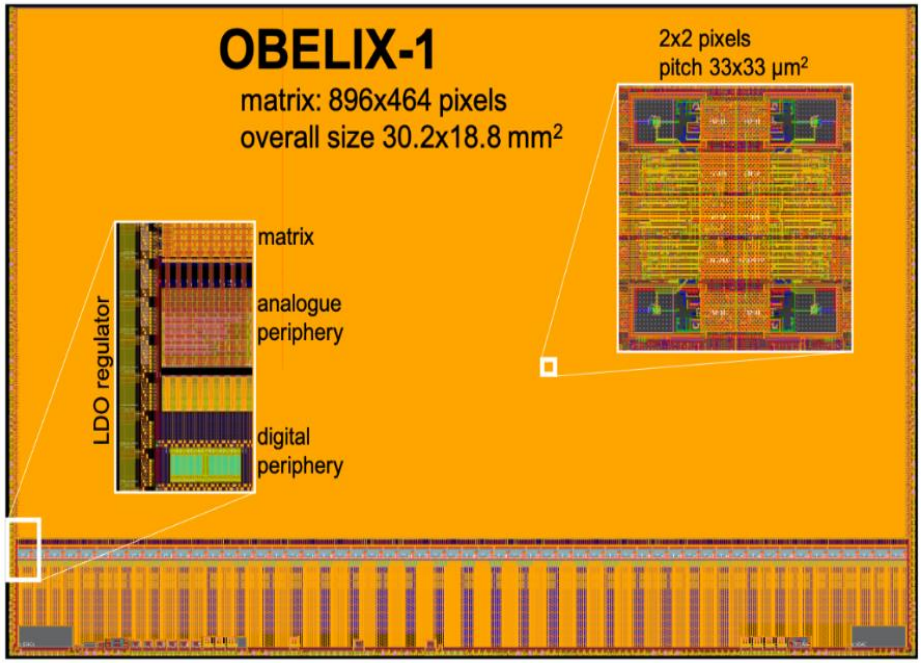
Results Test Beam July 2023

Another test beam planned for spring 2025

The OBELIX Sensor

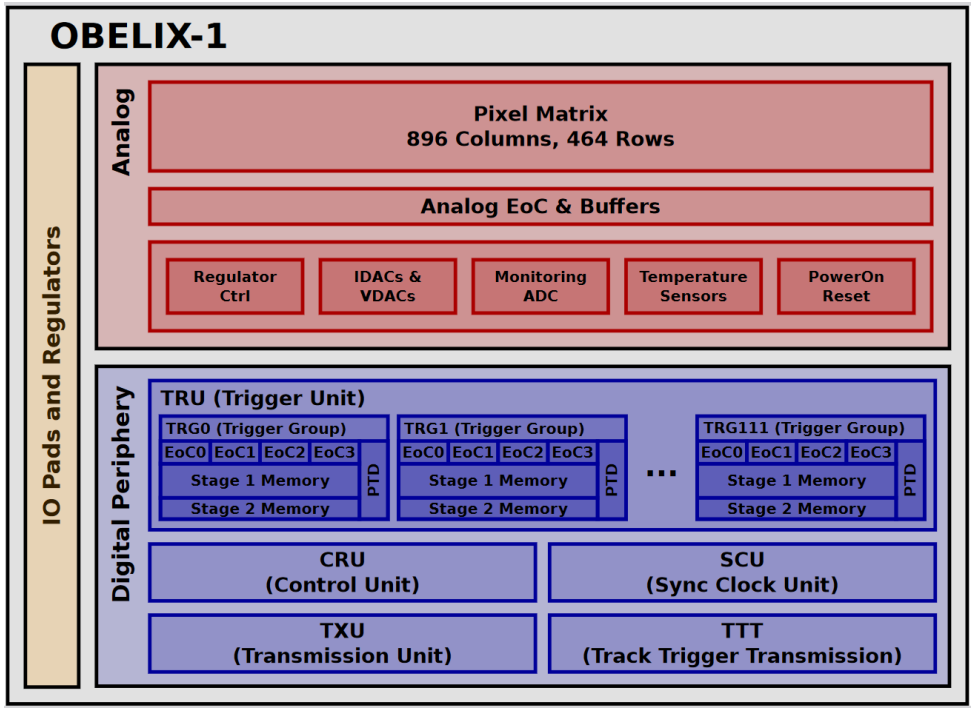
Sensor specifications:

- Tower Semiconductor 180 nm CMOS
- Hit rate up to 120MHz/cm²
- TID tolerance: 100 MRad
- NIEL tolerance: $5x10^{14}$ $n_{eq}/cm^2/year$
- Spatial resolution < 15µm
- Power < 200 mW/cm²
- Time precision < 100 ns
- Trigger at 30kHz average frequency with 10 µs latency



- 464 rows and 896 columns
- Overall sensor dimensions around 30.2x18.8 mm²
- Pixel pitch 33x33 µm²
- Main design based on the **TJMP2** chip

The OBELIX Block Diagram



Digital Periphery

- Main clk-in: 170MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 340 MHz average bandwidth
- RD53 control/readout protocol

Power pads

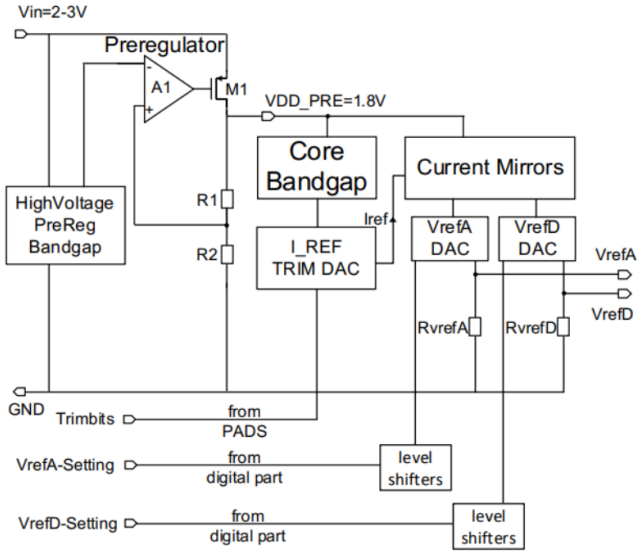
- Power regulators
- Simplified system integration

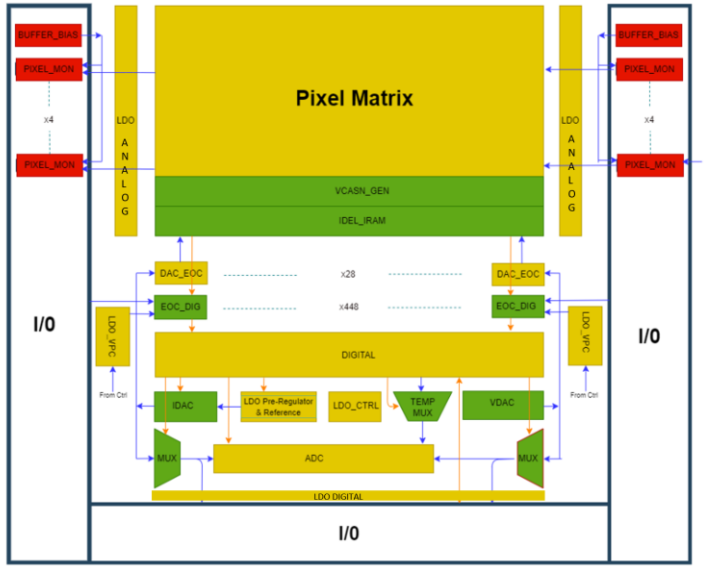
Analog

- Pixel matrix adapted from **TJMP2**
- Column drain architecture
- Monitoring ADC
- Temperature sensors

- **Based on current characterisation and simulation results, 2 FE flavors are chosen for OBELIX on equal area:**
  - **Cascode FE (DC)**
  - **HV Cascode FE (AC)**

The OBELIX Power management

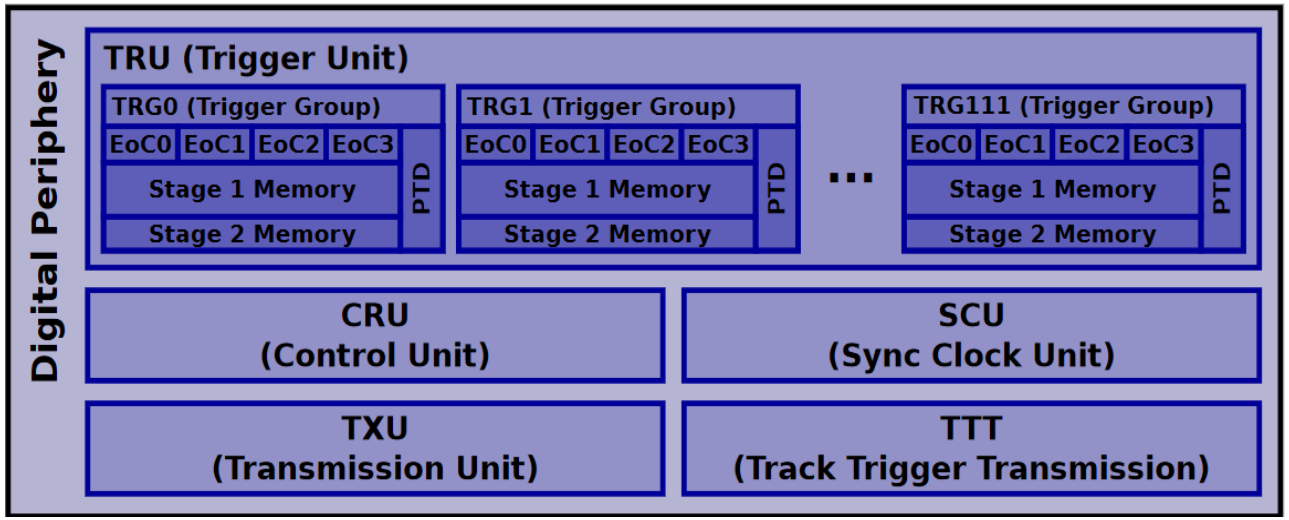


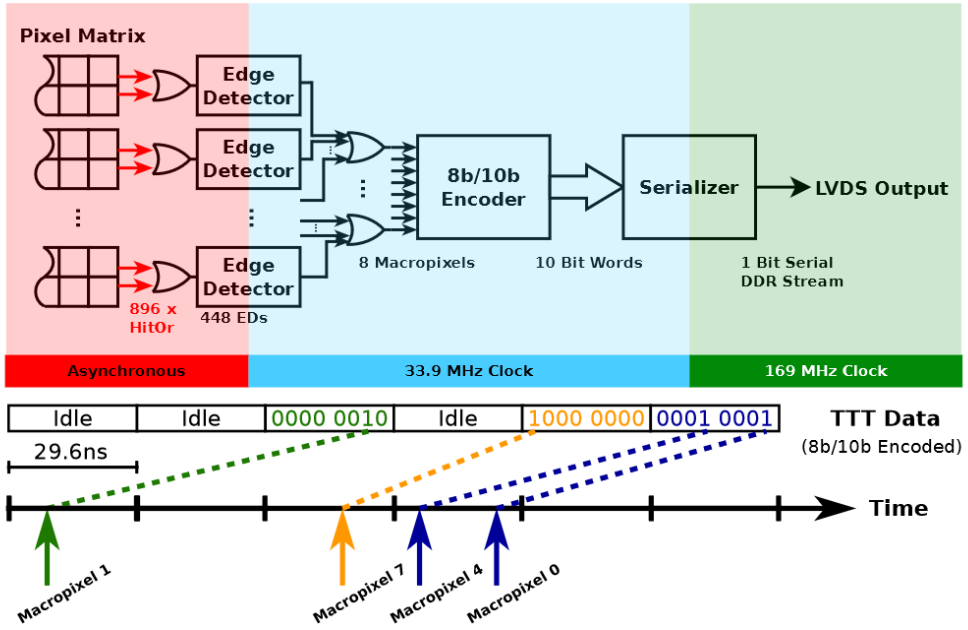


- Power distribution is a major concern as OBELIX is larger than TJMP2, leading to performance degradation
- Long linear ladders ⇒ voltage drop across ladder
- On chip regulators are developed to compensate the voltage drop and simplify the power distribution
  - Two analog **LDO (Low Dropout)** regulators to supply the matrix from both sides
  - A digital LDO in the bottom of the chip to supply the digital blocs
  - A preregulator to supply LDO references generator
  - A VPC (Voltage pre-charge) LDO to reset and recharge bit-lines between each read cycle
- The LDO generates the output voltage of 1.8 V (+ 10%, -20%) necessary for the technology to power the chip
- Wide input supply voltage range of 2-3 V

The Digital periphery of OBELIX

- Module division: 5 main parts with new modules related to the Belle II trigger
  - **TRU - Trigger Unit:** Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output
    - PTD - Periphery Time to Digital : Precision timing feature → 5ns for hit rate < 10 MHz/cm^2 (enabled via configuration)
  - **CRU - Control Unit:** Implement RD53B interface, command decoder and global configuration
  - **SCU - Sync Clock Unit:** Synchronize circuit and clk divider , Rx_data SIPO synchronization
  - **TXU - Transmission Unit:** Generate output data and sequential output, data framing, serializer
  - **TTT - The Track Trigger Transmission:** Provide coarse and rapid information to the Belle II trigger system





Conclusions

- The SuperKEKB collider is considering a major upgrade to reach a luminosity of **$6x10^{35}$ $cm^{-2}s^{-1}$** *[ref CDR]*
- Reaching the target peak luminosity requires an upgrade of the interaction region and the Vertex Detector
- A new DMAPS VTX is foreseen to improve the performance of the Belle II vertex detector
- The OBELIX sensor based on TJMP2 chip with TJ180 nm technology is under development with additional on-chip features:
  - Voltage regulators
  - ADC and temperature sensors
  - Trigger logic, 10 µs latency at 120 MHz/cm²
  - Precision timing module
  - Fast transmission for trigger contribution
- Lab testing and test beam campaigns on TJMP2 to validate key performance crucial for OBELIX design
- Development and verification of OBELIX are entering the final stages
- Aiming submission of first version of OBELIX sensor in spring 2025

Thanks for your attention

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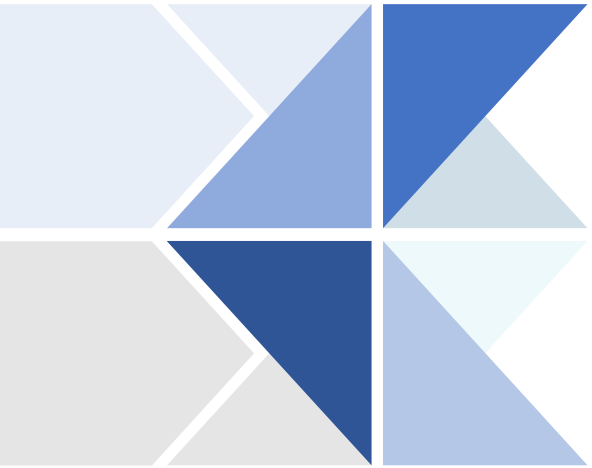
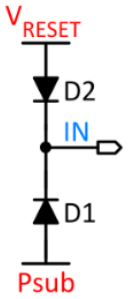


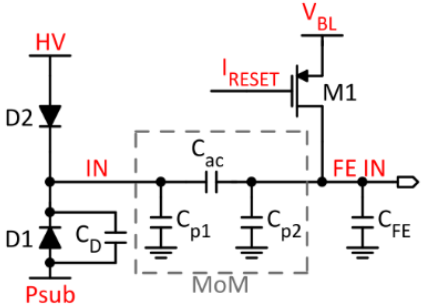
Backup slides

The analog FE design

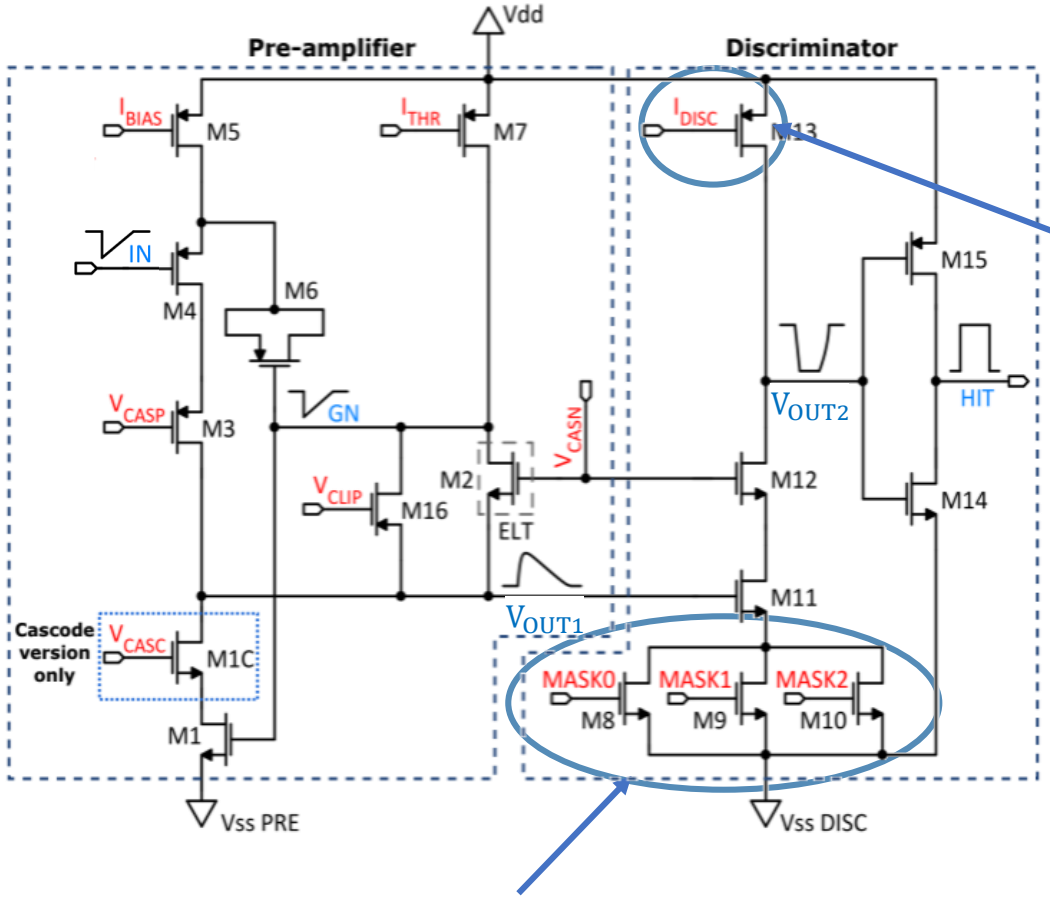
- Two flavors with a cascode pre-amplifier :
  - With an input **DC-coupling** using a forward biased diode **(Cascode FE)**
  - With an input **AC-coupling** allowing higher bias voltage above 30V (**HV Cascode FE)**



Input DC-coupling

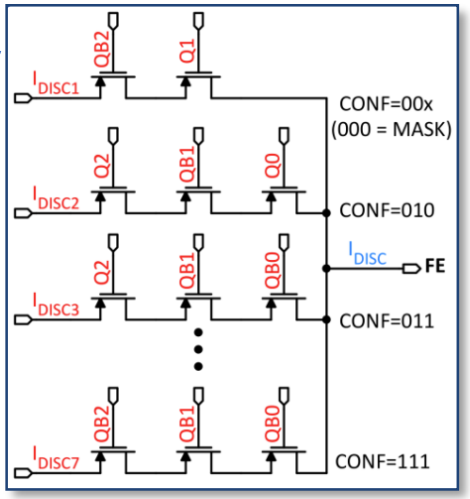


Input AC-coupling



Individual pixel masking

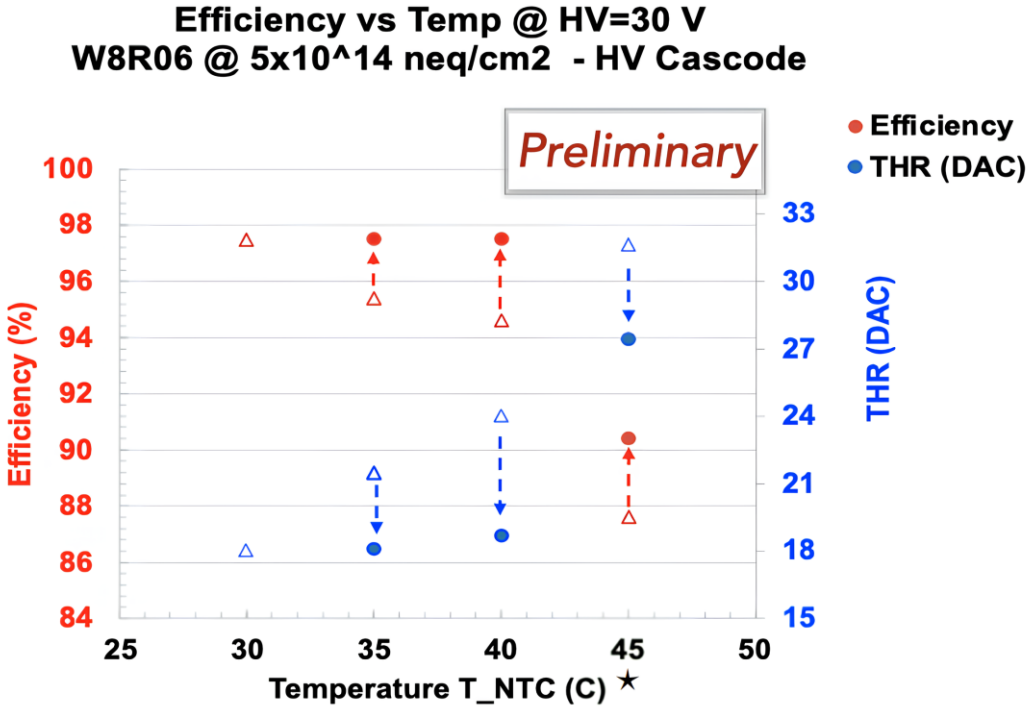
3-bit Threshold Tuning DAC



- A 3 bit threshold tuning is available at the pixel level to reduce the threshold dispersion

TJMP2 Test Beam

- **July 2024** : Irradiated chips at 5x10^{14} n_{eq}/cm^2, TID of 100 Mrad
  - Good efficiency but temperature influence
  - With chip temperature > 40C (T_{room}), both threshold and noise increase, with a drop in efficiency



Another TB planned for spring 2025 to explore lower temperature ranges and study the performance for irradiated sensors at different NIEL fluences