Design of the readout electronics for the engineering model of the HERD-TRD

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Abstract—In this work, we develop front-end electronics (FEE) as a standard readout unit for the engineering model of the HERD-TRD. The FEE uses 4 SAMPA ASICs to read 128 anode signals. To improve the detection accuracy, the FEE will realize an on-orbit adjustable dynamic range of 0-500 fC. The FEE design has progressed to the engineering model stage, and the FEE has carried out a series of irradiation-resistant designs. Comprehensive tests have been performed on the readout electronics. The test results indicate that the readout electronics have reached good performance.

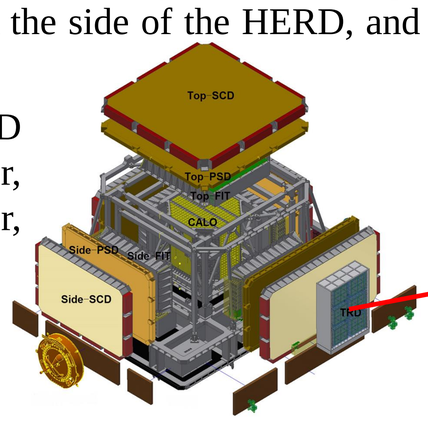
HERD and the prototype of TRD

The High Energy cosmic-Radiation Detection facility (HERD) is a part of the Chinese Cosmic Lighthouse Program in China's Space Station, which will be launched in 2027. TRD is mounted on the side of the HERD, and the 2×3 detection array composed of 6 detector units can be extended through the mechanical turntable.

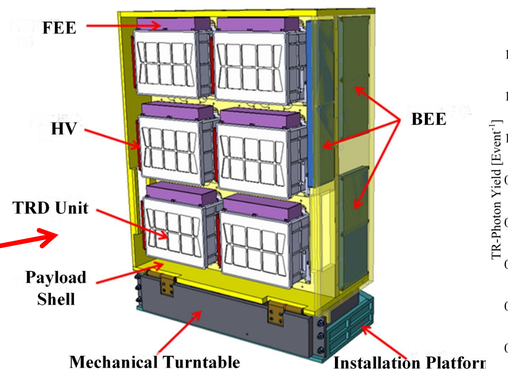
HERD consists of five detectors: 3D Imaging calorimeter (CALO), fiber tracker, plastic scintillator, silicon charge detector, and transition radiation detector (TRD).

Scientific goals:

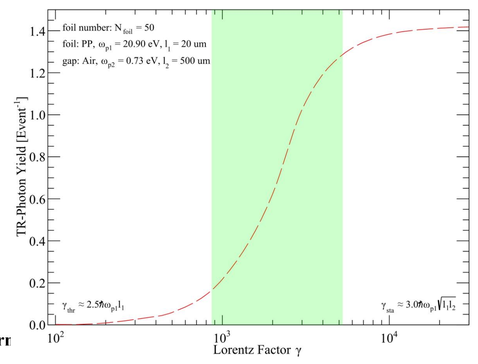
- Indirectly detect dark matter.
- Measure cosmic rays.
- Observe high-energy gamma rays



Architecture of HERD



Architecture of TRD detection system



Lorentz factor calibration curve

Calibration mode: The calibration of the TeV energy range of the CALO to improve the accuracy of cosmic ray detection.

GRB mode: The detection of high-energy gamma rays.

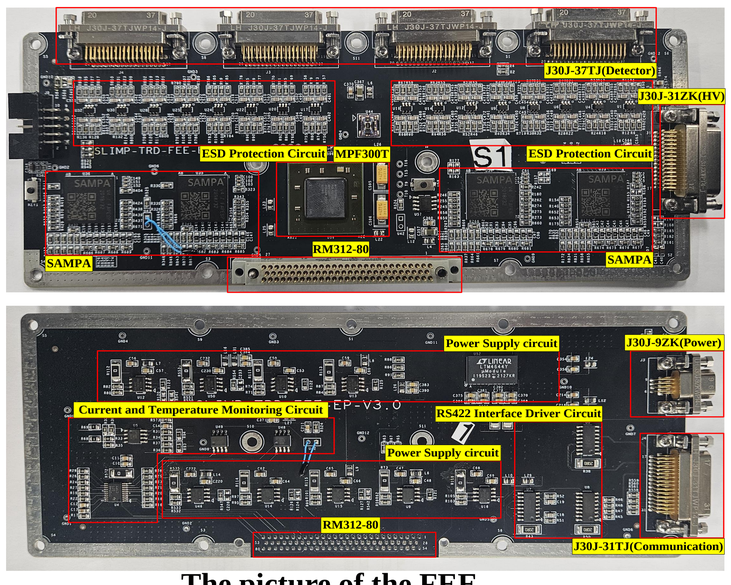
The sealed gas detector will first large-scale used in space exploration.

The energy of the transition radiation is proportional to the Lorentz factor (γ) of the incident-charged particle.

The design of the FEE

A. Hardware design of the FEE

Due to mechanical constraints, the FEE design is divided into two printed circuit boards. One is used for power supply and communication, and one is for reading detector signals and controlling the high-voltage unit. The two PCBs are connected using the RM312-80 interface. The FEE uses an irradiation-resistant FPGA (PolarFire MPF300T) design to improve the irradiation resistance characteristics of the system.

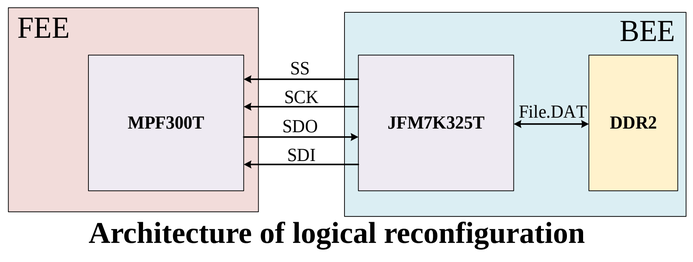


The picture of the FEE

In the design of the FEE, we have focused on the reliability of the TRD system.

Preventing Single-Event Upset in Orbit for FPGA: To prevent the Single Event Upset from affecting the FPGA's normal operation. It facilitates the maintenance and upgrading of the code, enabling in-orbit reconfiguration of the FPGA via the SPI bus.

- Preventing Single-Event Latch-Up in SAMPA Chips: FEE has three current monitoring points. By monitoring the power supply current of the SAMPA; when a latch-up occurs and the current abnormally increases, the power supply can be promptly shut off. The accuracy of current monitoring can reach 2.45 mA.



Architecture of logical reconfiguration

This type of programming requires that the external microprocessor run the Microchip SPI-DirectC solution.

The FEE uses four SAMPA ASICs for 128 detector signal readouts.

B. Firmware design of the FEE

Compared to previous FEE designs, this design focuses on the high-voltage control and monitoring module, including ramp-up and ramp-down high voltage and discharge protection.

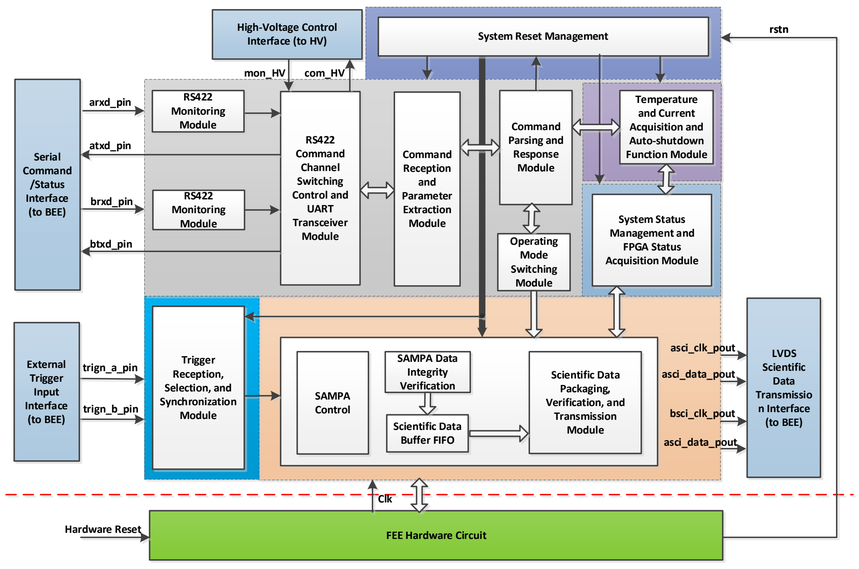
Main functions of HV control:

- Adjustment of high voltage levels:

The design sets half the normal operating voltage as the safe voltage value. When the voltage falls below this value, it increases at a rate of 100V/s until the safe voltage is reached, and thereafter, it increases at a rate of 20V/s. Similarly, the voltage decreases in steps following the same decremental rates. Additionally, these step sizes can be adjusted through commands.

Protection against minor and severe discharges:

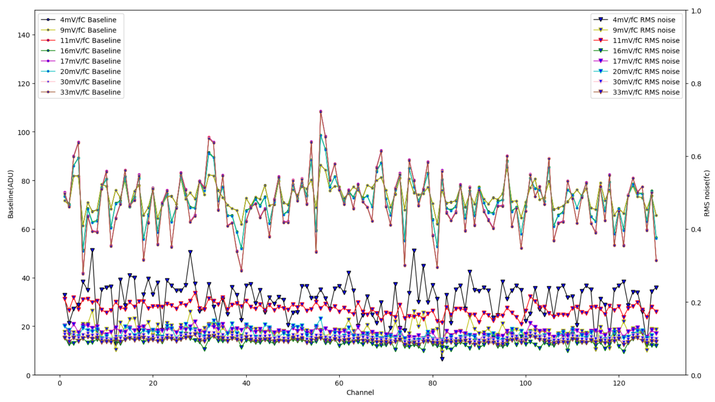
Monitor the current changes of the high-voltage module to identify minor and severe discharge phenomena. Immediately shut down the high-voltage module when severe discharge occurs to prevent damage to the detector and FEE. When minor discharge occurs, record the discharge time. If the continuous discharge exceeds the safe time limit, reduce the high voltage to a safe level.



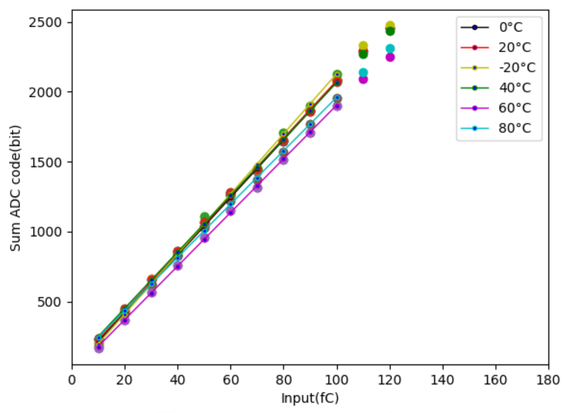
The architecture of FPGA firmware

Performance measurement

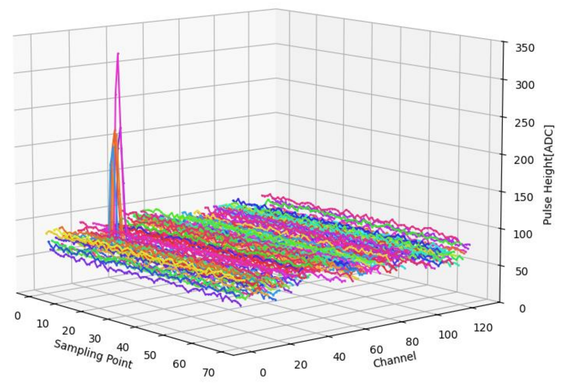
A series of tests were performed to evaluate the functionality and performance of the FEE. It includes the baseline and RMS noise under different gains, the changes of linearity under high and low temperature experiments, and the testing of radioactive sources. The in-orbit operating temperature of the FEE is 0 - 35°C. Within this temperature range, its linearity is highly stable, with a deviation of less than 1%.



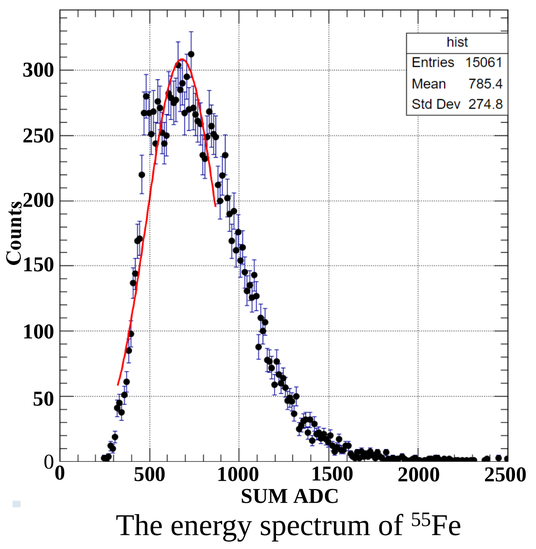
The baseline and RMS noise of 128 channels.



The result of linearity test.



The signal of ^{55}Fe



The energy spectrum of ^{55}Fe

Conclusion

A readout system has been successfully designed and produced for TRD in HERD. Test results indicate the FEE can operate stably under different gains and temperatures. Additionally, a radioactive source test was carried out to verify the performance of the combined operation of the detector and the FEE, and the result meets the expected design.

References

[1] J. Zhu et al., "Front-End Electronics Design for the Transition Radiation Detector Prototype in the HERD,"IEEE Trans. Nucl. Sci., 2024.

[2] A. Velure, "A Digital Signal Processor for Particle Detectors: Design, Verification and Testing," Germany: Springer Cham, 2021.