PSI Center for Photon Science

On-chip digitization to improve the frame rate of the JUNGFRAU charge-integrating X-ray pixel detector

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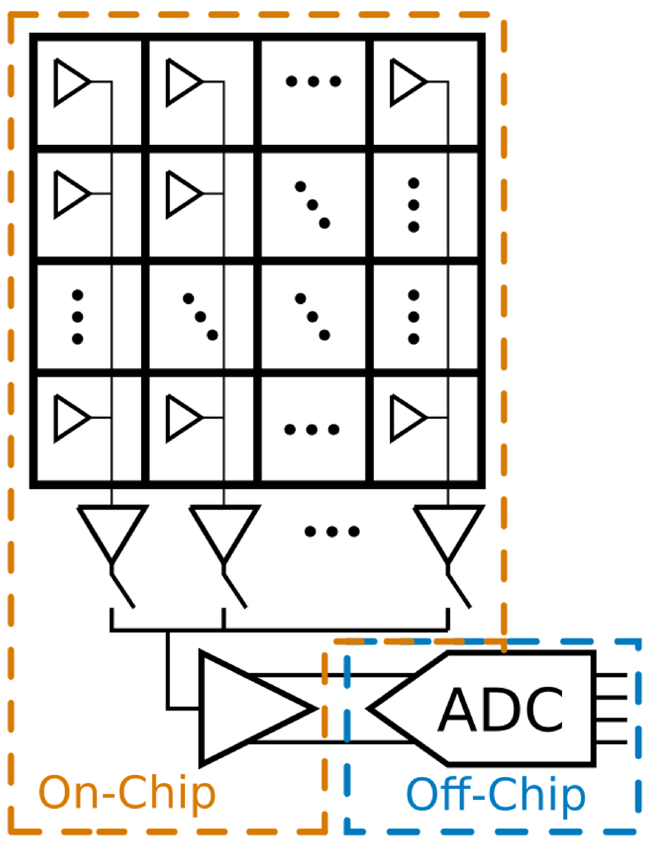
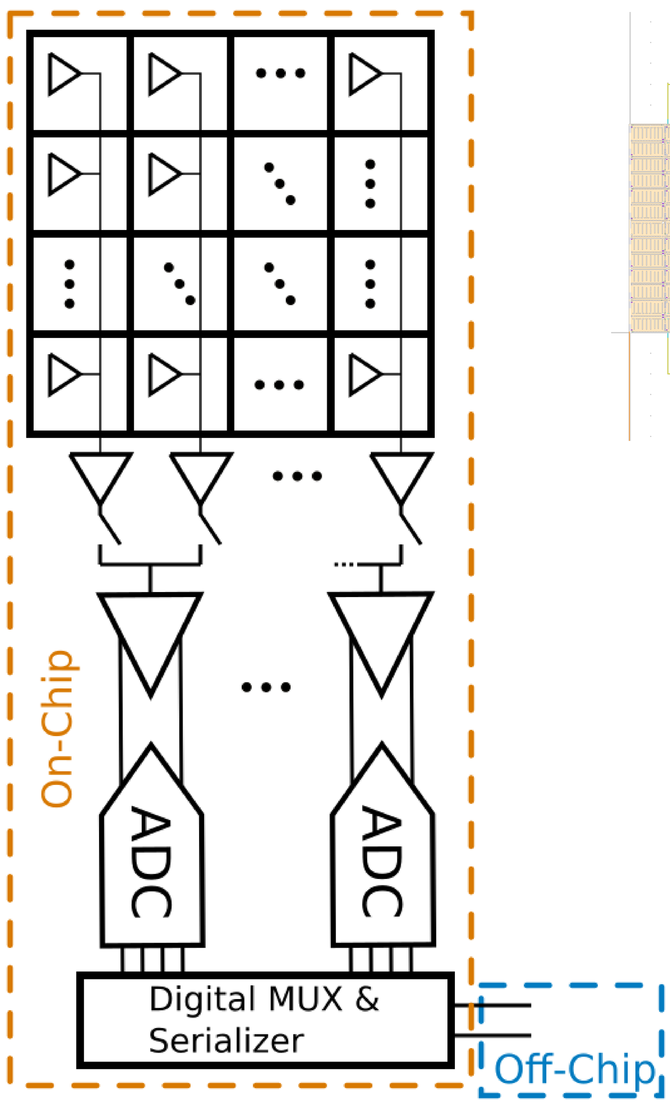
The future charge-integrating JUNGFRAU2.0 detector for high-rate synchrotron experiments

- Rate limitation of photon counting detectors due to pile-up already a problem at 3rd generation synchrotrons [1].
- Rate limitation will worsen at 4th generation synchrotrons

➔ Photon-counting at rates of >20 MHz/pixel difficult
➔ Charge-integrating detectors needed to overcome rate limitations



Data flow and digitization of JUNGRAU1

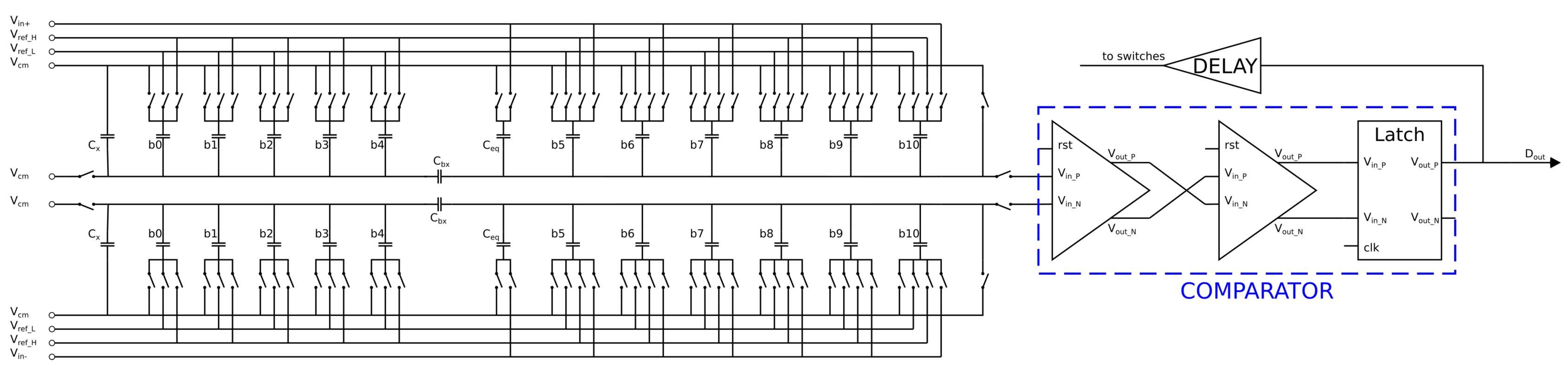


Data flow and digitization of JUNGRAU2.0

High speed analog buffers (>100 MHz) are difficult to design
➔ **More ADCs** (not faster ones!) are required
Numbers of output pads are limited
➔ **On-Chip ADCs** together with high speed (>3 GHz) serial links as solution

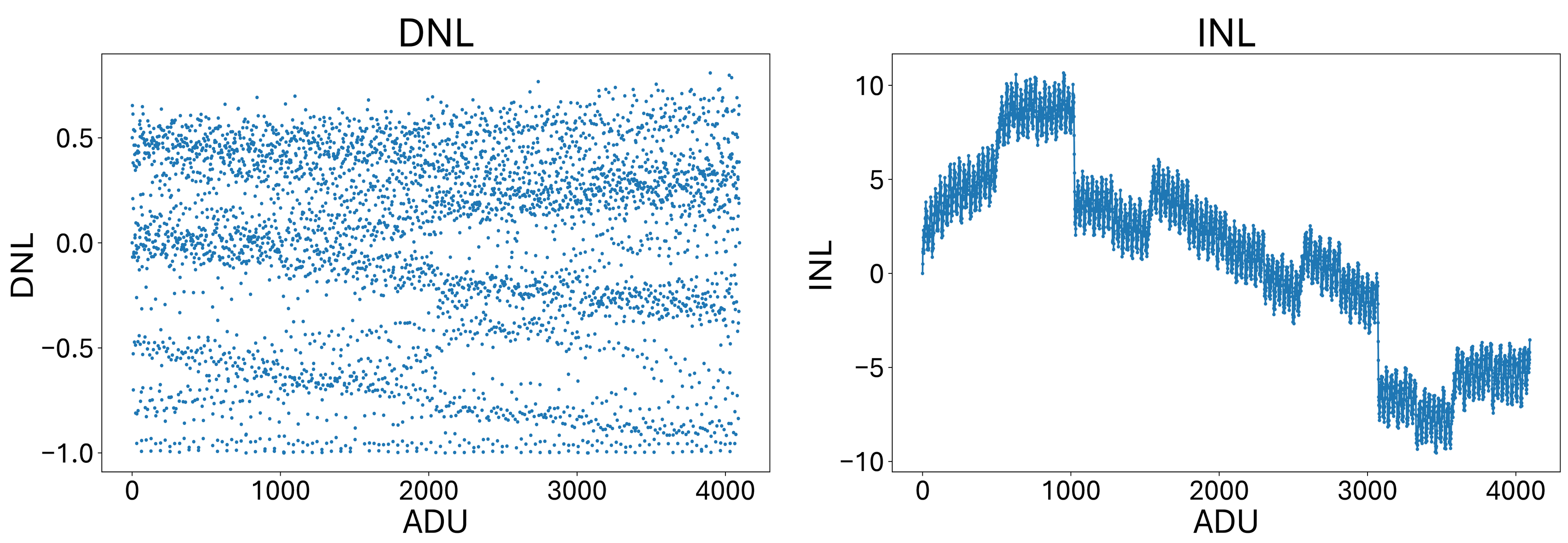
Details of the current JUNGFRAU1 can be found in [2]

SAR ADC architecture: Trade-off between power and speed



- 12-bit binary-weighted **S**uccessive **A**pproximation **R**egister (SAR) ADC
- Fully asynchronous control with configurable delay between bits
- Differential, switched-capacitor design
- Capacitive bridge to reduce area by a factor of 64

Predecessor ADC-SAR-04

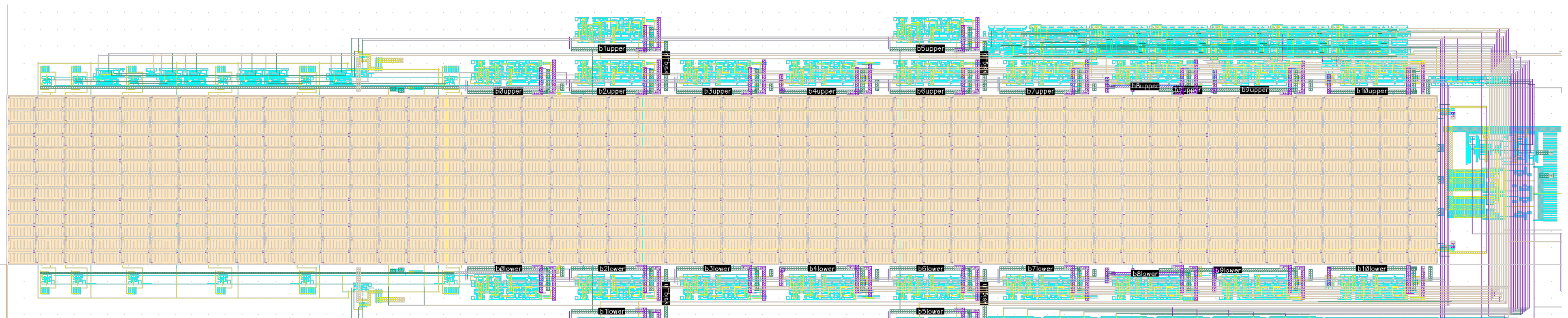


Sine-wave Histogram Testing of ADC-SAR-04 (raw data)

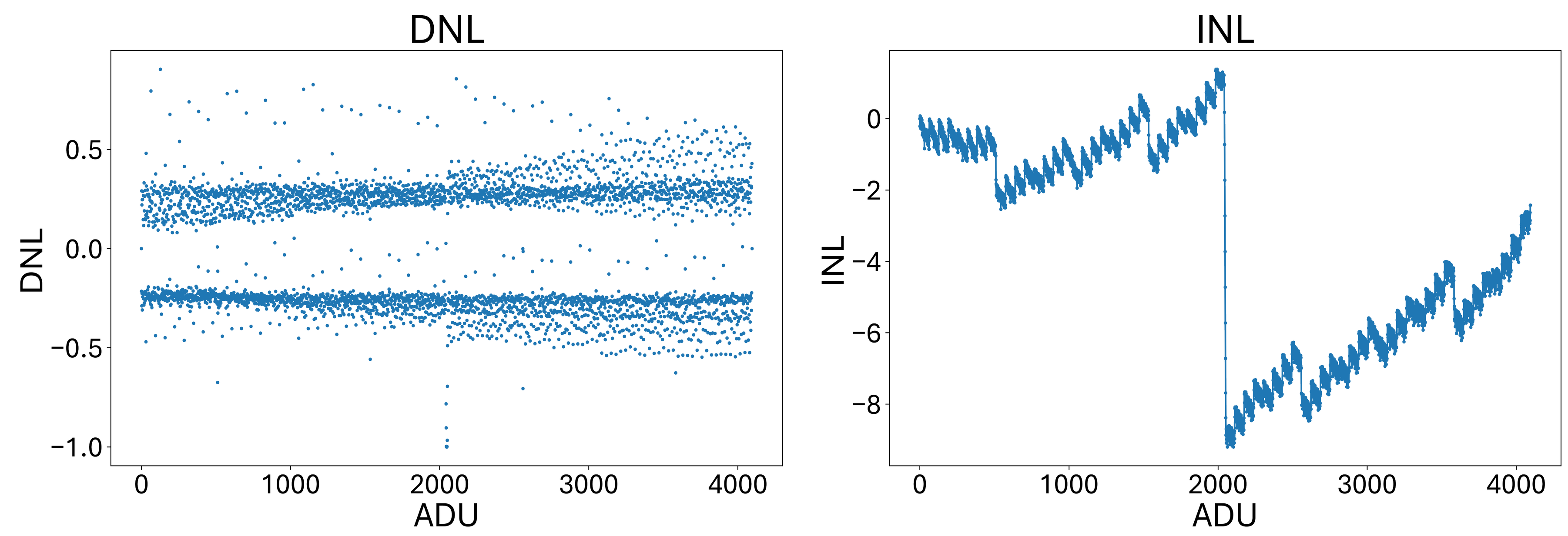
- Poor linearity due to **insufficient settling time of the signal** and **mismatch in the capacitor array**
- Maximum possible speed: 18 MHz (Shown: 1 MHz)
- The results show raw data. As shown in [3], calibration can significantly improve the results to a resolution of ~10 bit.

ADC-SAR-05

- UMC 110nm process
- Received October 2024
- 12-bit capacitive SAR architecture
- Unit capacitor size: 20 fF (same as in ADC-SAR-04, shown here)
  - 10 fF and 5 fF versions available
- Focus on linearity optimization instead of speed
  - Maximum possible speed: 16.6 MHz (Shown: 1 MHz)

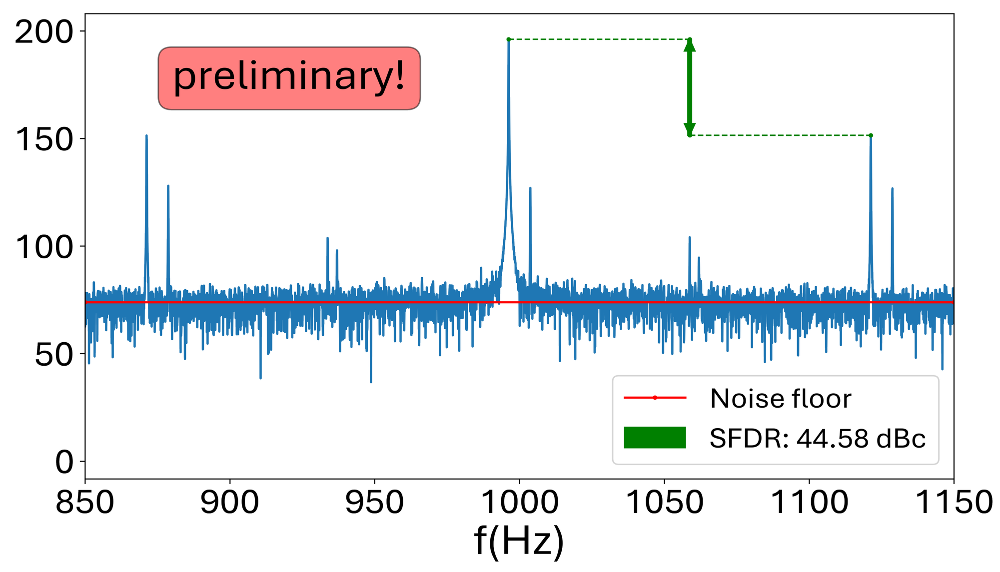

Layout of ADC-SAR-05

Results



Sine-wave Histogram Testing of ADC-SAR-05 (raw data)

➔ **Improvement of INL/DNL by a factor of ~2**
➔ Max. reasonable speed to be determined (trade-off between linearity and speed, likely ~10 MHz)



Spectral Analysis of ADC-SAR-05 with 995 Hz tone

- 1 MHz sampling frequency
- Distortions caused by measurement setup (discontinuous data)
- First Spectral and Dynamic characterization by this group!

➔ Only SFDR measured so far, SINAD and ENOB to be determined

Conclusion and Outlook

➔ Main goal of **linearity increase** achieved
➔ Speed limited by design mistake, not conceptual. (Limit with **5 fF unit capacitors** probably **around 60 MHz**)

➔ Configuration of ADC-SAR-05 to be done to determine maximum sampling speed
➔ Spectral analysis to be finished to measure ENOB

ADU = ADC Units
DNL = Differential Non Linearity
INL = Integral Non Linearity
SFDR = Spurious Free Dynamic Range
SINAD = Signal over Noise and Distortion
ENOB = Effective Number of Bits

References

[1] A. Bergamaschi, A. Mozzanica & B. Schmitt. XFEL detectors. Nat Rev Phys 2, 335–336 (2020). https://doi.org/10.1038/s42254-020-0200-x

[2] Characterization results of the JUNGFRAU full scale readout ASIC. A. Mozzanica et al 2016 JINST 11 C02047

[3] Design and first tests of the Gotthard-II readout ASIC for the European X-ray Free-Electron Laser. J. Zhang et al 2021 JINST 16 P04015