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A 28 nm CMOS front-end circuit with in-pixel flash ADC for high-rate hybrid detectors

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New developments in the field of instrumentation for high energy physics experiments are being carried out worldwide by several research groups in the 28 nm CMOS technology. In the design of pixel readout circuits, such a technology node promises to push more intelligence at pixel level, while higher bandwidths can be achieved in I/O circuits thanks to improved transition frequencies of the MOS transistors.
This work is focused on the design and characterization of a proof-of-concept, CMOS front-end circuit for pixel detectors. The circuit has been designed in a high-performance 28 nm process, optimized for high speed, and includes a charge sensitive amplifier with detector leakage compensation, together with a 2-bit flash ADC. The readout channel, which can handle subsequent events with zero dead time, has been integrated in a 4x8 pixel matrix in a 1x2 mm2 prototype chip. The conference paper will provide a discussion on the design of the front-end circuit and will gather the main results from the characterization of the test chip.

Primary experiment

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