ASTRA-64 : Tests and Characterization of a Silicon Micro-Strip Detectors Read-Out ASIC

Gianluigi Silvestre[1], G. Ambrosi[1], M. Barbanera[1], F. Cossio[2], M. D. Da Rocha Rolo[2], M. Duranti[1], R. A. Giampaolo[3], M. Movileanu[1], P. Placidi[1], A. Rivetti[2]

(1) Istituto Nazionale di Fisica Nucleare – Sezione di Perugia
(2) Istituto Nazionale di Fisica Nucleare – Sezione di Torino

INTRODUCTION

Silicon strip detectors remain a popular choice due to their flexibility and capability to achieve high spatial resolutions, ranging from tens of μm to less than 5 μm while covering large areas up to several square meters.

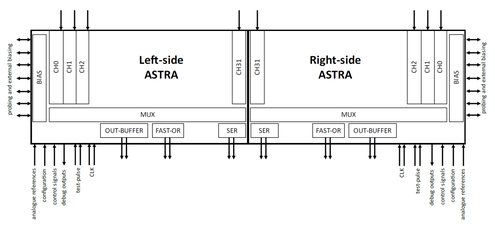
The ASTRA-64 (Adaptable Silicon sTrip Read-out ASIC) is a 64-channel mixed-signal ASIC designed to read micro-strip silicon detectors.

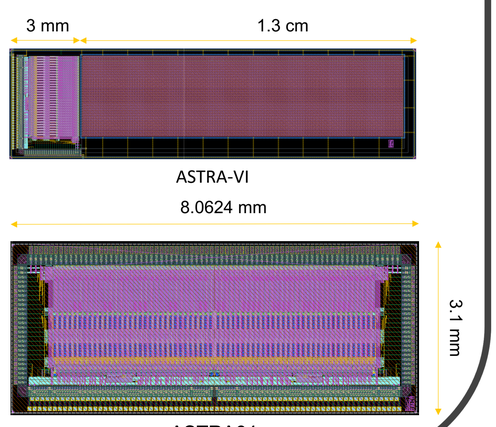
The first prototype was developed in the framework of the INFN project ARCADIA with two different versions:

- 64 channel read-out: ASTRA64
- 32-strips fully-depleted monolithic active CMOS microstrip sensor: ASTRA-VI

The two versions share the same electronics

- configurable Gain
- configurable Peaking Time
- configurable Readout mode (analog or digital)



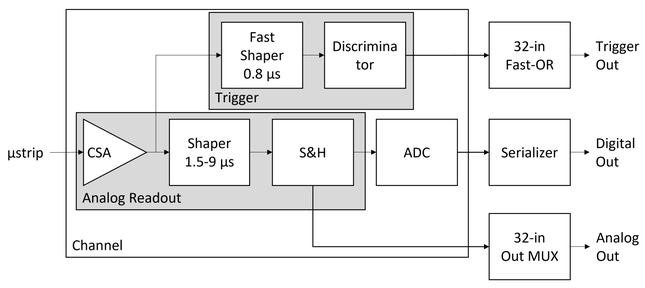


ASTRA REQUIREMENTS

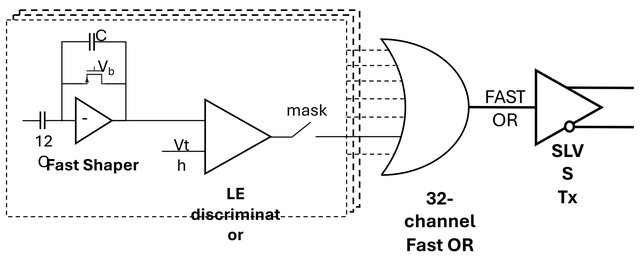
- Designed by INFN Torino
  - Electronics for the read-out 110-μm-pitch silicon μStrip Detectors
  - Electronics + Sensor Monolithic ASIC
- Requirements tailored to HERD Silicon Charge Detector (SCD)
- Produced at LFoundry

	ASTRA Requirements
Channels	64
Dynamic Range	± 160 fC
Linearity Region	± 160 fC
Shaping Time	Adjustable in 1÷10 μs
ENC	< 1000 e^- @ C_{in} 100 pF
Output	Multiplexed pulse height, Digitized pulse height, Channels FastOR
Power supply	Positive (only) supply
Channel power consumption	< 1 mW per channel
Production Process	110 nm CMOS
Size	6x6 mm^2

ASTRA ARCHITECTURE



General architecture



Fast Shaper block

PreAmp
Charge Sensitive Amplifier
Test-pulse injection circuit

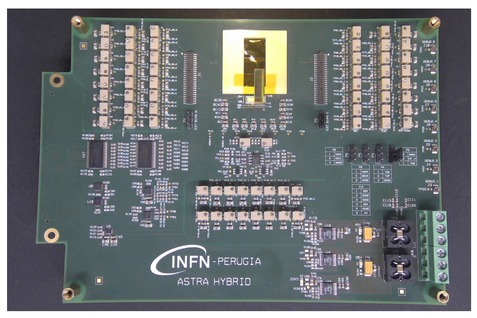
Slow Shaper
Charge measurement
Externally-controlled S&H circuitry

Analogue readout
MUX-differential output buffer

Digital readout
Wilkinson ADC and serializer

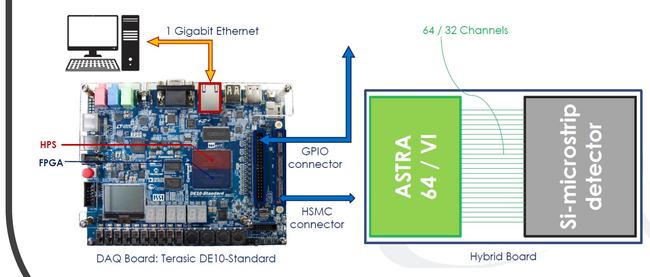
Fast Shaper
Trigger output
Fast-OR output

TEST BOARD



PCB

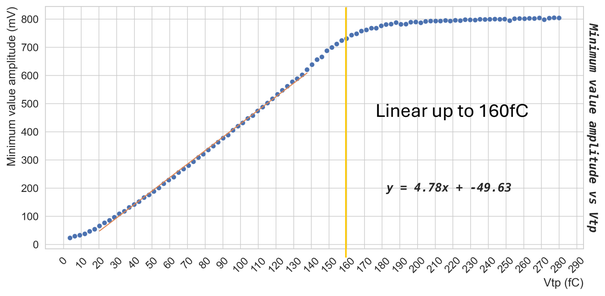
- ADCs for analog output digitization
- Analog/Digital Power Supplies
- Level shifters and SLVS converters
- Trimmer resistors for external bias
- Sensor HV bias



DAQ

- ASTRA configuration, readout operations, and data acquisition
- *Terasic DE10-Standard*
- *Intel Cyclone V* FPGA

PRELIMINARY CHARACTERIZATION



V_{tp} scan for standard gain @ 6.5μs peaking time

Gain (mV/fC)	V_{tp} 3.5 μs	V_{tp} 6.5 μs	V_{tp} 9 μs
Standard	4.42	4.78	4.85
High	7.56	8.72	9.19

- Freeze one channel in output and send *integrated* test pulses (V_{tp})
- V_{tp} scan by varying combinations of the parameters
  - Gain: Standard / High
  - Peaking Time: 3.5 μs, 6.5 μs, 9 μs
- Conversion from V_{tp} to Q_{inj}
  - C_{inj} = 240 fF
- Measurement of front-end linearity dynamic range and real gain for various configurations

CONCLUSION

- ASTRA64: 64-channel ASIC readout electronics for Si μStrips
  - in house design of versatile chip
  - possible application in different space and ground experiments
- Each ASTRA channel performs signal amplification and charge measurement
  - Positive and negative input signal polarities readout capability
  - 2 gain settings providing input dynamic range up to 80 or 160 fC
  - 4 peaking time configurations: 1.5 μs, 3.5 μs, 6.5 μs, 9 μs
  - Dual-readout mode: analog and digital
  - FastOR trigger output
- ASTRA characterization still in progress
  - Exploit all the functionalities
  - Optimize behavior with external biases
  - Use it in actual beam tests

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