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ASTRA-64 : Tests and Characterization of a Silicon Micro-Strip Detectors Read-Out ASIC

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Silicon strip detectors remain a popular choice in various fields of physics due to their flexibility and capability to achieve high spatial resolutions, ranging from tens of micrometers to less than 5 micrometers while covering large areas up to several square meters. The ASTRA-64 (Adaptable Silicon sTrip Read-out ASIC) is a 64-channel mixed-signal ASIC designed to read micro-strip silicon detectors. Designed in 110 nm technology, ASTRA-64 consists of two mirrored blocks of 32 channels. Each channel is equipped with a Charge-Sensitive Amplifier featuring two programmable gain settings for both input signal polarities, followed by a shaper with programmable peaking time to optimize noise performance based on the detector's capacitance.

ASTRA-64 supports two read-out modes: an analog mode, where charge information is transmitted off-chip via an analog multiplexer, and a digital mode, which embeds a Wilkinson ADC per channel for voltage digitization. The front-end gain configuration allows linear charge measurements up to 160 fC in standard gain and 80 fC in high gain mode. Finally, a fast shaper coupled with a leading-edge hysteresis discriminator enables rapid trigger signal generation through FAST-OR logic from the 32-channel discriminator outputs.

This work presents the testing, characterization, and performance evaluation of the ASTRA-64 chip.

Primary experiment

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