OBELIX: A DMAPS chip for the Belle II VTX Upgrade

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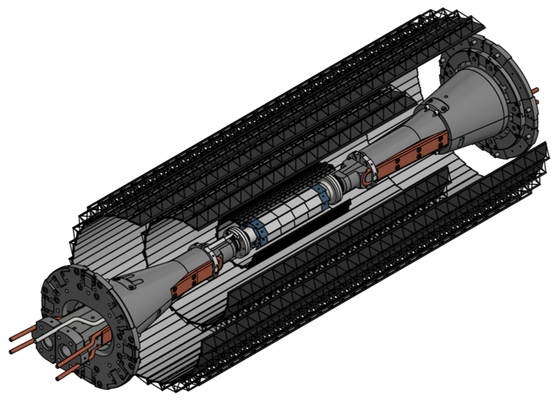
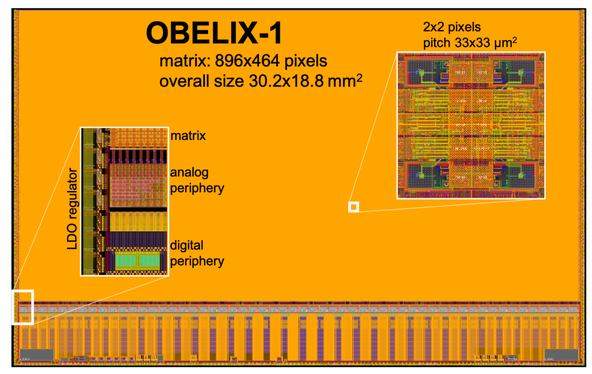
on behalf of the VTX Upgrade Group

The VTX Upgrade

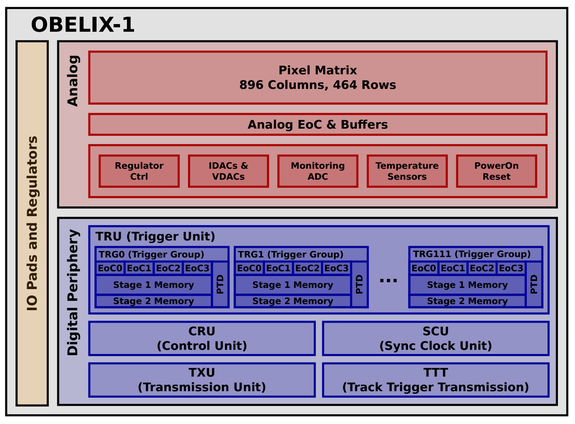
- Opportunity to upgrade the Belle II Vertex Detector during Long Shutdown 2 (Around 2032)
- Interaction region upgrade possible: Rework of the Vertex Detector necessary
- Improves tracking performance at increased beam background due to luminosity increase
- Five layers using the same DMAPS sensor: The OBELIX (**O**ptimized **BEL**le II p**IX**el) Chip
- Fully pixelated design for low occupancy and fake-rate at high hitrates
- iVTX (2 inner layers): Self supported, air/liquid cooled, all silicon ladders, redistribution layer
- oVTX (3 outer layers): Carbon fiber support, liquid cooled
- See talk from R. Boudagga on Monday





The OBELIX-1 Chip

- Matrix derived from TJ-Monopix2
- 464 rows and 896 columns
- Timestamping: 47 ns
- Up to 10 µs trigger latency
- Hitrates up to 120 MHz/cm^2
- Power: < 200 mW/cm^2
- TID tolerance: 1 MGy
- NIEL tolerance: 5×10^{14} n_{eq}/cm^2
- LV Supply: 2 to 3 V

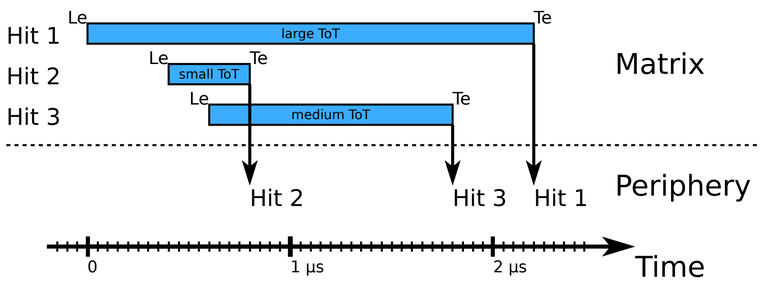


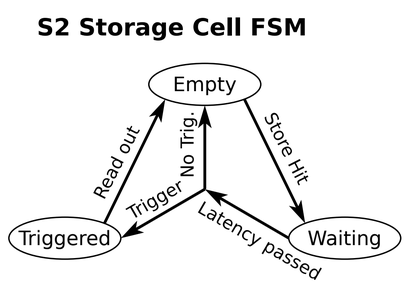
New On-chip features

- Trigger memory (TRU)
- Precision timing measurement (PTD)
- Transmission for trigger contribution (TTT)
- LDOs for wide LV supply voltage range
- 32 temperature sensors across the chip
- Daisy chaining: planned for OBELIX-2

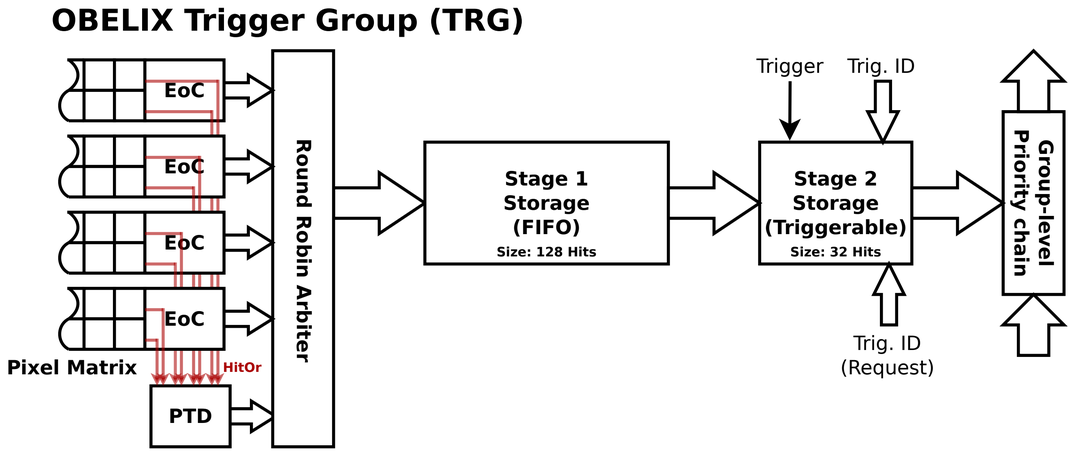
Trigger Unit (TRU)

- Column drain readout architecture of the Matrix
- Data is released to matrix after ToT period
- Data is not chronologically ordered ⇨ Needs to be handled by TRU





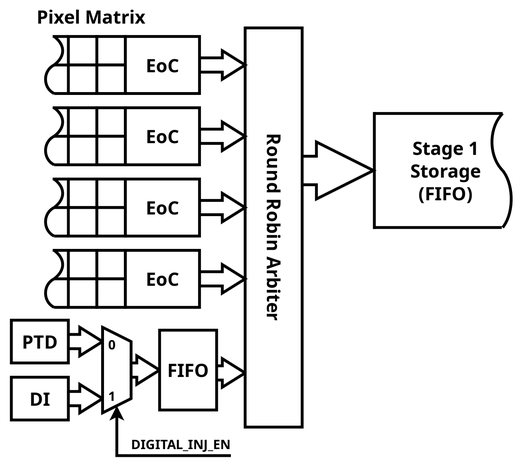
OBELIX Trigger Group (TRG)

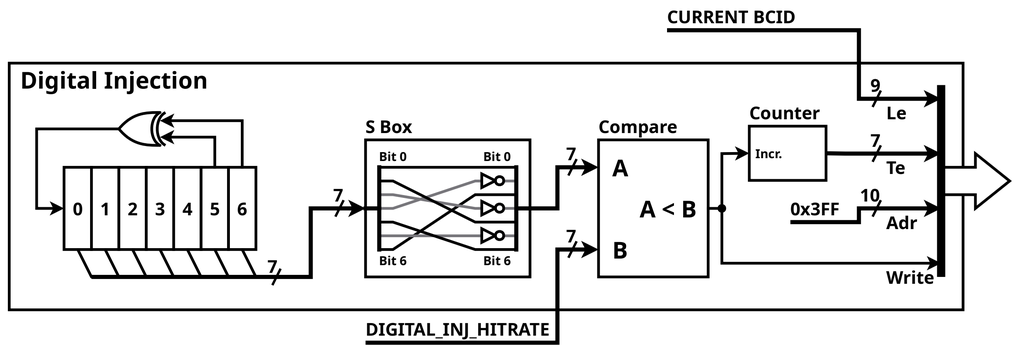


- TRU is organized into Trigger Groups (TRG)
- Each TRG handles 4 double columns, each with an end of column circuit (EoC)
- Two-stage memory in each TRG for storage during the trigger latency
- Stage 1: SRAM based FIFO for initial storage: compact, energy efficient
- Stage 2: Associative memory for triggering: smaller but power hungry
- Each storage cell in S2 has an FSM comparing current BCID with contents
- As soon as space in S2 is avilable, it is filled from S1
- Maximum ToT is about 3 µs ⇨ this is the magnitude of the expected time-disorder
- Stage 2 needs to cover at least the last 3 µs of the latency
- Stage 1 covers the remaining time before that

Design For Test Stategy

- Register rich design: Stage 2 is built from D-FFs
- Scan chains would cause significant overhead
- Custom test pattern generator implemented
- Can inject hitdata at the RR-Arbiter
- Selectable injection rate
- Can operate during normal chip readout, i.e. charge injection scans
- Fully deterministic operation
- Very low footprint (die area)

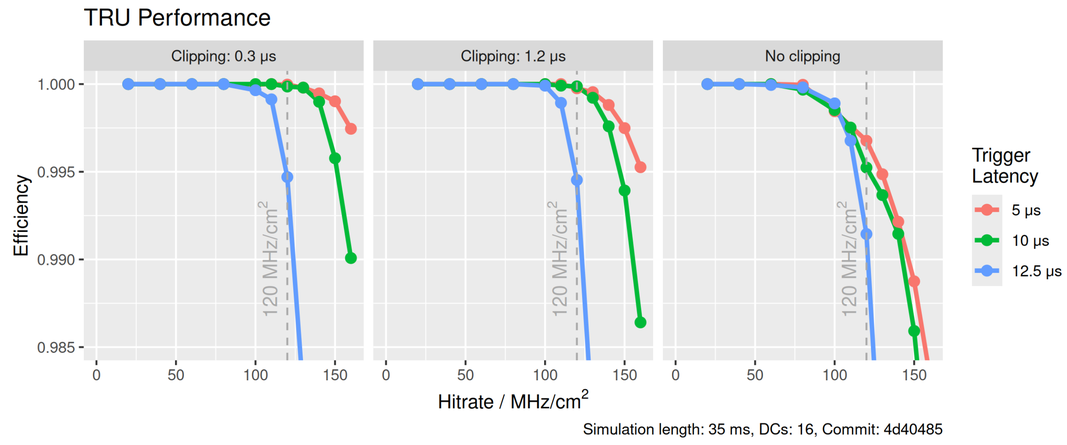




- Fibonacci linear feedback shift register
- Substitution box to scramble bits of SR around
- Comparator with threshold reference
- Inject hit if below threshold
- Initial value (seed) is different for each TRG and can be overwritten by configuration
- Allows to fill up trigger memory and the trigger on specific values
- Also useful at testbeams: artificially add 'background hits' without external circuitry

TRU Performance Simulations

- Realistic hit distribution, landau and charge sharing
- Check performance of the trigger unit block
- Verify sizing of the memories



- ToT clipping affects performance via allowed time-disorder
- With strong ToT clipping, the total size of S1+S2 is the limiting factor:

⇨ Performance depends on selected trigger latency

- With no ToT clipping, the time that the data stays in S2 is the limiting factor:

⇨ Performance less affected by trigger latency setting

- Optimal prformance for a target clipping of 1.2 µs