ÖAW AUSTRIAN ACADEMY OF SCIENCES

HEPHY INSTITUTE OF HIGH ENERGY PHYSICS

RD50 HV-CMOS Meeting

RD50-MPW4

Investigating DACs

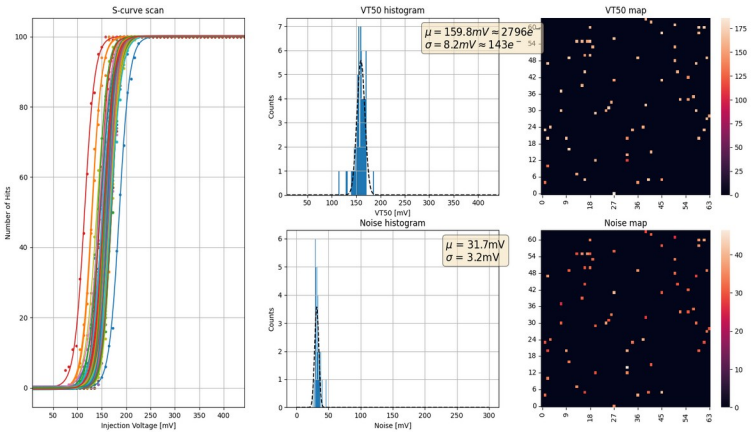
Bernhard Pilsl

DAQ news

- GUI seems to have some bugs
  - Compilation needs specific Qt version, otherwise some „#include“ are missing
  - Control tab making problems, use „pearycli“ until problem sorted out
- New method *dacScan* implemented to scan range of DAC and perform S-curves
  - In „mpw4_dev“ branch
- Added „power report“ (from LDO readback) to S-curves output file
- I2C bug fix
  - At every write operation the subsequent register was also written
  - Did only work until now because always all registers got written in the „correct“ order
  - Mandatory for everyone who wants to perform DAC scans
  - Fix in „mpw4_dev“ branch

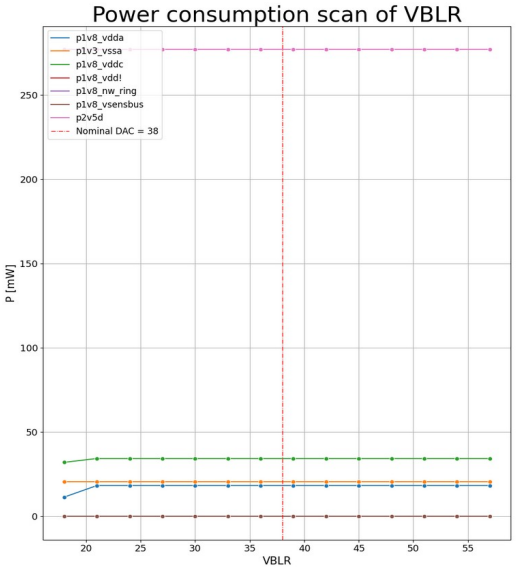
Methods

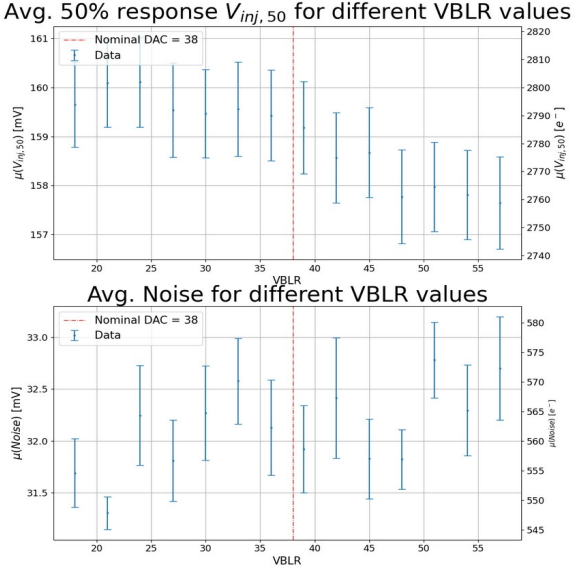
- Record S-curves for 32 pixel (to save time)
- Fit S-curves → Extract halfway point $V_{inj,50}$ and Noise
- Fit $V_{inj,50}$ and Noise to Gauss
- Use μ of the Gauss
- For power consumption read out current from LDO via Peary
  - Also measuring various chips and resistors on PCB
  - Shunt resistors placed right after SAMTEC connector, measuring just the chip with current PCB not (easily) possible
- Scan 1 DAC at a time in range nominal +- 20
- DAC values as shown written via I2C
  - Get bitwise inverted in MPW4



VBLR

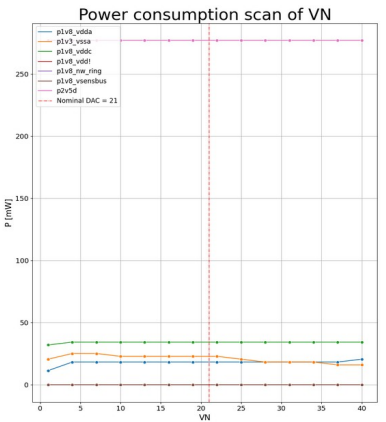
- No significant impact on any characteristic

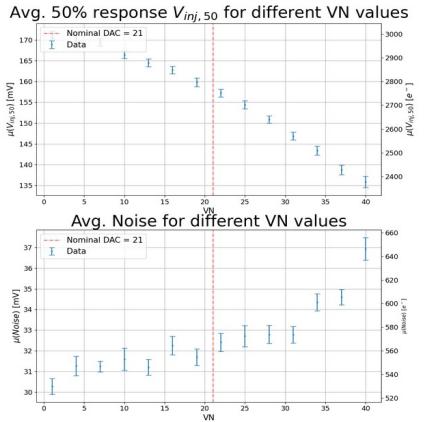


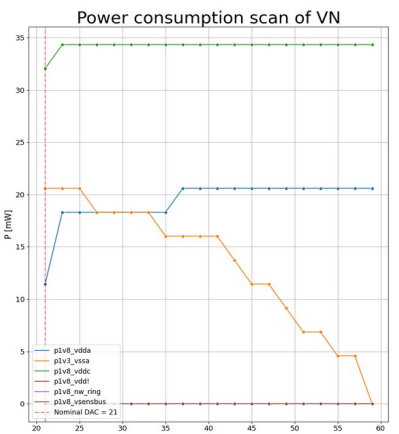


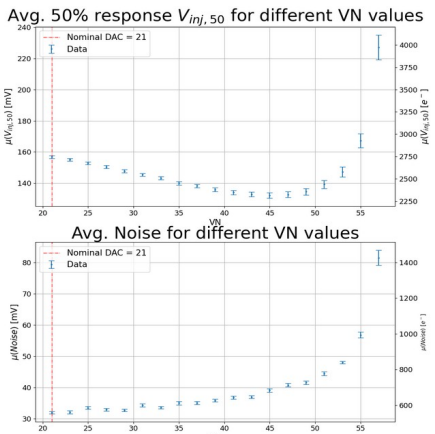
VN

- Power consumption at 1V3_VSSA lower at higher DAC values
- $V_{inj,50}$ lower (better) at higher DAC values



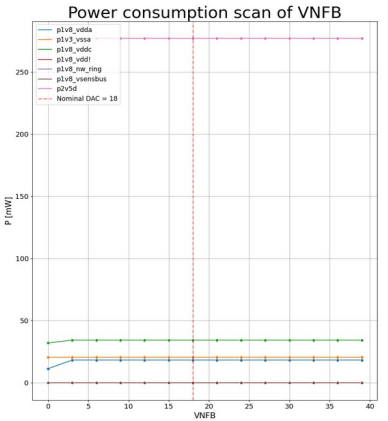


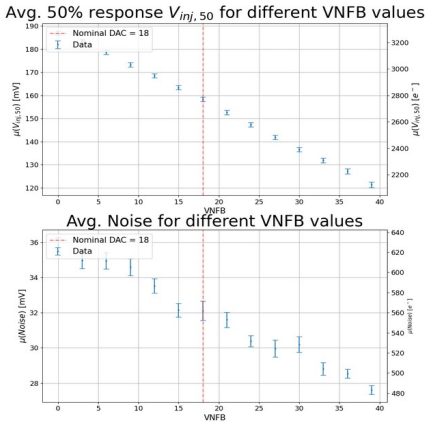


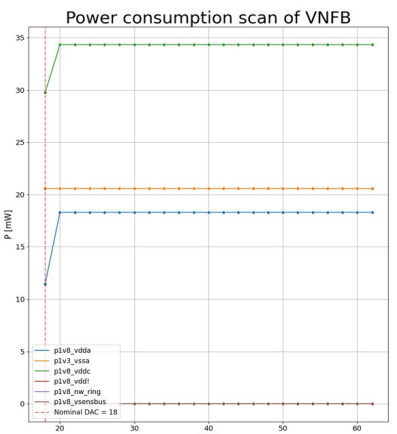


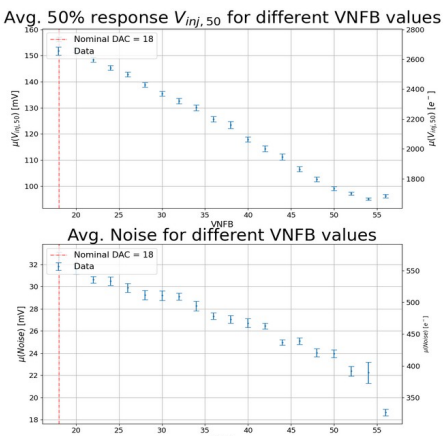
VNFB

- Power consumption „constant“
- $V_{inj,50}$ lower (better) at higher DAC values
- Noise lower (better) at higher DAC values



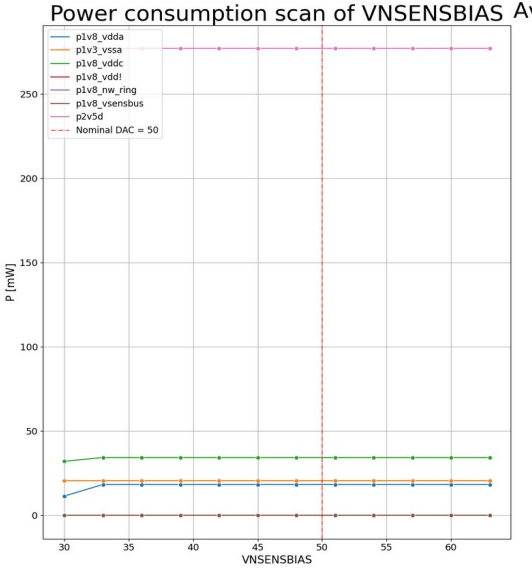


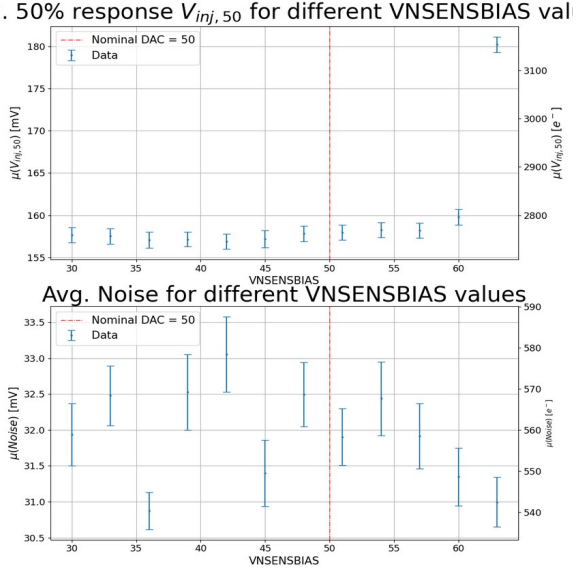




VNSENSBIAS

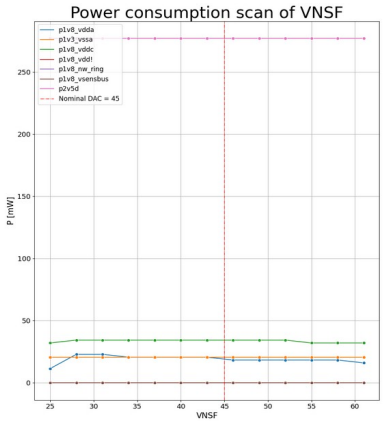
- No significant impact on performance

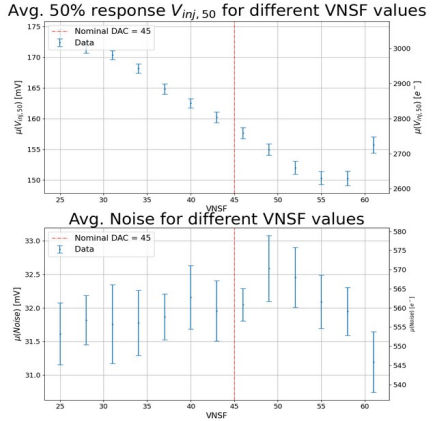


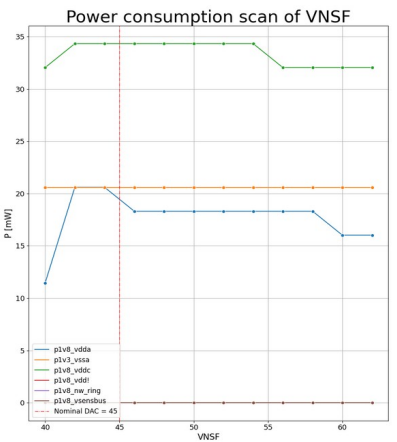


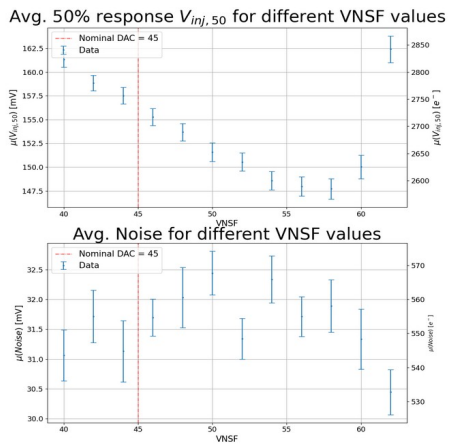
VNSF

- At higher DAC values:
  - Reduced power consumption at p1V8_VDDC and P1V8_VDDA
  - $V_{inj,50}$ lower (better)



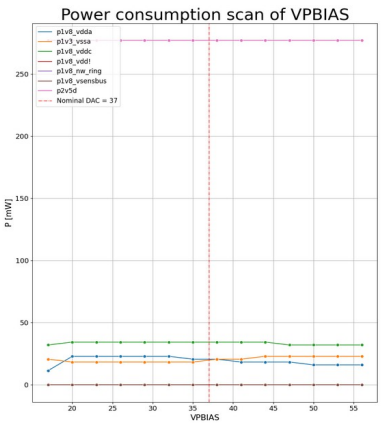


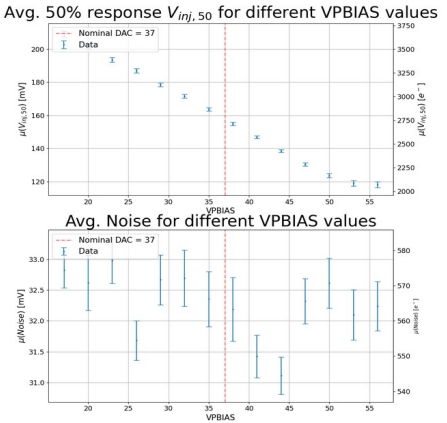


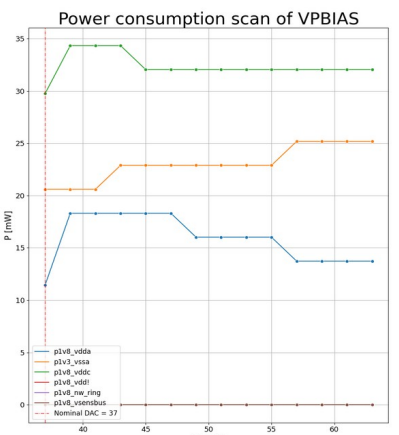


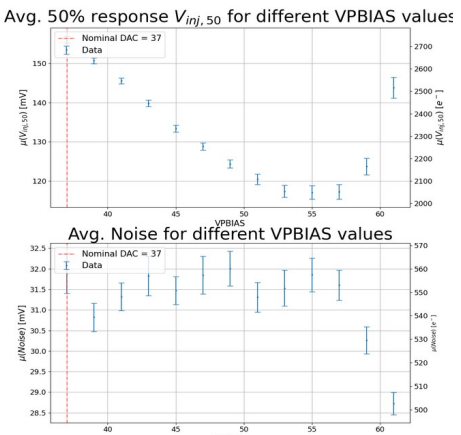
VPBIAS

- At higher DAC values:
  - Increased power consumption at P1V3_VSSA
  - Decreased power consumption at P1V8_VDDC, P1V8_VDDA
  - $V_{inj,50}$ lower (better)



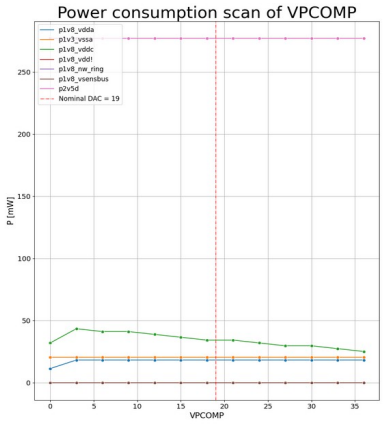


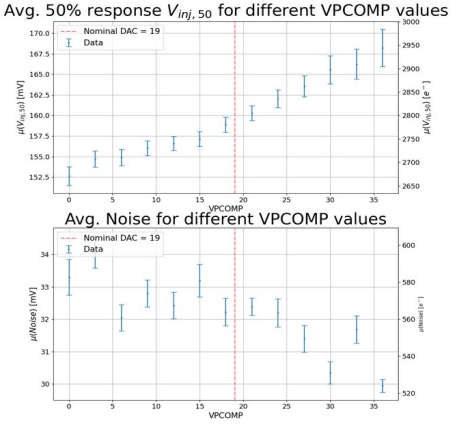


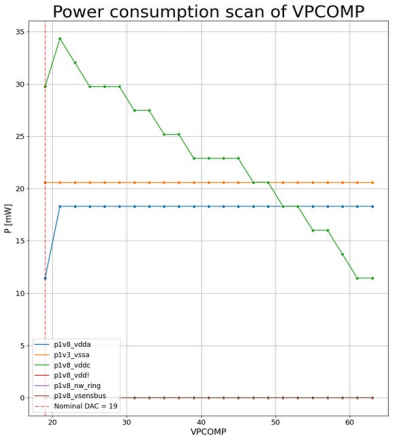


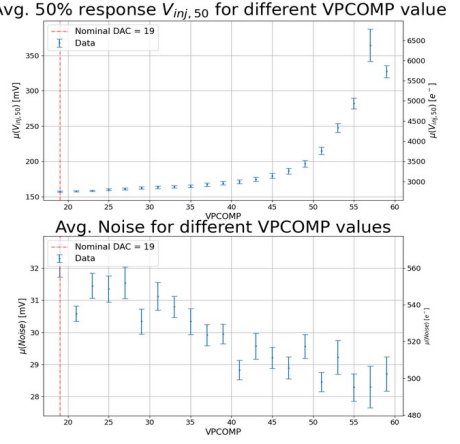
VPCOMP

- At higher DAC values:
  - Drastically reduced Power consumption at higher DAC values for P1V8_VDDC
  - $V_{inj,50}$ higher (worse)





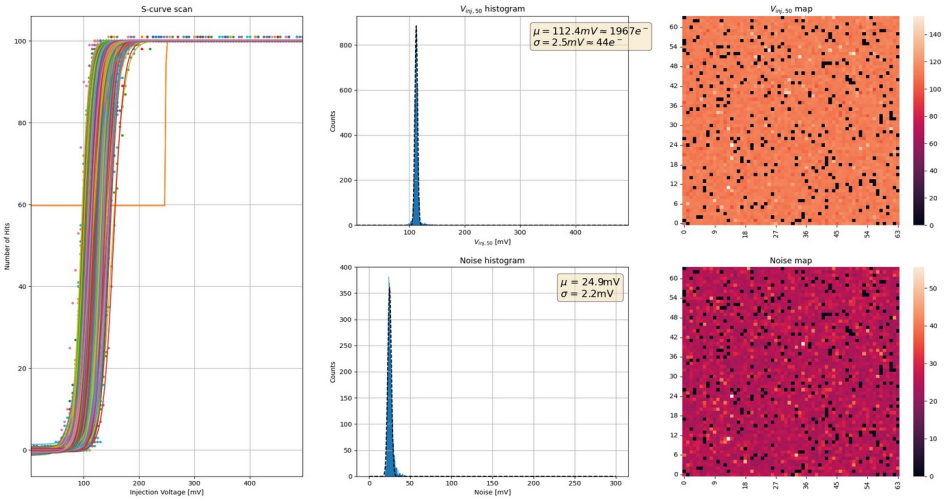




„Modified“ DAC values

- Adjusted DAC values to fit „best“ $V_{inj,50}$ behavior
- Possible interplay between various DACs not investigated (so far)

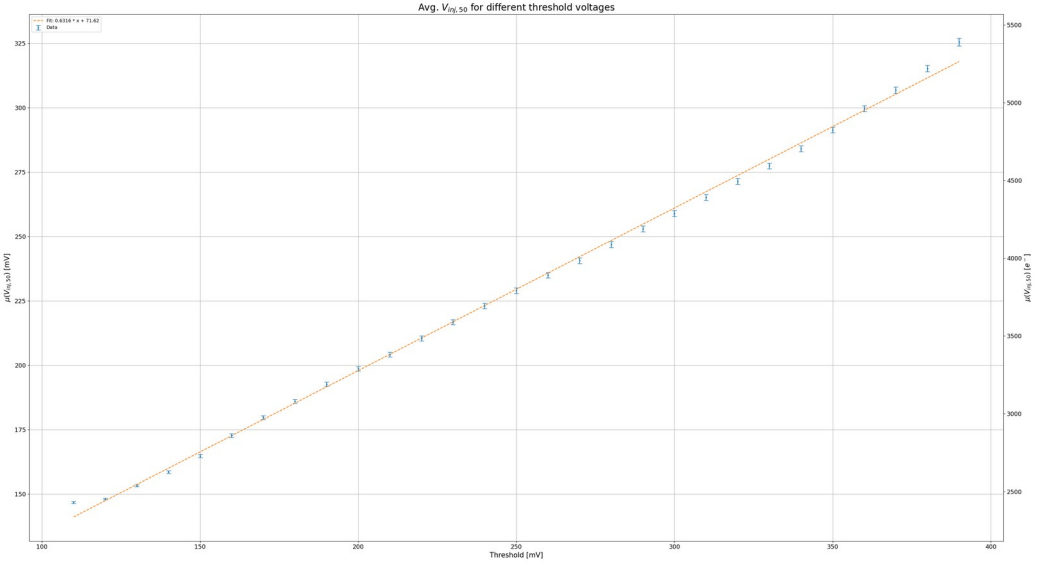
DAC	Nominal	“Modified”
VN	0x15	0x2D
VNFB	0x12	0x34
VNSF	0x2D	0x34
VPBIAS	0x25	0x37
VPCOMP	0x13	0x13



- Higher threshold V_{thr} = 970mV needed (200V bias) for not running in noise
- Still effective threshold ($V_{inj,50}$) reduced to ~1970e^-
- With nominal DACs same routine results in V_{thr} = 920mV, but $V_{inj,50}$ ~ 2765e^-

Threshold scan with “modified” DACS

- Comparing linear fit to response vs. threshold behavior of nominal vs. “modified” DAC values
  - “Modified“: $\mu(V_{Inj,50}) \sim 0.63 * V_{Thr} + 71.62$
  - Nominal: $\mu(V_{Inj,50}) \sim 0.9 * V_{Thr} + 184.13$
- Nominal: steeper slope, larger offset
  - Larger offset explains why $V_{inj,50}$ smaller even at higher V_{Thr} with “modified“ DACs



Summary / Outlook

- Changing DAC settings allows us to be more sensitive / reducing $V_{inj,50}$
- There is room to reduce power consumption
  - Trade-off with sensitivity likely
- TODO:
  - Investigate interplay between different DACs
  - Do a proper power consumption study
    - LDO readback not well suited
      - See jumps in the power consumption curves (digitization effects?)
    - Shunt resistors not well suited
    - Solution?
  - Look into effects of DACs on ToT distributions
  - Are there side effects by operating the chip with the „modified“ DACs?
    - Operational point pretty different compared to nominal DAC settings