

# Smart Pixels: Towards radiation hard ASIC with on-chip machine learning in 28nm CMOS

Wednesday 16 October 2024 17:30 (15 minutes)

We introduce a smart pixel prototype readout integrated circuit (ROIC) fabricated using a 28 nm bulk CMOS process, which integrates a machine learning (ML) algorithm for data filtering directly within the pixel region. This prototype serves as a proof-of-concept for a potential Phase III pixel detector upgrade of the Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC). This chip, the second in a series of ROICs, employs a fully connected two-layer neural network (NN) to process data from a cluster of 256 pixels, identifying patterns corresponding to high-momentum particle tracks for selection and readout. The digital NN is embedded between the analog processing regions of the 256 pixels, maintaining the original pixel size. Its fully combinatorial digital logic circuit implementation minimizes power consumption, avoids clock distribution, and activates only upon receiving an input signal. The NN performs momentum classification based on cluster patterns, achieving a data rejection rate of 54.4% to 75.4% with a modest momentum threshold, opening up the possibility of using pixel information at 40 MHz for trigger purposes. The neural network NN itself consumes around 300  $\mu$ W. The overall power consumption per pixel, including analog and digital functions, is 6  $\mu$ W, resulting in approximately 1 W/cm<sup>2</sup>, within the permissible limits of the HL-LHC experiments. This presentation will showcase the preliminary testing results using Spacely, an open-source framework for post-silicon validation of analog, digital, and mixed-signal ASICs. Spacely maximizes hardware and software reuse, streamlining the testing process for small ASIC design teams in academia and research institutions.

## Focus areas

HEP

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**Session Classification:** Contributed talks