CERN lpGBT – Merging Timing, Data, and Control of Detectors

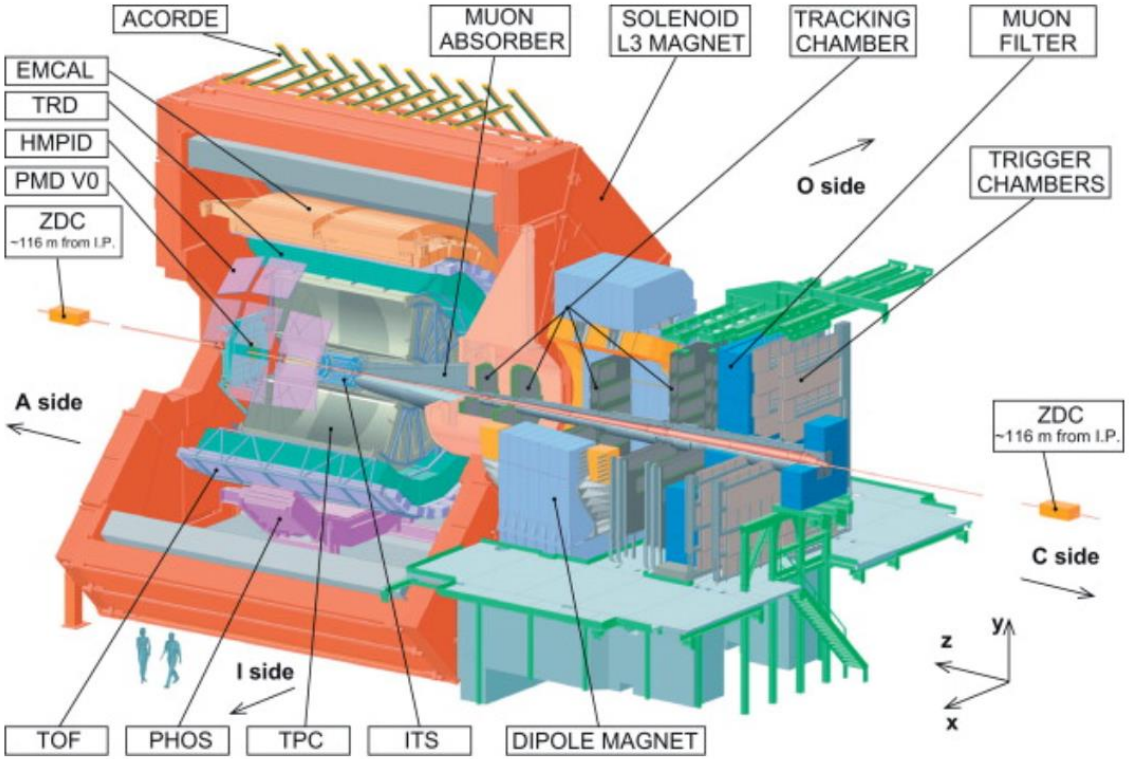
Tivadar KISS @ Wigner Research Centre for Physics, HUN-REN

Erno DAVID @ Wigner Research Centre for Physics, HUN-REN

14 March 2024

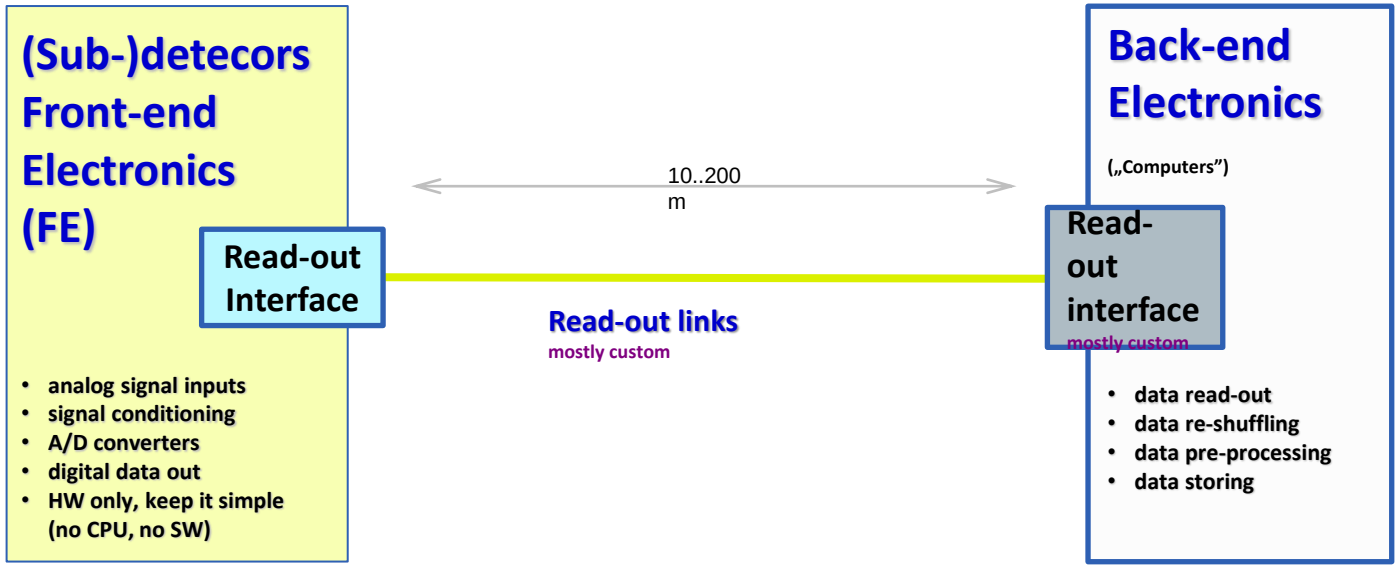
V4-HEP, Budapest, Hungary

Example - The ALICE detector (CERN LHC)



The Basic Task

Acquiring and storing of measurement data for later, offline analysis



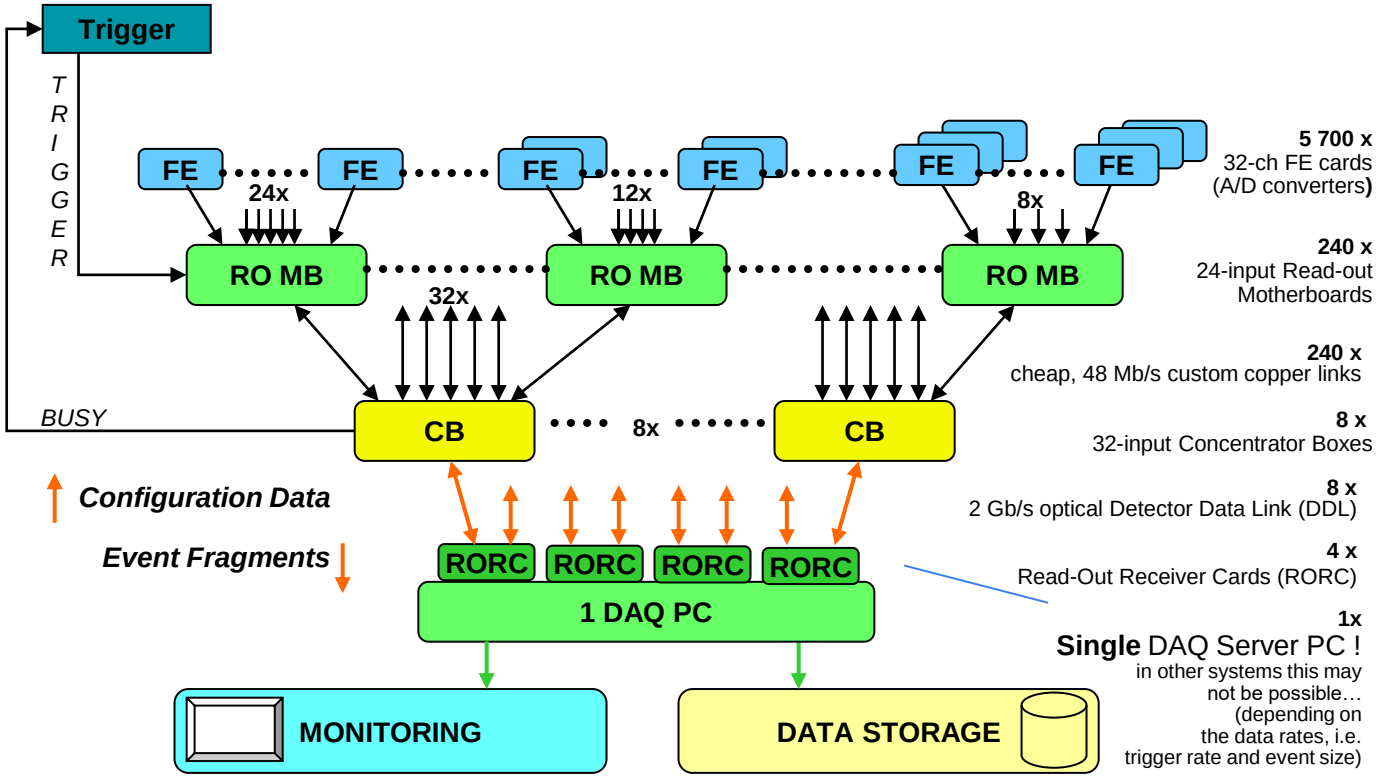
Special custom-developed electronics
- (Sub-)detector specific functional requirements
- Additional general, special requirements: (e.g. small size, low-power, low material budget, radiation tolerance, etc.)
- → lots of HW development

Industrial standard solutions
- no sub-detector specific HW requirements
- commercial, off-the-shelf components (to minimize HW development)
- lots of detector specific SW development (online and offline SW)

Large, unique systems: challanging data amount and data rates
„Big Physics" → „Big Data"

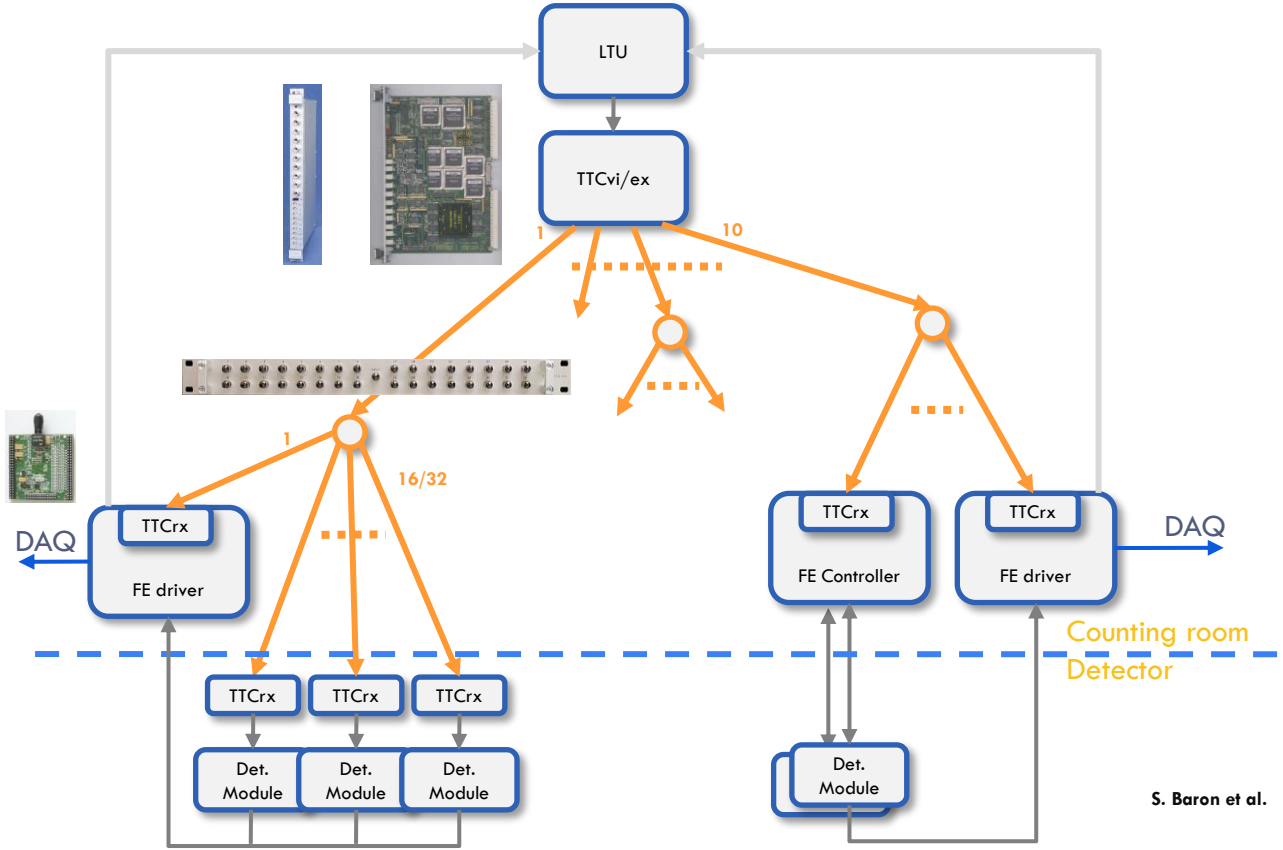
Data Concentrators Needed!

Example: CERN NA61 DAQ architecture

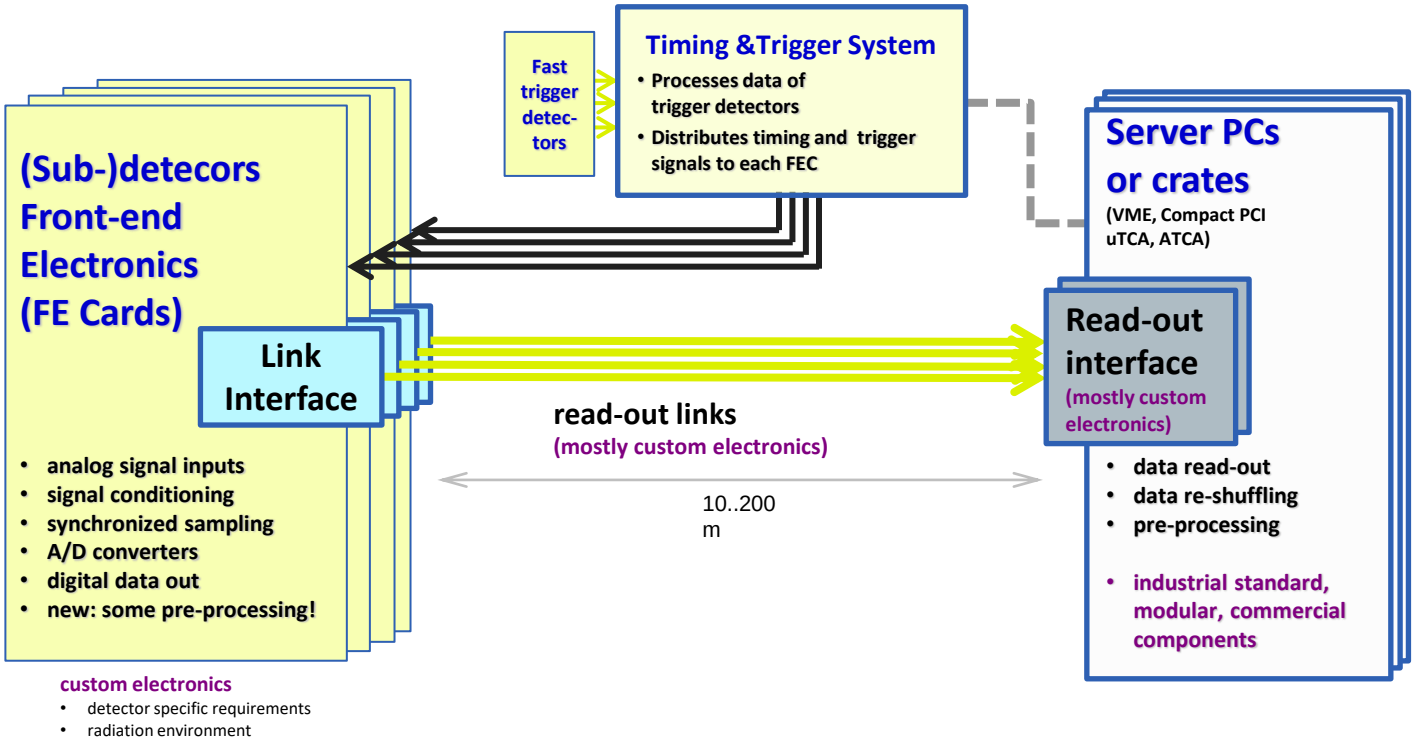


This simple, 1 server scheme is not possible wigth larger systems!

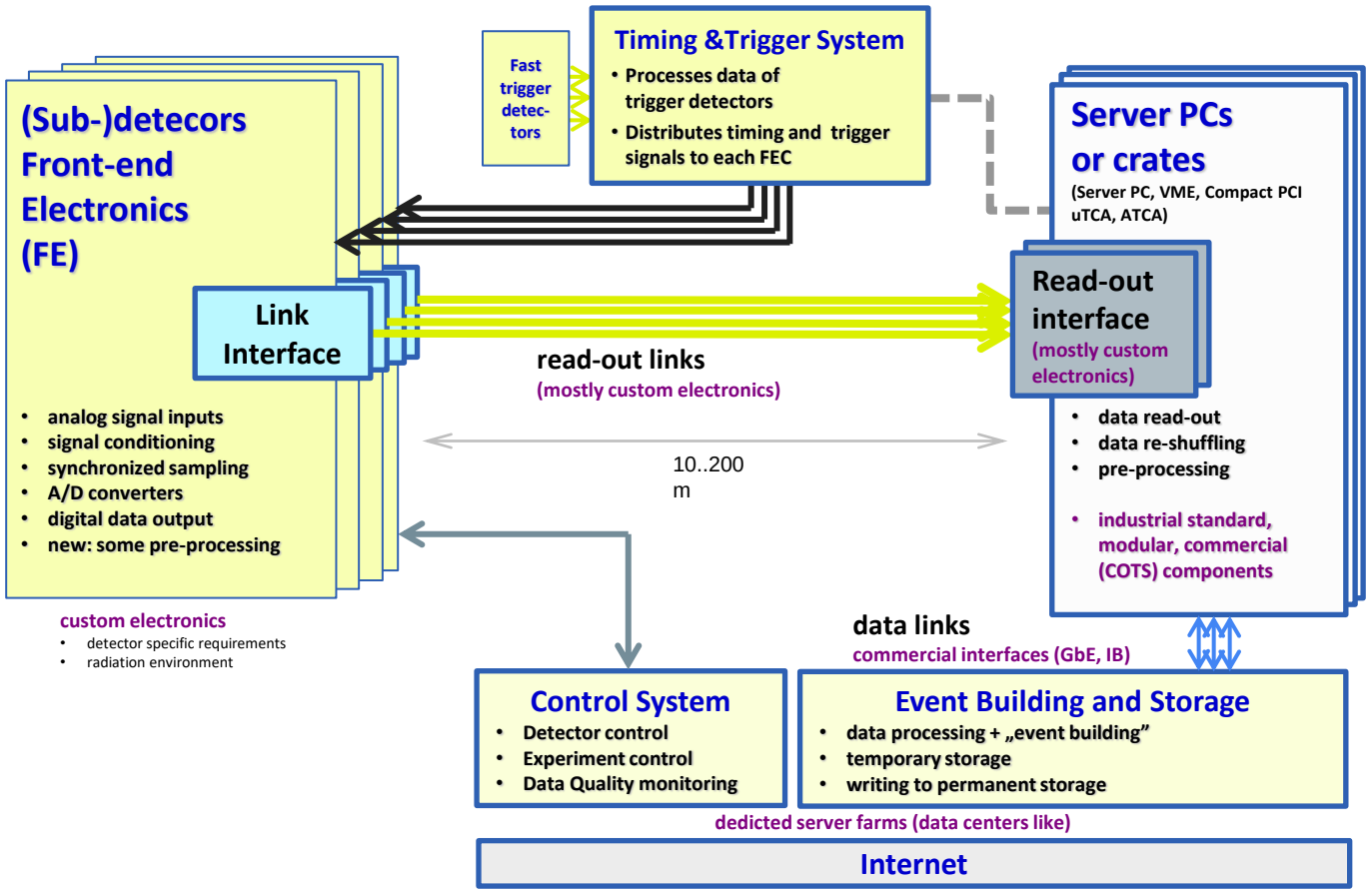
Legacy TTS System: CERN TTC



A Large System with Sync



The „Whole" Picture

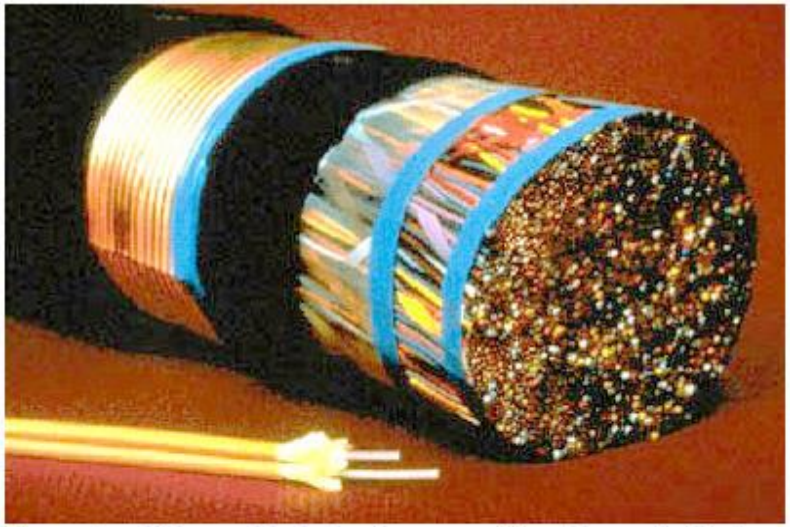


Optical vs. Copper

- By that time, the development of optoelectronics allowed to transmit the high-speed serial bit stream **optically**…

Duplex multimode optical cable with LC connector

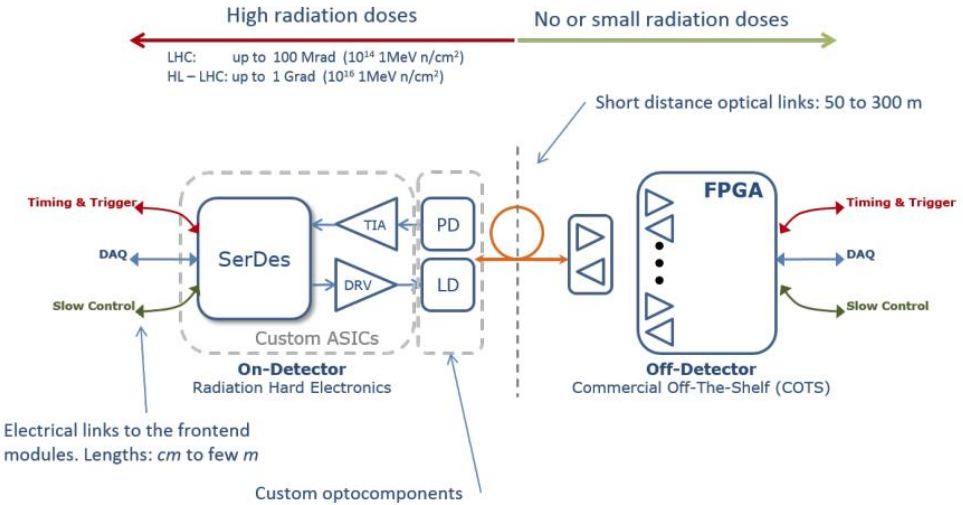
Transmitting 1 ~ 10 Gb/s bidirectionally



The optical fiber cable in the foreground has the equivalent capacity of the copper cable in the background.

GBT/lpGBT Overview

The arcitecture of a typical HEP link based on a *single* bidirectional optical link



This scheme is implemented by the CERN GBT link and its successor: the lpGBT

- **Back-end implmentation: Commercial components + lpGBT soft IP**
  (Optical transceivers, FPGA, lpGBT-FPGA FW code)
- **Fron-end implementation: Rad-hard lpGBT ASIC and Versatile Link Plus (VL+) optical components**
  (lpGBT ASIC, lpGBT/VL+ Laser Driver, and PIN Receiver, rad-hard optical cables and connectors)

lpGBT Main Fetaures

Radiaton hardness:

- Developed to whitstand HL-LHC radiation levels
- Radiation qualified commercial 65 nm CMOS technology and special layout techniques
- Robust line coding and error correction scheme (FEC5 or FEC12), capable of correcting single bit and bursts errors caused by SEUs and transmission errors

Downlink: deterministic latency

- clock and data (incl. trigger bits) can be delivered synchronously to all e-ports of the lpGBT ASIC on the FECs

Highly configurable features

- Can be a bidirectional transceiver, a simplex transmitter or a simplex receiver;
- Several front-end interface modes and options;
- Extensive features for precise timing control (a.k.a. „fast control”);
- Several features for experiment control and monitoring (a.k.a „slow control”);
- Robust operation against SEUs

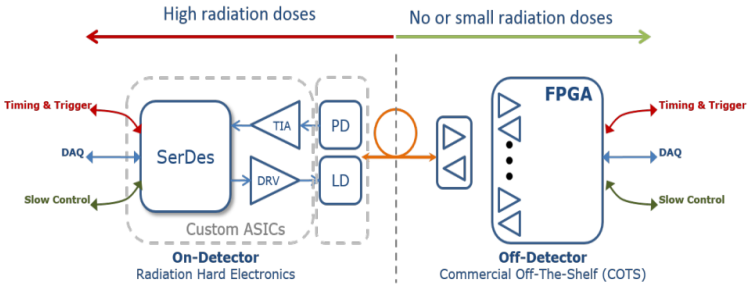
This scheme is provided by the CERN GBT link and its successor: the lpGBT

lpGBT Coming in ALICE…

- During the LS2 upgrade a brand new DAQ and trigger system had been developed for ALICE for Run 3 and Run 4
- The upgrading sub-detectors are now connected to the DAQ and Trigger systems with rad-hard **GBT links** through the CRU
- This enables the delivery of timing & control with deterministic latency and taking of data through a single fiber connection
- The GBTx ASIC is not available any more and the new lpGBT supersedes it for new developments or system additions

Main features of the present GBT links

- 4.8 Gb/s downlink
- 4.8 Gb/s uplink
- Front-end components:
  - GBTx ASIC
  - external slow-control (I2C, SPI, etc.) controller ASIC (SCA)
  - Versatile Link (VL) optical components
- Back-end components:
  - GBT-FPGA firmware code (IP) for FPGAs
  - Commercial optical transceivers

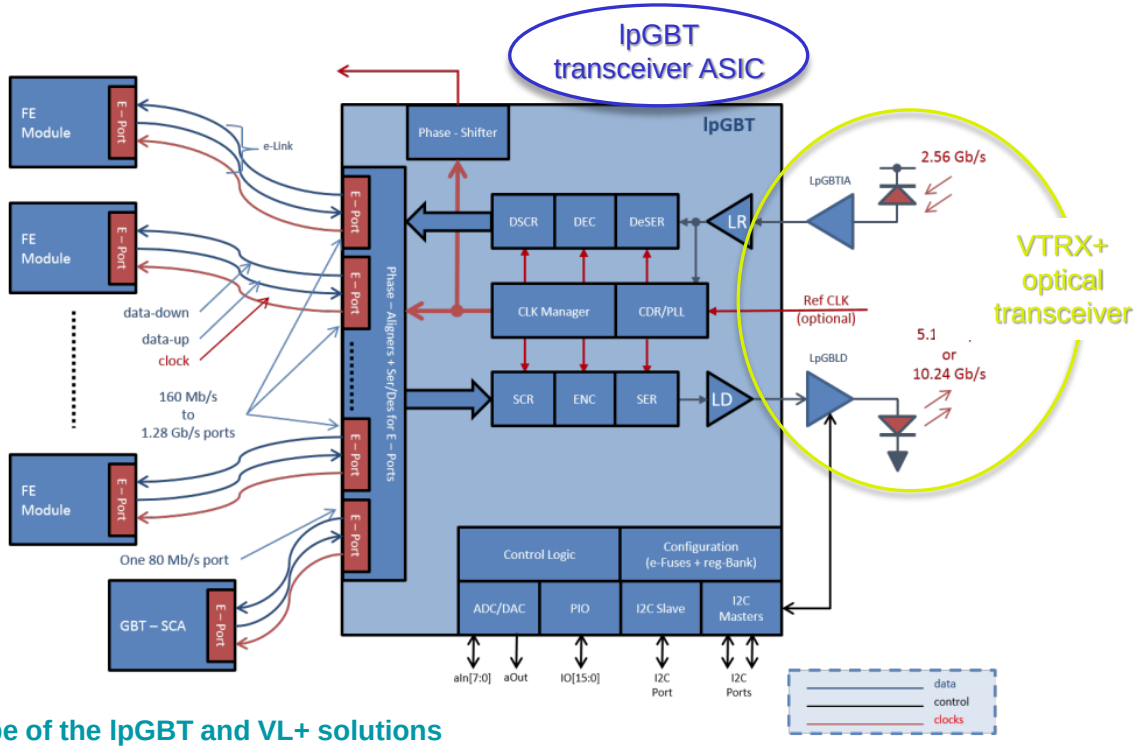


- During the coming LS3 upgrades, the new FE systems (e.g. ITS3, FoCal) will (have to) use lpGBT links to connect to the CRUs
- The lpGBT links have to be integrated into the existing CRU FW while keeping the compatibility with the existing O2, TRIGGER, and DCS systems

Main features of the new lpGBT with VTRX+

- 2.56 Gb/s downlink,
- 5.12/10.24 Gb/s uplink
- Front-end components:
  - lpGBT ASIC
  - internal slow-control controllers (I2C, SPI, GPIO, ADC, etc) (and optional external SCA)
  - VL+ optical components
- Back-end components:
  - lpGBT-FPGA firmware code (IP) for FPGAs
  - Compatible commercial transceivers (Samtec FireFly recommended for new developments)

lpGBT and VTRX+ Architecture



Time scope of the lpGBT and VL+ solutions

- **By now it is extended to Run 5 and Run 6. No new link type can be expected. (Silicon photonics integrated in FE ASICs will come, but not in this time frame...)**
- **Production is going on, and it is unclear if there will be later productions…**

lpGBT and VTRX+ Architecture

Optical link speeds

Uplink:

- 10.24 Gb/s
- 5.12 Gb/s

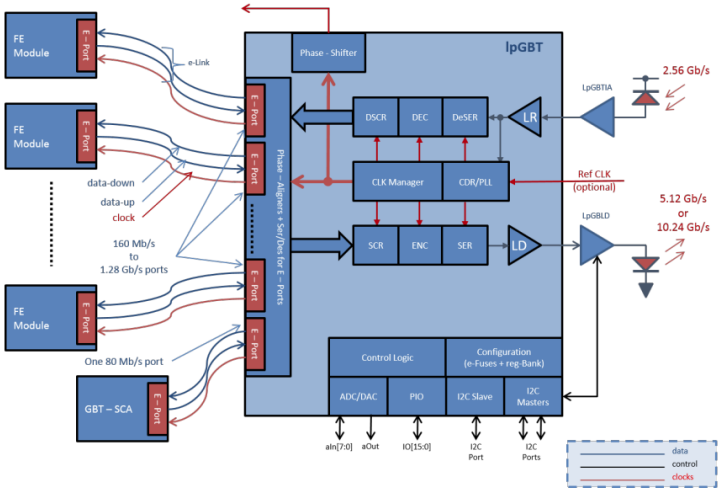
Downlink:

- 2.56 Gb/s, 64-bit frames

E-links:

Connections to the front-end ASICs are made through sets of local eLinks.

- Depending on the data rate and transmission media, e-links can extend up to a few meters.
- E-links use the CERN Low Power Signaling (CLPS), with programmable signal amplitudes to suit different application requirements
- The e-Links are driven by a series of *e-Ports* on the lpGBT and are associated with eLink ports in the front-end modules.
- The number of active eLinks and their data rates are programmable in groups of 4 e-links



Uplink	Useful data bandwith	
Link speed	FEC5	FEC12
5.12 Gb/s	4.48 Gb/s	3.84 Gb/s
10.24 Gb/s	8.96 Gb/s	7.68 Gb/s

lpGBT (Future, Run 4 and Run 5) vs. GBT (Present Run 3)

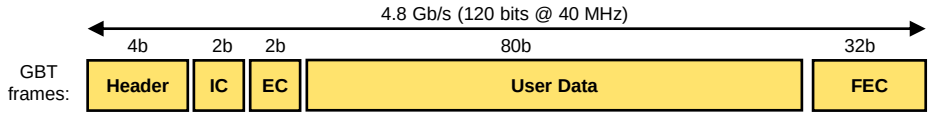
DOWNLINK

Header, internal and external control channels, data channel, forward error correction

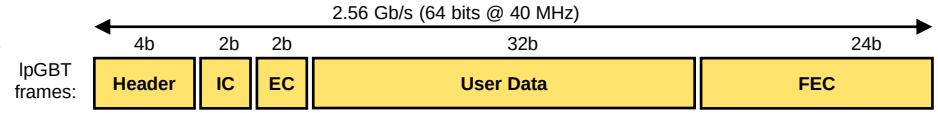
differences:

- 64-bit @ 40 MHz vs 120-bit @ 40 MHz
- 32-bit payload vs 80-bit bayload
- 2.56 Gb/s vs 4.8 Gb/s
- TX parallel clock 320 MHz vs 240 MHz

GBT downlink (CRU -> FEE)



lpGBT downlink (CRU -> FEE)



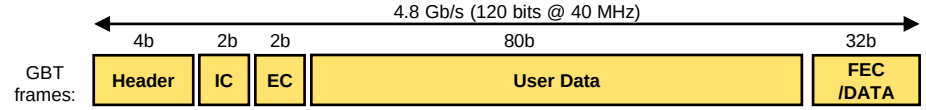
UPLINK

Header, internal and external control channels, data channel, optional forward error correction

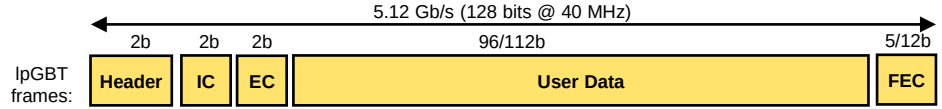
differences:

- 128/256-bit @ 40 MHz vs 120-bit @ 40 MHz
- 96/112/192/224-bit payload vs 80/112-bit payload
- 5.12 Gb/s or 10.24 Gb/s vs 4.8 Gb/s
- RX parallel clock 320 MHz vs 240 MHz

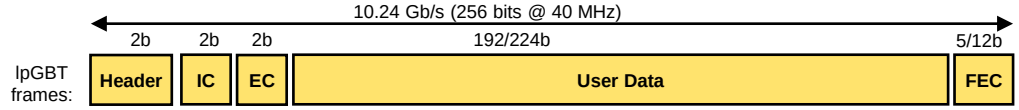
GBT uplink (FEE -> CRU)



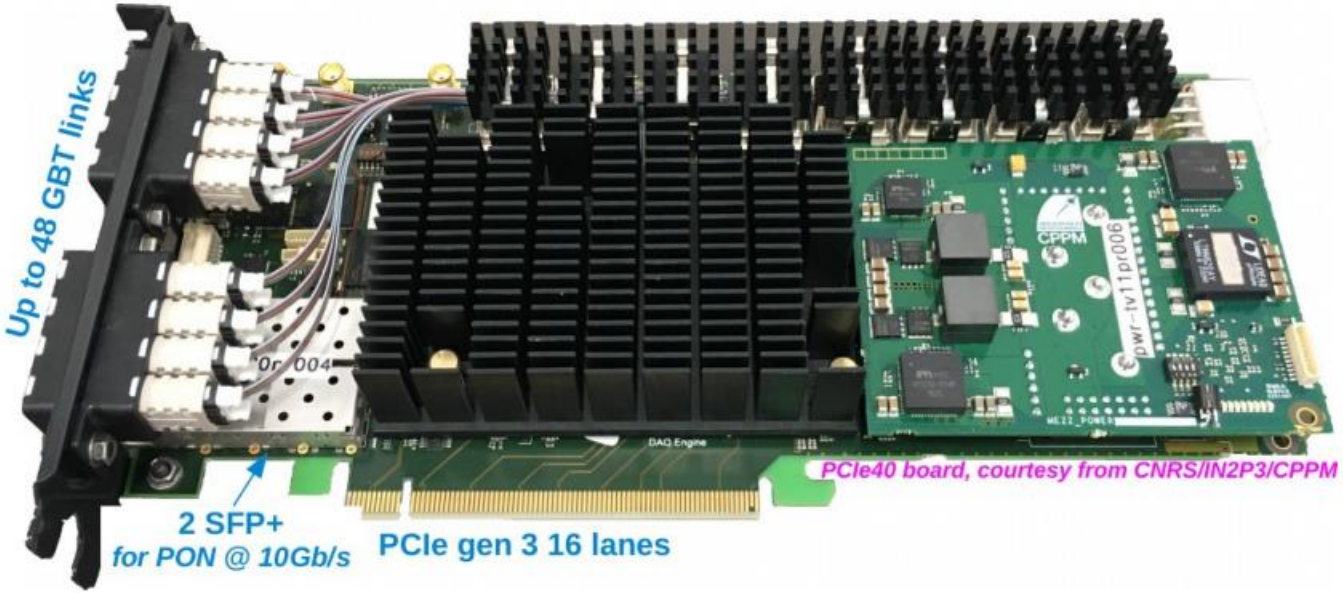
lpGBT uplink (FEE -> CRU)



lpGBT uplink (FEE -> CRU)



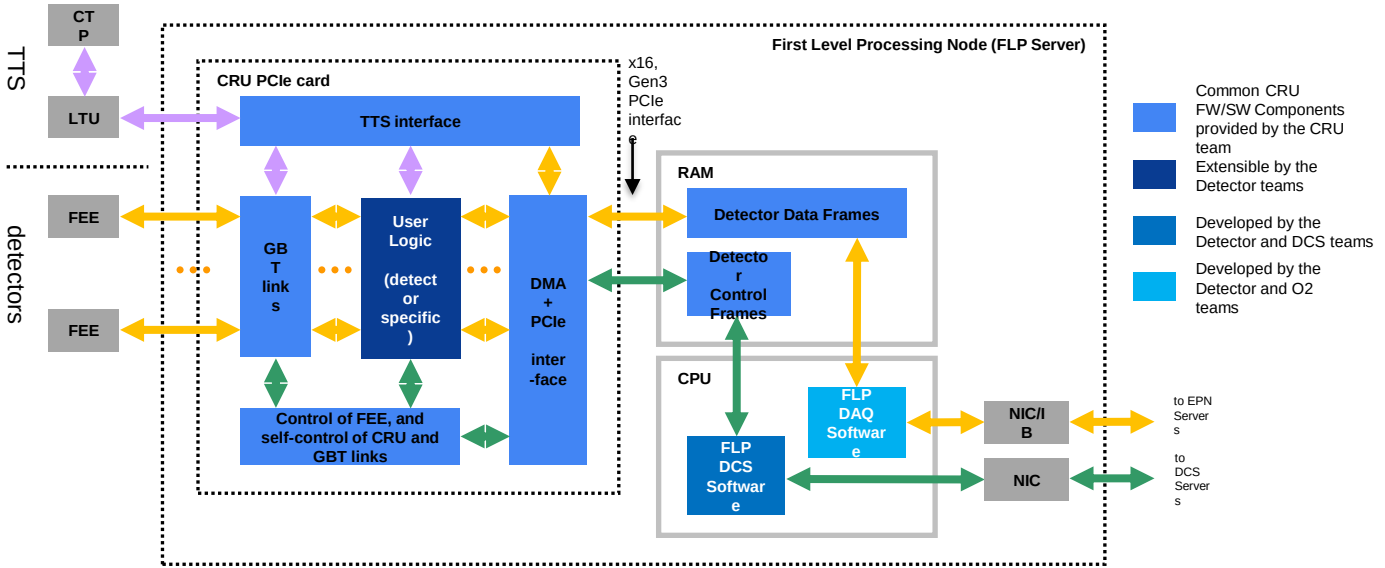
An lpGBT Back-end: ALICE Common Read-out Unit (CRU)



The Common Read-out Units (CRU) are PCIe add-on cards installed in the First Level Processor (FLP) nodes of the ALICE DAQ system. Main tasks of the CRU:

- **Deliver the trigger, timing and read-out control information to the Front-End Electronics**
- **Deliver detector data to the O2 (FLP Servers) with and/or without processing in the CRU FPGA**
- **Transport detector control information between the DCS and the FEE**
- **Take part of the Busy / Drop / Throttle mechanism of the detectors read-out**

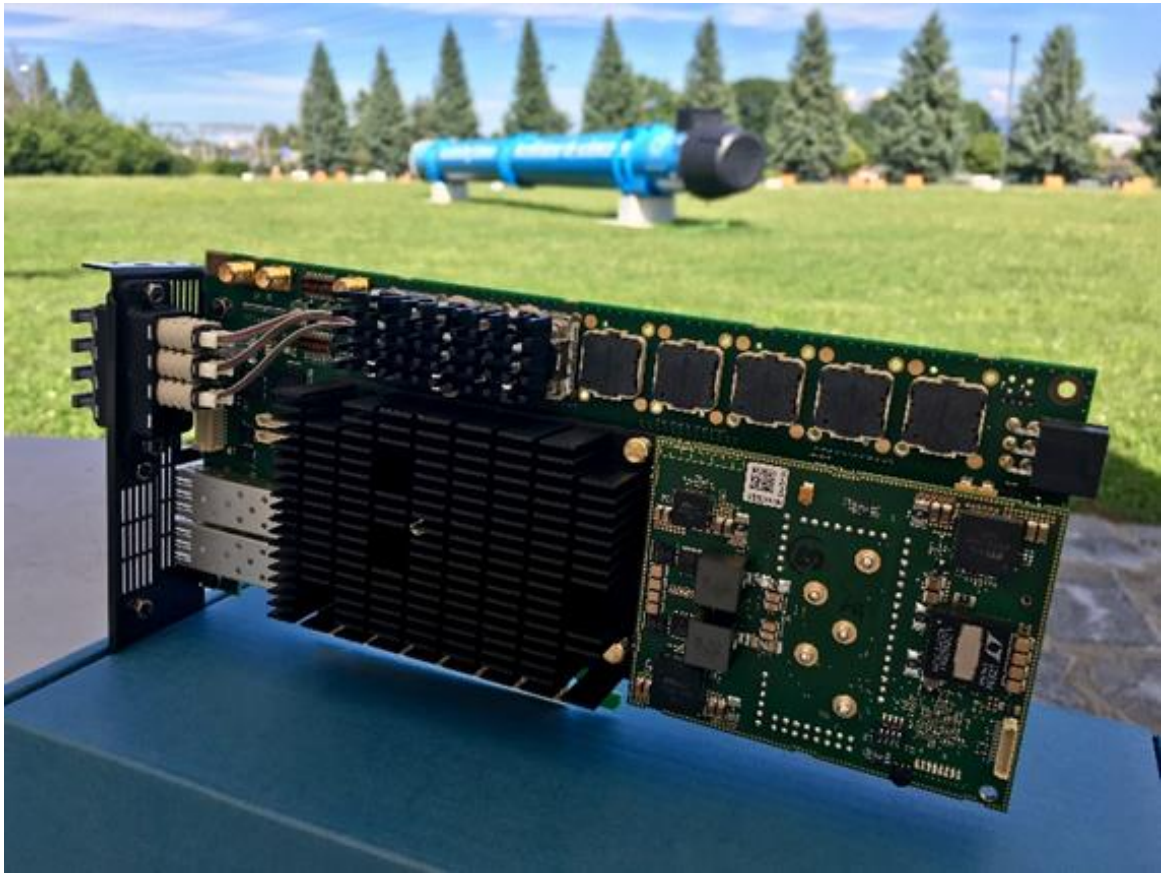
CRU Overview



Main Tasks of the CRU:

- Deliver the trigger, timing and read-out control information to the Front-End Electronics
- Deliver detector data to the O2 (FLP Servers) with and/or without processing in the CRU FPGA
- Transport detector control information between between the FLP Servers (DCS) and the FEE
- Take part of the Busy / Drop / Throttle mechanism of the detectors read-out

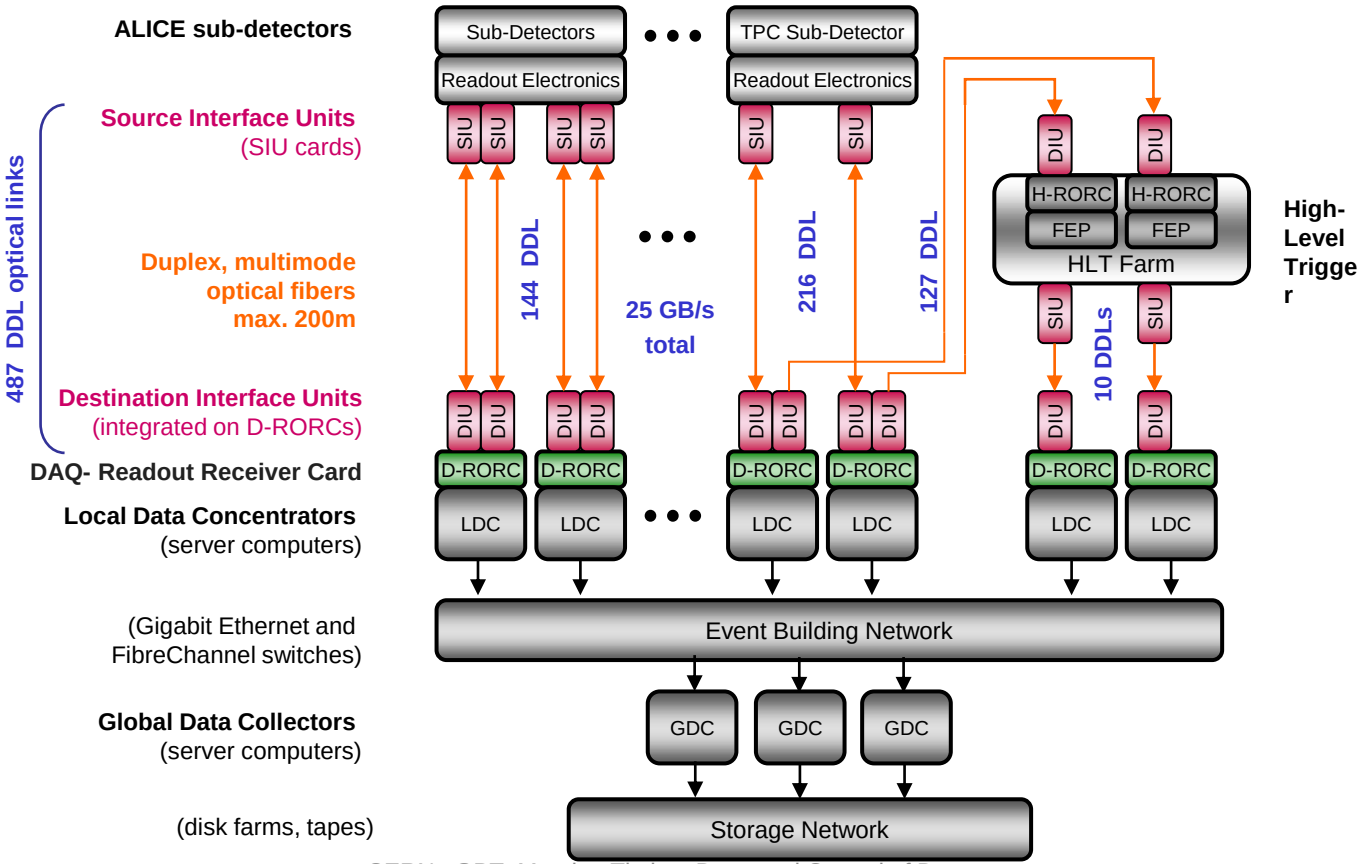
Thank you for the attention!



Back-up slides

BACK-UP

DDL in the ALICE DAQ System



CRUs in ALICE Read-out