Science and Technology Facilities Council

DRD7

Questions:

What the key technologies will be?
What the state of formation of the international collaboration is?
Who is involved from the UK?
What the priority projects are (areas we'd like to bid for funds for) and what future experiments they will support….

Marcus French
Detector & Electronics Division
UKRI STFC, RAL

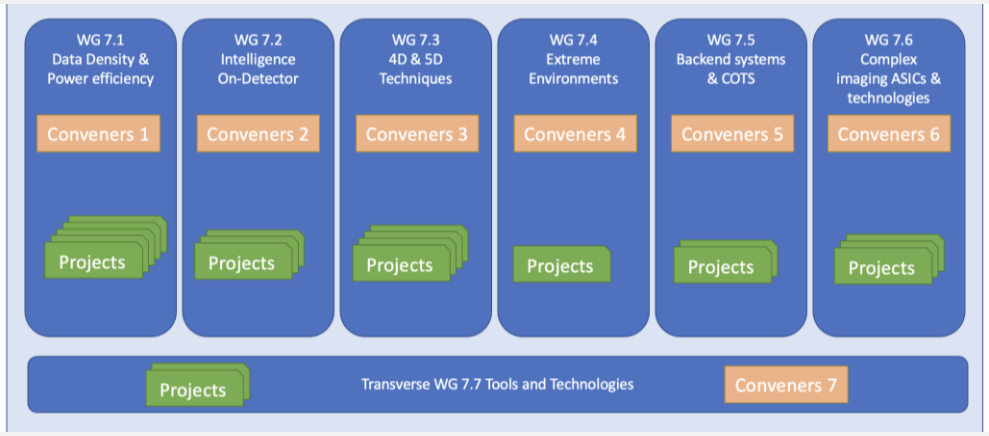
Also member of DRD7 Steering Committee

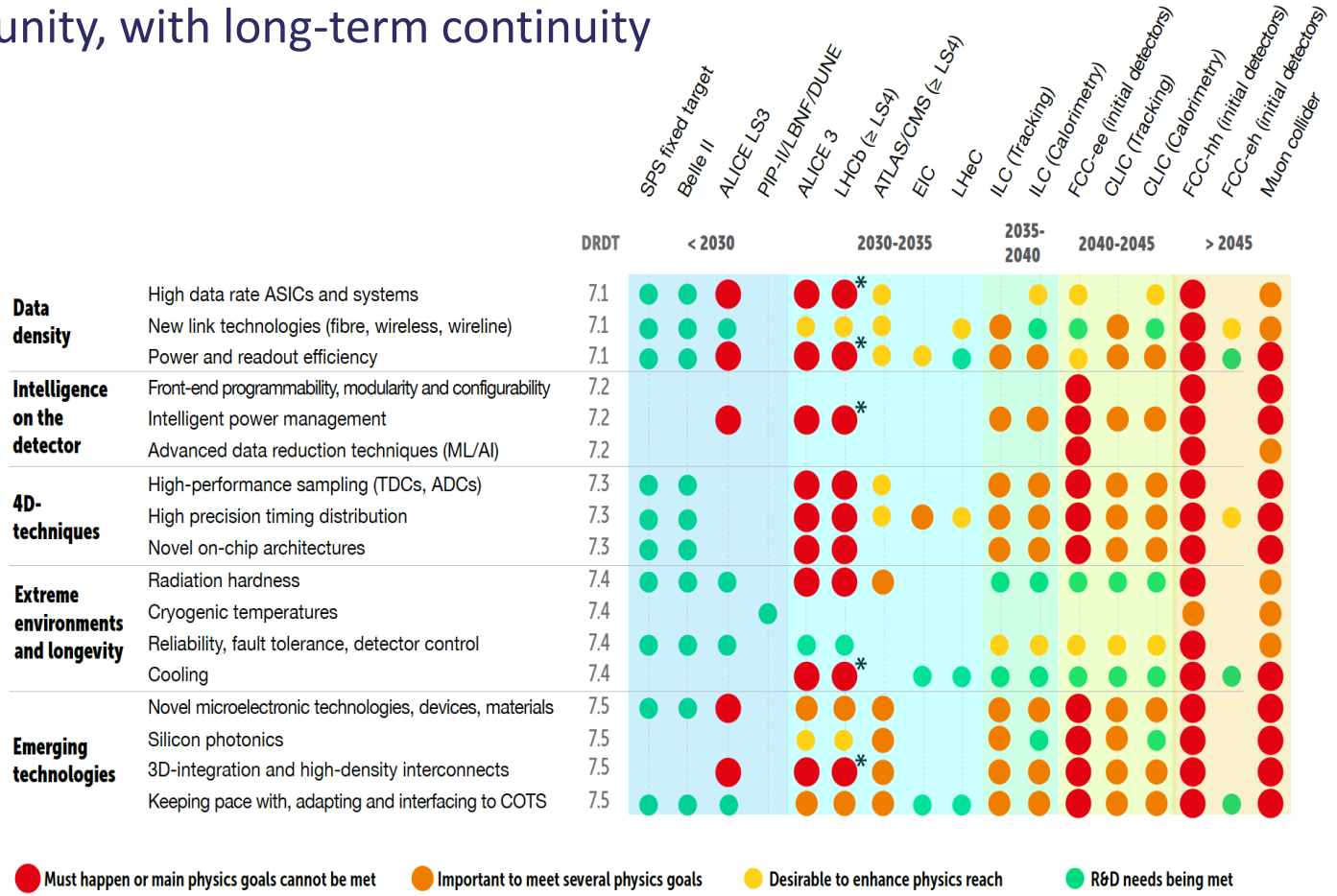
DRD7 – A reminder of the key objectives

Advance the state-of-the-art in performance of electronics and data processing
Improve and develop further common standards, methodologies, and IP
Build expertise, increase efficiency and decrease duplication of effort
Provide facilities and tools for R&D in the community, with long-term continuity

DRDT 7.1 Advance technologies to deal with greatly increased data density
DRDT 7.2 Develop technologies for increased intelligence on the detector
DRDT 7.3 Develop technologies in support of 4D- and 5D-techniques
DRDT 7.4 Develop novel technologies to cope with extreme environments and required longevity
DRDT 7.5 Evaluate and adapt to emerging electronics and data processing technologies

implementation proposal





DRD7 – Status and key dates

- **Step 1a (Mar – Jun 2023):** convenors
  - seeks expressions of interest in specific projects
  - defines few initial priority projects with rel… …stantial community interest
- **Step 1b (Mar – Jul 2023):** technical committee
  - defines common p… …other DRDs
  - avoids duplic… …rk
  - set DRD… …to other DRDs plans
- **Step 2 (July – Aug 2023)**: Letter of Intent
  - submit to the …
  - with sco… …ganisation + list of researchers and institutes
- **Step 3 (Sep – Oct 2023):** second DRD7 workshop
  - …tailed proposals for the initial projects
  - …cuss areas of common interest.
  - …pen to both LoI signatories and other institutes seeking to join the effort
- **Step 4a (Sep – Nov 2023):** initial set of proje…
  - take account of feedback from the DRDC
  - planned and costed in detail
- **Step 4b (Sep – Nov 2023):** natio…
  - discuss with national funding agencies
  - define likely participation and resource envelope for the initial projects
- **Step 5 (Dec 2023):** DR… …roposal
  - submit to the DRDC
  - includes resource-loaded plans for the initial projects
- **Step 6 (2024 on):** Projects …art in national communities
  - take into account feedback from the DRDC,
  - make proposals to their funding agencies
  - start projects as resources are allocated

=> from 2024 onwards: annual DRD7 workshops

What I showed last time

DRD7 – Status and key dates

- **Step 1a (Mar – Jun 2023):** convenors
- **Step 1b (Mar – Jul 2023):** technical committee
- **Step 2 (July – Aug 2023)**: Letter of Intent
- **Step 3 (Sep – Oct 2023):** second DRD7 worksho
- **Step 4a (Sep – Nov 2023):** initial set
- **Step 4b (Sep – Nov 2023)** ommunities
- **Step 5 (Dec 2023):** DRD7 Collaboration Proposal **(Feb 2024)**
- **Step 6 (2024 on):** Projects start in national communities

Submitted to DRDC in late Feb 2024

- Currently under review with some informal feedback so far

- Will discuss with Thomas Bergauer planned for early May

- Next annual workshop planned for September 9th -10th at CERN

DRD 7: Proposal for an R&D Collaboration on: Electronics and On-Detector Processing

The DRD7 Collaboration

February 29, 2024

Jerome Baudot[1], Marcus French[2], Ruud Kluit[3], Angelo Rivetti[4], Frank Simon[5,*], Francois Vasey[6,*]
(**DRD7 Steering Committee**)

Marlon Barbero[7], Sophie Baron[6], Giulio Borghello[6], Michele Caselle[5], Davide Ceresa[6], Francesco Crescioli[8], Manuel Da Rocha Rolo[4], Oscar Augusto De Aguiar Francisco[9], Conor Fitzpatrick[9], Marek Idzik[10], Kostas Kloukinas[6], Szymon Kulis[6], Xavi Llopart Cudie[6], Niko Neufeld[6], Jeffrey Prinzie[11], Iain Sedgwick[2], Walter Snoeys[6], Jan Troska[6], Mark Willoughby[2]
(**DRD7 Working Group Conveners**)

* Co-chairs of the Steering Committee
[1]Université de Strasbourg, CNRS, IPHC, Strasbourg, France
[2]UKRI-STFC RAL, Chilton, Didcot, Oxfordshire, UK
[3]NIKHEF, Amsterdam, Netherlands
[4]INFN, Torino, Italy
[5]Karlsruhe Institute of Technology, Karlsruhe, Germany
[6]CERN, Geneva, Switzerland
[7]CPPM, Aix-Marseille Université, CNRS/IN2P3, France
[8]Université Paris Cité, CNRS, LPNHE, Paris, France
[9]University of Manchester, Manchester, UK
[10]AGH University, Krakow, Poland
[11]Katholieke Universiteit, Leuven, Belgium

Contents

1

- includes resource-loaded plans for the initial projects

- take into account feedback from the DRDC,
- make proposals to their funding agencies
- start projects as resources are allocated

=> from 2024 onwards: annual DRD7 workshops

DRD7 – A broad range of technology

DRD7:
A broad range of topics in electronics

WG 7.1: Data density and power efficiency

Szymon Kulis (CERN), Jeffrey Prinzie (KU Leuven), Jan Troska (CERN)

- High data-rate ASICs and systems
- New link technologies, including silicon photonics technology
- Power conversion and efficiency optimisation

WG 7.2: Intelligence on the detector

Davide Ceresa (CERN), Francesco Crescioli (IN2P3-LPNHE), Frédéric Magniette (IN2P3-LLR)

- Front-end programmability and modular design
- Intelligent power management
- Advanced data reduction techniques

WG 7.3: 4D and 5D techniques

Sophie Baron (CERN), Marek Idzik (AGH-Kracow), Adriano Lai (INFN-Cagliari)

- High-performance sampling
- High-precision timing distribution
- Novel on-chip architectures

WG 7.4: Extreme environments

Giulio Borghello (CERN), Oscar Francisco (Uni-Manchester), Manuel Rolo (INFN-Torino)

- Cryogenic technology and operation
- Thermal management of ASICs
- Radiation hardness

WG 7.5: Backend systems and COTS

Conor Fitzpatrick (Uni Manchester), Niko Neufeld (CERN), NN

- Use and adaptation of advanced COTS technologies
- Real-time software and firmware development
- System-level control and readout

WG 7.6: Complex imaging ASICs and technologies

Marlon Barbero (IN2P3-CPPM), Michele Caselle (KIT), Iain Sedgwick (RAL), Walter Snoeys (CERN)

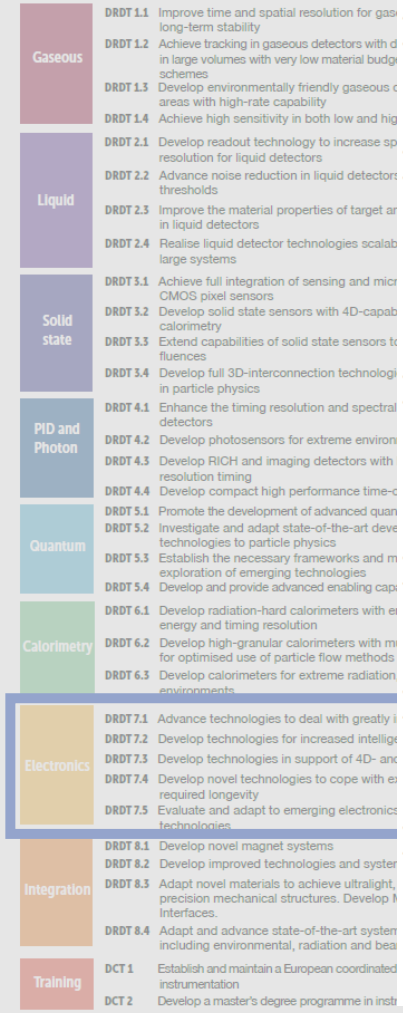
- Common access framework to selected imaging technologies
- Common IP for imaging ASICs
- 3D integration and interconnects

WG 7.7: Tools and technologies

Kostas Kloukinas (CERN), Xavi Llopart (CERN), Mark Willoughby (RAL)

- Access and support to qualified technologies and tools
- Investigation of emerging microelectronics technologies
- Support and training for device and systems development and verification
- Common IP and design reuse

DRD7 – A br



power efficiency
zie (KU Leuven), Jan Troska (CERN)
stems
ding silicon photonics technology
ency optimisation

e detector
Crescioli (IN2P3-LPNHE), Frédéric Magniette

and modular design
ent
chniques

ques
(AGH-Kracow), Adriano Lai (INFN-Cagliari)

bution

nents
ancisco (Uni-Manchester), Manuel Rolo (INFN-

peration
ICs

and COTS
r), Niko Neufeld (CERN), NN
nced COTS technologies
ware development
adout

ASICs and technologies
lichele Caselle (KIT), Iain Sedgwick (RAL), Walter

to selected imaging technologies
Cs
nects

logies
part (CERN), Mark Willoughby (RAL)
fied technologies and tools
icroelectronics technologies
vice and systems development and verification
e

DRD7 – UK involvement

Overall - 20 Staff Years out of 118 (so 17%)

Average of ~6.5 per year including academia and NL

Country	Institute	Email address	1			1 Total	2		2 Total	3			3 Total	4			4 Total	5		5 Total	6		6 Total	Grand Total
			WG7.1.a	WG7.1.b	WG7.1.c		WG7.2.b	WG7.2.c		WG7.3.a	WG7.3.b1	WG7.3.b2		WG7.4.a	WG7.4.b	WG7.4.c		WG7.5.a	WG7.5.b		WG7.6.a	WG7.6.b		
UK	Imperial College	g.iles@imperial.ac.uk	1			1													1	1				2
	Queen Mary University of London (QMUL)	m.bona@qmul.ac.uk																1		1				1
	UKRI-STFC Rutherford Appleton Laboratory (RAL)	mark.pryderch@stfc.ac.uk					1		1									1	1	2	1		1	4
	University College London (UCL)	a.kam@ucl.ac.uk																1		1				1
	University of Birmingham	S.J.Hillier@bham.ac.uk	1			1												1		1				2
	University of Bristol	David.Cussans@Bristol.ac.uk					1		1			1	1					1	1	2				4
	University of London Royal Holloway	veronique.boisvert@rhul.ac.uk					1		1					1			1							2
	University of Manchester	conor.fitzpatrick@cern.ch														1	1	1		1				2
	University of Oxford; Rutherford Appleton Laboratory	prof.jocelyn.monroe@gmail.com												1			1							1
	University of Warwick	karolos.potamianos@cern.ch					1		1															1
UK Total			2			2	4		4			1	1	2		1	3	6	3	9	1		1	20
Grand Total			14	8	8	30	8	2	10	9	3	10	22	10	5	9	24	10	7	17	10	5	15	118

Science and Technology Facilities Council

Note these numbers do not include any UK Hub activity!

DRD7 – WP7

Hub based structure:

- Enable the successful use of advanced CMOS and EDA by the community

- Ensure professional standards of design and verification

- Facilitate collaboration and IP sharing between institutes

- Establishing this year, so we need to know UK requirements

Science and Technology Facilities Council

B.7 Working Group 7.7: Tools and Technologies

In response to the DRD7 projects detailed above and those related to electronics in other DRDs, and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a task force that will propose an implementation solution for a hub-based structure for ASICs developments.

B.7.1 A Hub-based structure

A few central ASIC development centres defined as 'Hubs' will be established with CERN as the lead focus. On behalf of the DRD7 Collaboration, these Hub centres will be available to support best practice design of a selection of large and complex DRD sponsored ASIC projects within their region.

The overall goal of this Hub-based structure is to:

- Establish and maintain access, for the community at large, to state-of-the art microelectronics technologies and EDA software tools through regional collaboration and coordination
- Ensure a professional approach to prototyping and production fabrication cycles by delivering best practice in design, verification and foundry submission,
- Facilitate collaborative work across distributed design teams establishing the necessary infrastructure for IP block sharing, and
- Follow rigorous project review and submission processes to manage risks and control changes in projects

The Hub institutes will collaborate with their wider region's design groups to deliver a wide programme of sophisticated, complex or large size DRD-sponsored ASICs. They will contribute by ensuring thorough planning, review and design validation in all design fabrication cycles. Then, working with CERN and other Hubs, they will plan and coordinate foundry access for these projects over their lifetime.

In addition, the Hub institutes will collectively:

- Provide access to necessary technical support for projects to ensure rigorous completion of all design validation and foundry design rules checks. Maintain signoff checklists, foundry submission check lists and 'lessons learned' logs to support each other and build best practice
- Coordinate fabrication manufacturing runs and IP library access in partnership with supported foundries, CERN ASIC support and Foundry Services and Europractice
- Maintain a master list of all current projects to enhance global overview and forecast foundry access, and
- Provide advice in ensuring that projects are correctly resourced for the anticipated goals

Locally, in their region, Hub institutes will also:

- Lead the preparation and management of IP sharing agreements that meet the needs of their region
- Ensure that the strict end-use rules, export controls and taxation issues in each region are recognised, understood and met by their community, and
- Engage with their local funding agencies to ensure that support and submission management costs are planned for and included in projects.

The overall objective of the above is to support the wider community so that everyone can continue to contribute and innovate new electronic systems in the knowledge that with their Hub partner they will be able to implement successful ASIC production solutions for their experiments, when needed by the experimental programme. The best way to achieve this objective at project-level is to include from the beginning a Hub institute in all the most complex and risky DRD-sponsored ASIC projects.

B.7.2 Hub roles and requirements

Hub centres will be expected to be equipped and have all the resources and skills necessary to develop and submit full-scale ASICs to supported foundry(ies), making best use of state-of-the-art practices and tools. In addition, they must demonstrate their ability to support a reasonable number of community projects in their region. Practically, Hubs are expected to be large established institutions or national laboratories. Hubs might adopt an infrastructure setup resembling the CERN ASIC support and Foundry service model. This would involve personnel working on design projects and providing support services as necessary.

As members of the DRD7 collaboration, Hubs will participate in Working Group WG7.7 (tools and technologies). They will collectively maintain their expertise through appropriate training, collaboration with industry and engagement in ASIC design projects. They will, wherever necessary, develop "common design platforms" incorporating design kits, IP libraries and design flows and provide long-term maintenance, technical support and training. Funding of Hub support will be achieved directly via centralised national channels, or indirectly via the projects requesting support.

The list of Hub institutes will be agreed and reviewed periodically by the DRD7 collaboration.

In their preparation for complex projects, the community will be invited to discuss and agree the level of Hub involvement required with their regional Hub centre. This could range from active design and/or verification work to just engagement with design reviews.

The DRDC may, based on expert reviews, recommend that a Hub institute is added to the list of project participants, in case it judges that the design is too challenging for the project team as is.

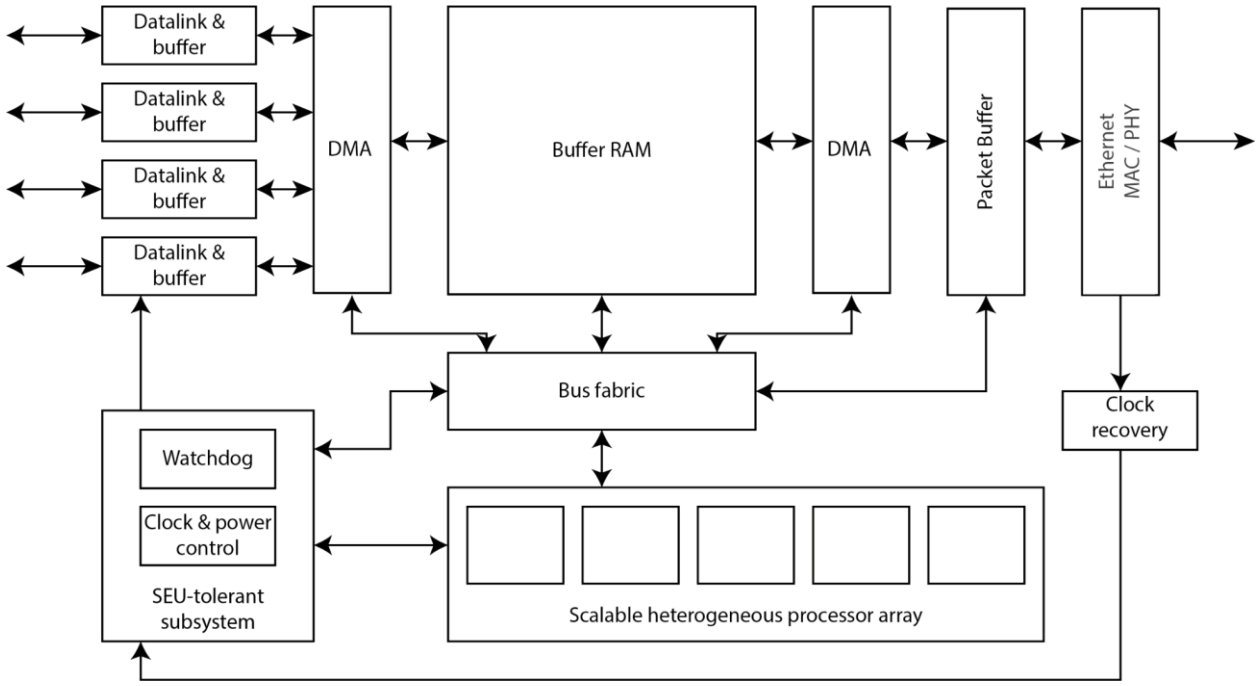
CERN, as lead focus, will coordinate the overall structure and undertake central roles including:

- Negotiating legal and commercial aspects for accessing new technologies on behalf of the community
- Maintaining a list of Institutes eligible to collaborate on NDA protected technologies
- Providing technical support and training to Hub Institutes
- Working with Hub institutes to develop "common design platforms" and to facilitate maintenance, technical support, training and collaboration, and
- Assisting in supporting the wider community when circumstances prevent a regional Hub from doing so

B.7.3 Timeline

The timeline for the taskforce to propose an implementation solution to the Hub-based model sketched above is 12 months. The proposal will identify the hub institutes and their interactions, the supported technologies and target projects, and will propose a roadmap for presenting, discussing and rolling out the new structure for the DRD community.

DRD7 Case study – Vision of a common interfacing ASIC components



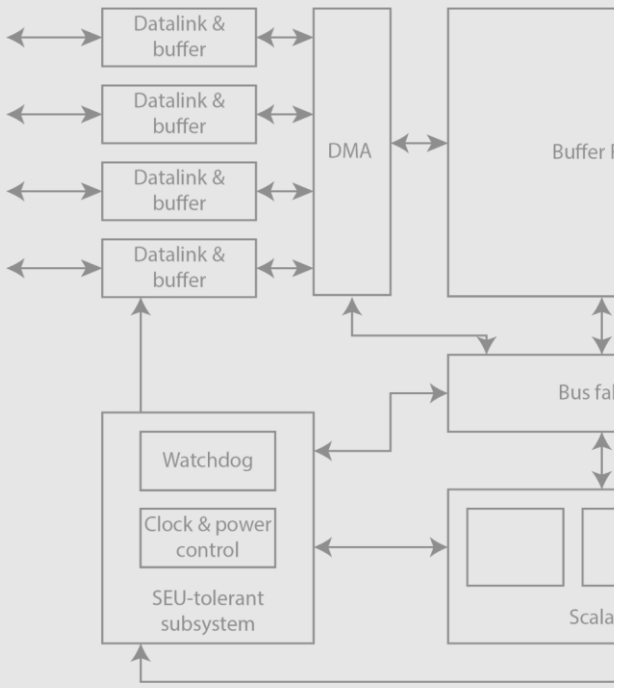
Proposed common interface ASIC for detector readout, timing, & control

Our goal is to develop and demonstrate specialised FE ASICs to a common industry-standard off-detector interface in rad hard 28nm

- STFC TD involvement across both DRD7 and DRD3 activities
- More funding will be needed downstream for a serious level of commitment
- Early work will help define link specifications and protocols
- ASIC emulation in FPGA using RISC-V/SoC open-source solutions
- Study & design of IPs necessary for 10 / 25 / 100Gb Ethernet cores

Science and Technology Facilities Council

DRD7 – Vision



Proposed common interface AS
& co

6.1 Project 7.2.b

The project aims to develop a radiation-hardened System-On-Chip (SoC) based on the RISC-V ISA standard.

Project Name	Radiation Tolerant RISC-V System-On-Chip (WG7.2.b)
Project Description	Develop a radiation-hardened SoC based on the RISC-V ISA standard according to the roadmap defined in M7.2b.1. Topics: 1- SoC architectures 2- Radiation Tolerance design methodology, 3- Verification methodology, 4- SoC generator toolchain. Duration 5-6 years.
Innovative/strategic vision	Develop a technology and a design platform to anticipate and adapt the challenges and opportunities of the future Electronic systems and IC design.
Performance Target	The following targets will be defined in M7.2b.2: Processing Speed Power Consumption Radiation Tolerance Memory and Storage Communication Interfaces Scalability and Flexibility Verification and Testing
Milestones and Deliverables	M7.2b.1 - Rad-Tol RISC-V SoC roadmap (12M) M7.2b.2 - SoC architectures proposal (24M) D7.2b.3 - Rad-Tol SoC building block test chip (36M)
Multi-disciplinary, cross-WG content	Electronics Engineering - Digital Design Computer Science - Embedded Systems Systems Engineering - Integration and Testing
Contributors	DE: FH Dortmund BE: KU Leuven CERN UK: UKRI-STFC RAL UK: Royal Holloway University Of London UK: University of Warwick UK: University of Bristol US: Fermilab
Available resources - 2024-26 -	6.15 FTE/year 40 kEUR/year
Resource request - 2024-26 -	7.9 FTE/year 21.7 kEUR/year

e of specialised FE ASICs to a
ndard off-detector interface.

tudy to STFC

l Grant Submission -- Feb 2024

requested for TD involvement
7 and DRD3 activities

ll be needed for a serious level

specifications and protocols.

n FPGA using RISC-V/SoC open-

f IPs necessary for 10 / 25 /
cores.

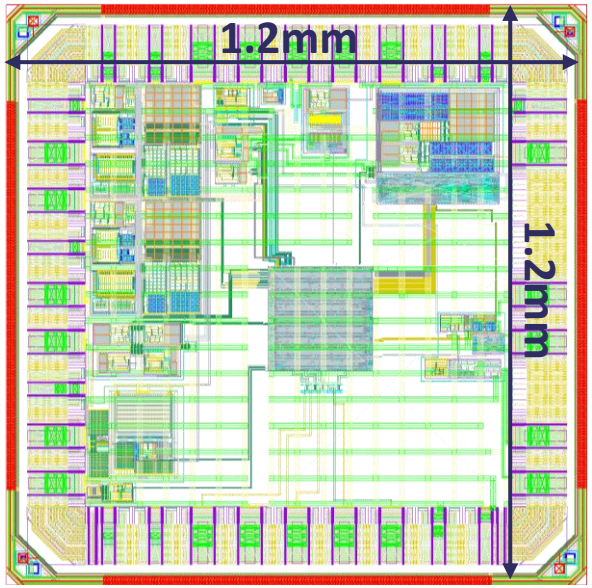
Science and Technology Facilities Council

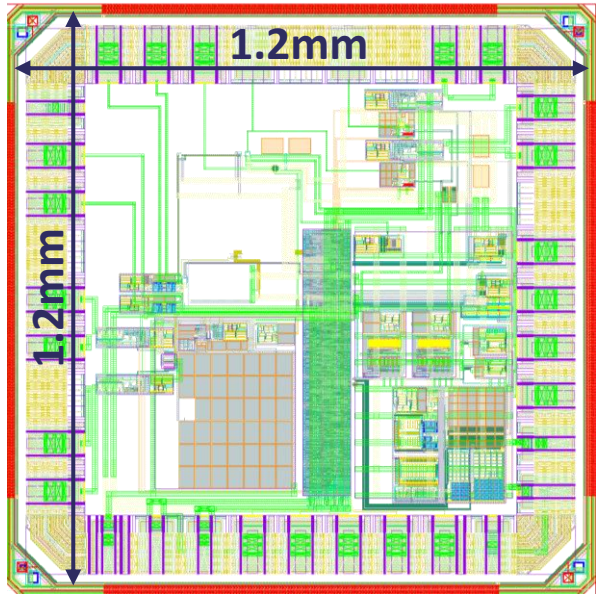
University of BRISTOL

DRD7 – Background 28nm design experience at RAL

- Funded 3-year programme (2024/25 final year)
- 2 Test-structure ASICs submitted 25th October 2023 including:
  - Rail-to-Rail Amplifiers - PMOS & NMOS Reference Drivers
  - Beta-Multiplier & Voltage Bandgap
  - 10-bit IDAC & 10-bit VDAC
  - SLVS Clock Receiver, CML Output Driver & 2.4GHz PLL
  - Triplicated high-speed digital circuitry
  - Low-jitter LGAD Front-end
  - Vernier Delay Line TDC building blocks

PURNIX →





←YELNIX

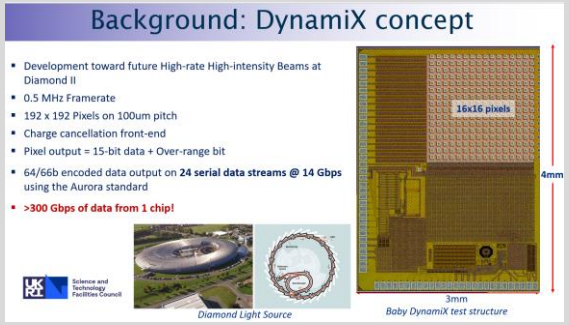
Science and Technology Facilities Council

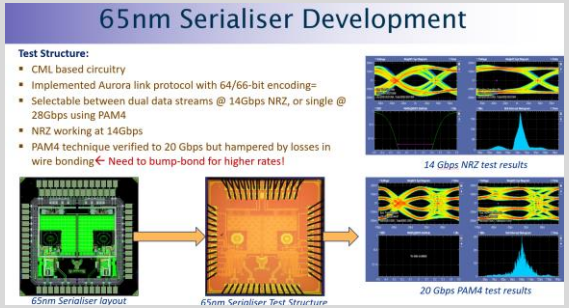
DRD7 – Current priorities for RAL TD this FY

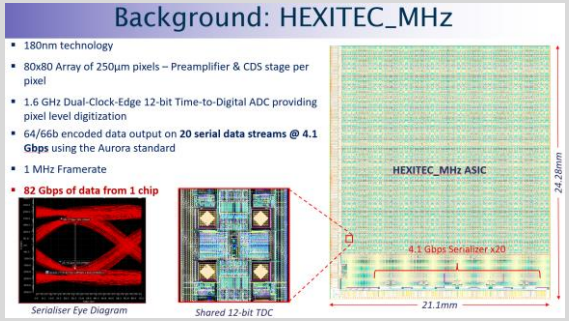
- Testing and irradiation of 28nm IP (with help from Birmingham & Oxford Uni.)
- Consider Ethernet requirements, in particular the Physical Layer & identify required IP for development (What IP already exists in the community?)
- Develop targeted IP for 25Gb Ethernet for new 28nm test structure towards start of 2025
- Need to establish the UK Hub and ensure the UK needs are fully represented

Science and Technology Facilities Council

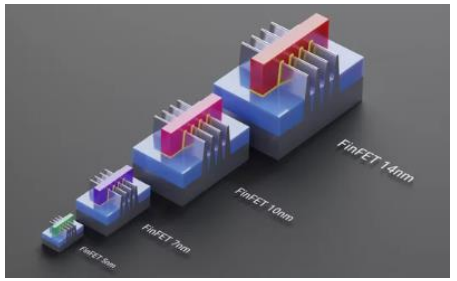
Other recent work:







DRD7 – Summary, overall purpose and activities



Purpose

- Advance the state-of-the-art in **performance and deliverability** of detector **electronics and data processing**
- Build **expertise**, improve and develop further **common standards, methodologies**, and **IP** for implementation of electronic and data processing systems
- Increase efficiency and **decrease duplication** of effort in detector electronics development
- Provide **facilities and tools for R&D in the community**, with long-term continuity.

Activities

- Oversee, drive and coordinate **strategic R&D** in electronics for particle physics
- Support and maintain an active and well connected **R&D community**
- Promote and maintain a **connection between the developers and users** of future electronic systems
- Coordinate **cross-European access** to technologies, tools, and knowledge
- **Interface with other DRDs** in areas of common interest, **undertaking joint projects**

Science and Technology Facilities Council

Thank you

Facebook: Science and Technology Facilities Council

Twitter: @STFC_matters

YouTube: Science and Technology Facilities Council