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U.S. DEPARTMENT OF ENERGY

CHARMS250: A Cryogenic Front-End ASIC for Low-Noise Readout of Light or Charge Signals

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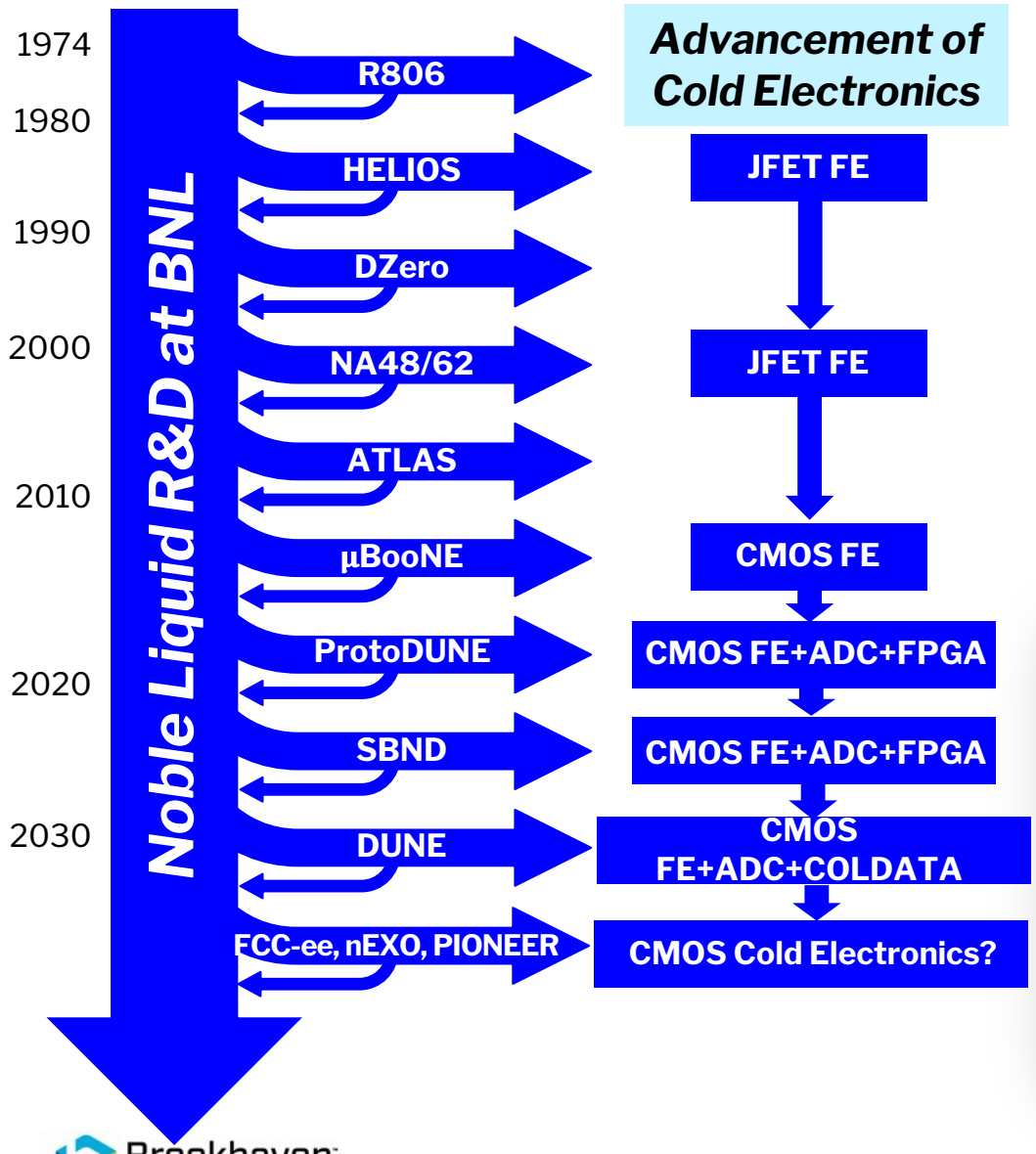
Long History of Noble Liquid Detector R&D at BNL



- BNL pioneered Liquid Argon based detector technology in 1974
  - ***Unique experience in cryogenic electronics and low-noise microelectronics***
  - ***Strong collaboration between Physics and Instrumentation Departments at BNL for half a century***
- R&D → Experiments → R&D
  - ***Readout electronics*** has always been an ***integral*** part of detector R&D effort for ***precision measurement*** with noble liquid detector

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LIQUID-ARGON IONIZATION CHAMBERS AS TOTAL-ABSORPTION DETECTORS*

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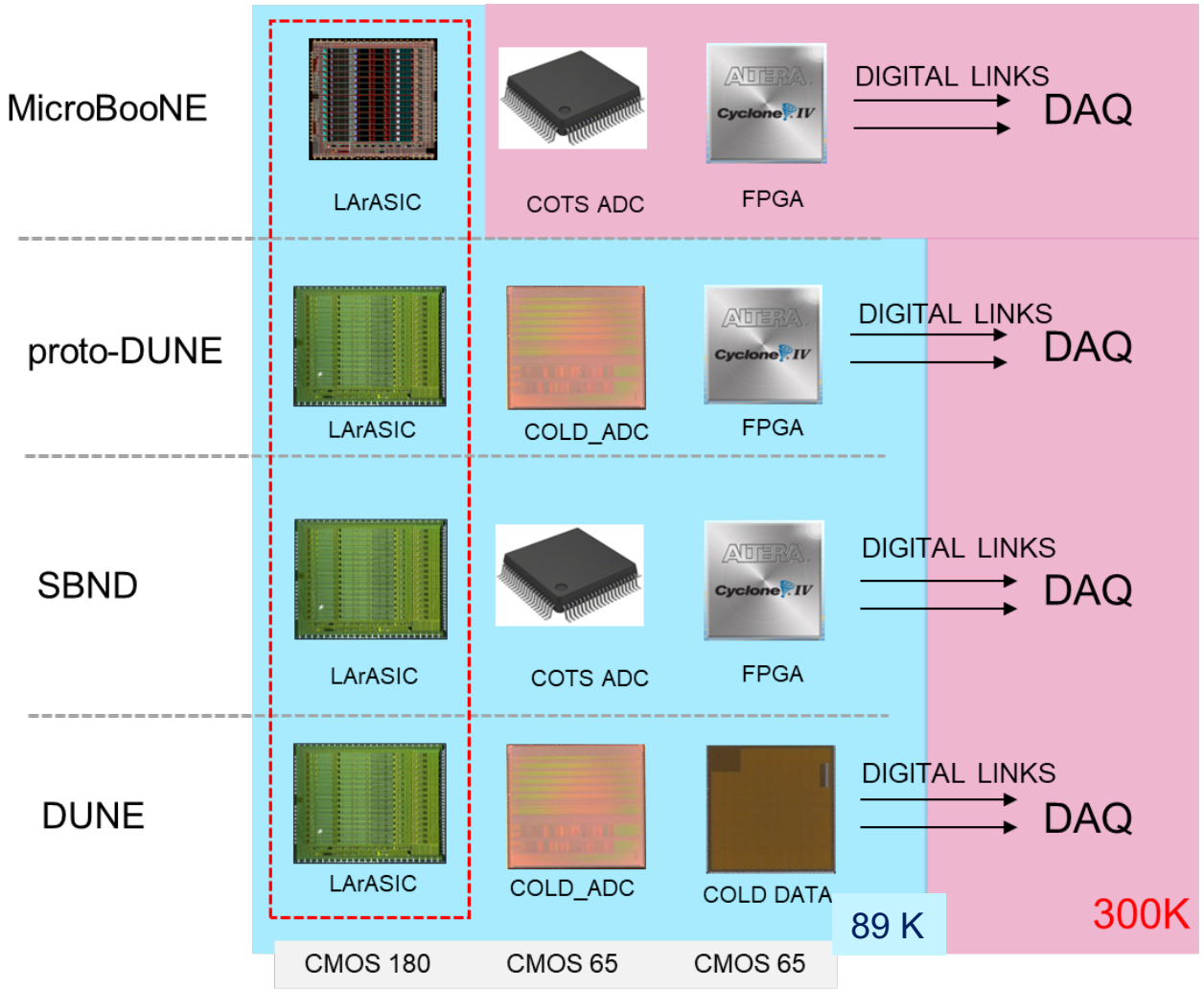
Status of Cryogenic Front-end ASICs



3 ASICs vs. 1 ASIC solution:

- Initially two readout options were proposed:
  - 3 ASICs vs. 1 ASIC
    (idea of building 1 ASIC, combining FE/ADC/transmission brought in 2016 and included as parallel path of development)
- Evolutionary development MiCroBooNE→ DUNE led to the 3 ASIC solution that:
  - Helped perfect the FE (through multiple iterations)
  - Allowed debugging (procedure for ADC calibration)
  - Allowed independent optimization of each chip
  - Disallowed analog – digital interfaces

Currently in development: CHARMS250 (CHARge aMplifer + Shaper -> 65 nm cryogenic analog front-end ASIC with 250 ns shortest peaking time)

CHARMS10 with 10 ns shortest peaking time also planned for future development

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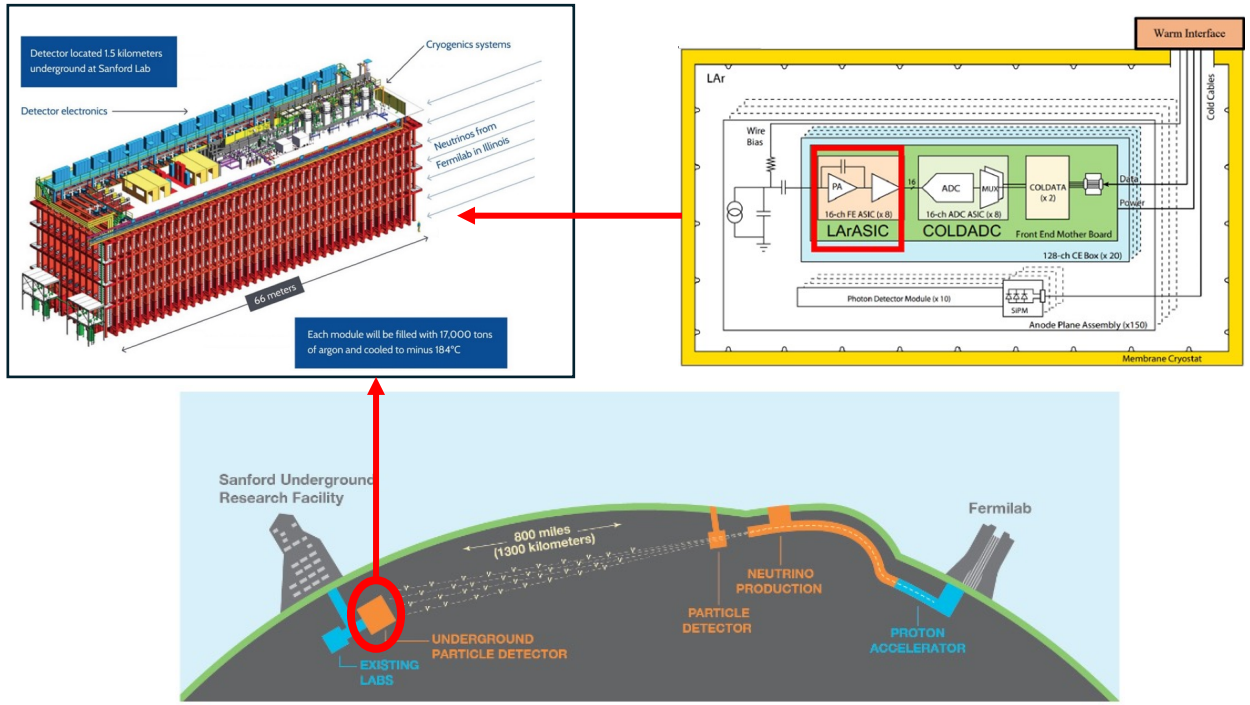
About a decade of development

Targets for CHARMS - DUNE [1]

Deep Underground Neutrino Experiment:

- Major scientific experiment for studying neutrino/antineutrino oscillations, detect neutrinos emerging from exploding stars, search for signs of proton decay
- DUNE far detector (FD) located 1.5 km underground in South Dakota will operate with an intense neutrino beam generated at Fermilab
- FD will utilize four 10kTon liquid argon time projection chambers (TPCs) to detect ionization charge and scintillation light generated when incident neutrinos interact with argon atoms



Usage	Temperature	Detector Capacitance	Shaping Time	Noise	Dynamic Range
FD 3/4 charge readout	89 K – 300 K	150 pF – 200 pF	250 ns – 2 μs	500 e^- at 89 K	10 bits
FD 3/4 light readout	89 K – 300 K	TBD	20 ns – 250 ns	TBD	10 bits

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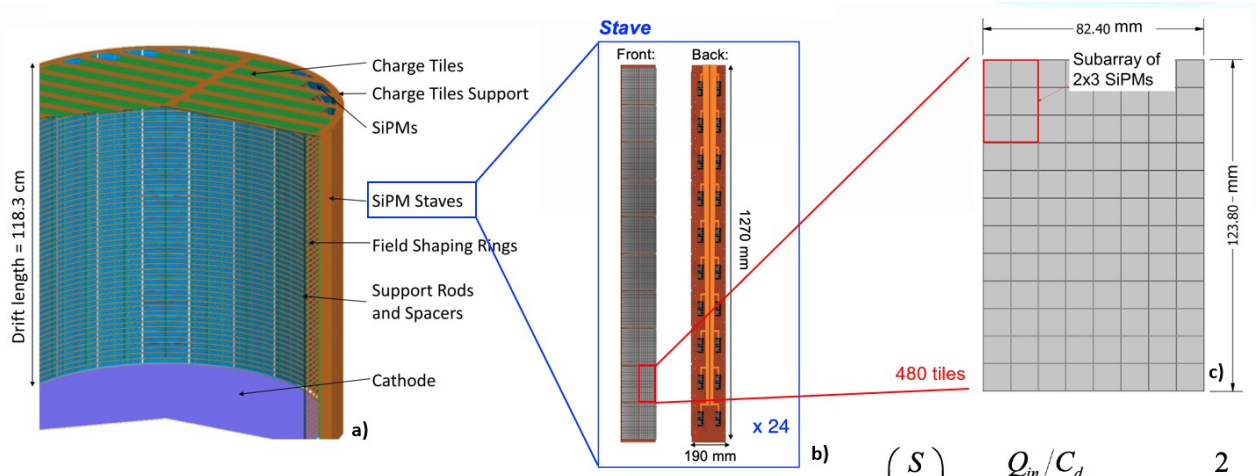
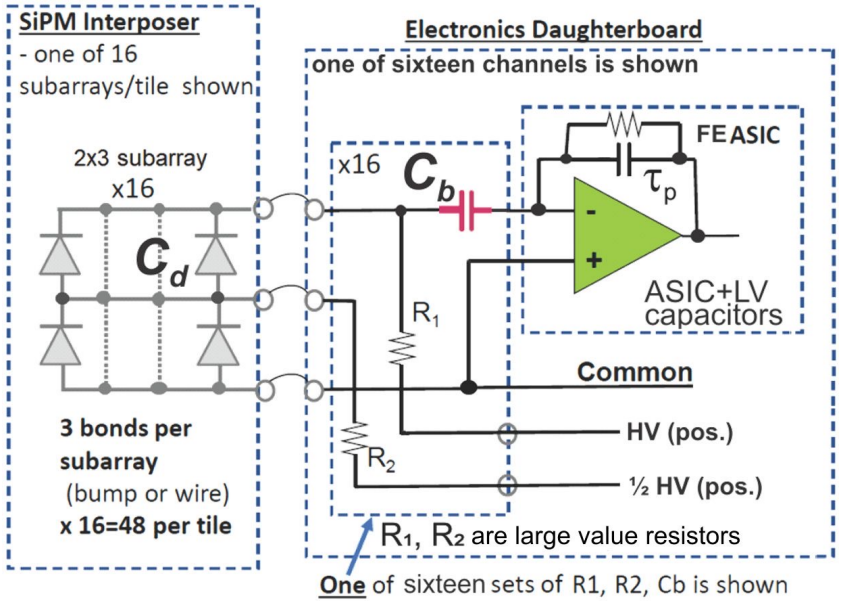
Targets for CHARMS - nEXO [2]

Enriched Xenon Observatory Experiment:

- Experiment for studying a rare nuclear decay called neutrinoless double beta decay
- nEXO will search for neutrinoless double beta decay in 5000 kg of the xenon-136 isotope (2 x 10^{28} nuclei), allowing potential observation of a few decays in the 10-year experiment span
- Combination of ionization charge and scintillation light detected at the anode of the TPC used to reconstruct the kinetic energy of the electrons from the decay
- Silicon photo-multipliers (SiPMs) used to convert the generated light signals to electrical signals



$$\left(\frac{S}{N}\right)_{n=2} = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{2}{1+C_g/C_b+4C_g/C_d} \approx 54$$



Usage	Temperature	Detector Capacitance	Shaping Time	Noise	Dynamic Range
nEXO light readout	160 K – 300 K	5 nF	1 μs	0.1 pe^- at 160 K	10 bits

C_b is a radiopure 100-500 pF/100 V capacitor

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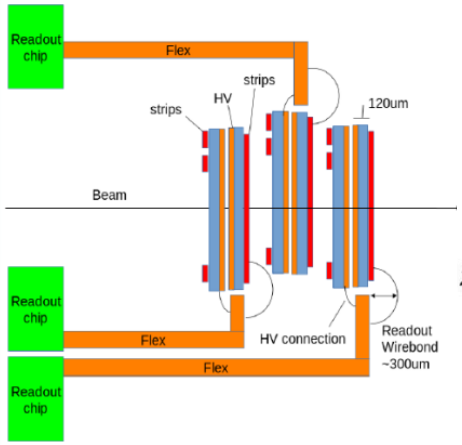
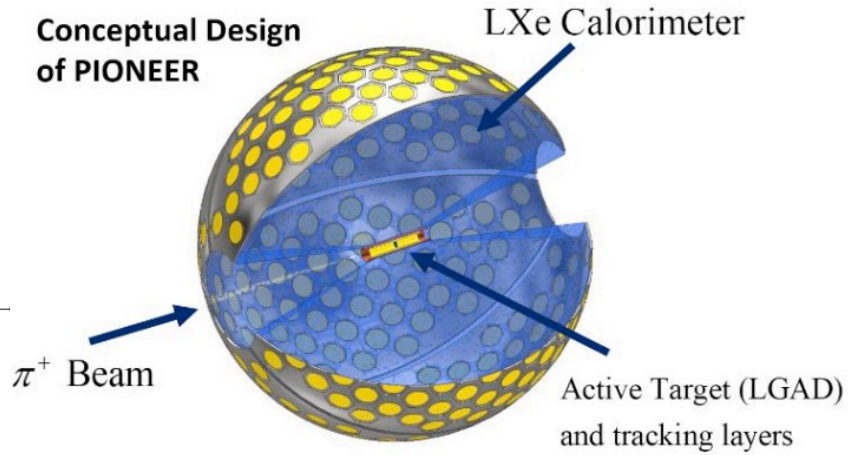
Targets for CHARMS - PIONEER [3]

PIONEER:

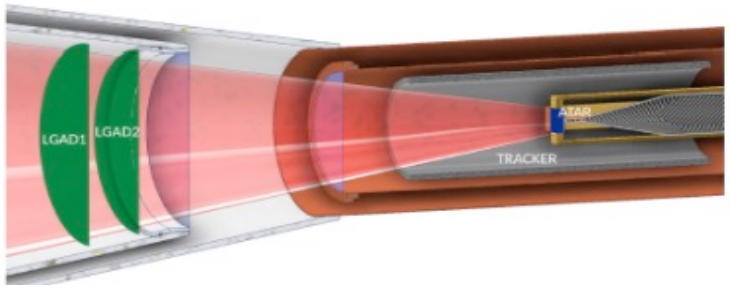
- Next generation rare pion decay experiment proposed at the Paul Scherrer Institute (PSI)
- Aims to measure the charged-pion branching ratio to electrons vs. muons
- Later phases will also study pion beta decay, aiming at an order of magnitude improvement in precision
- Front-end peaking time of ≈ 20 ns to allow identification of double hits



Readout



Usage	Temperature	Detector Capacitance	Shaping Time	Noise	Dynamic Range
PIONEER	160 K – 300 K	20 pF	20 ns	570 e^- at 160 K	10 bits



LGAD strip target (ATAR)

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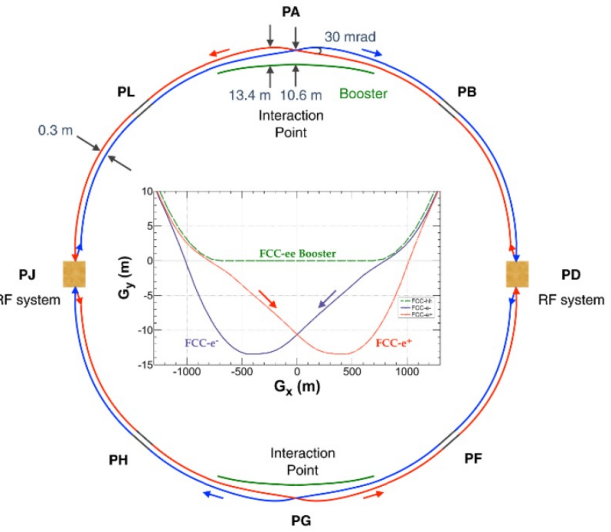
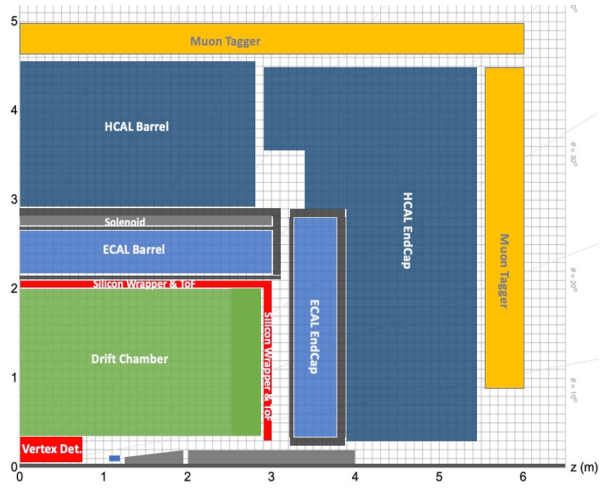
Targets for CHARMS - FCC-ee [4]

Electron-Positron Future Circular Collider:

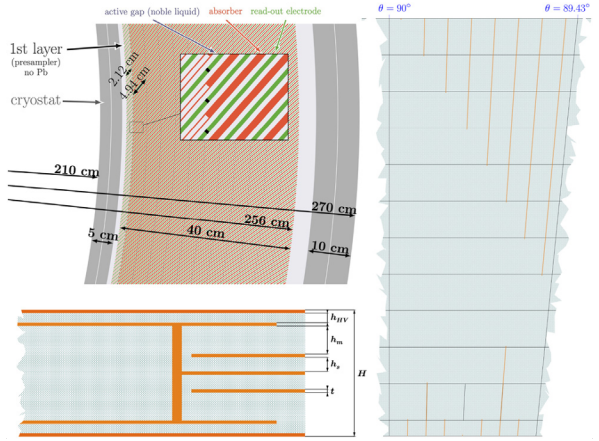
- Proposed to be constructed at CERN to serve as a general precision instrument for exploration of nature at the smallest scales
- Optimized to study with high precision the Z bosons, W pairs, Higgs bosons and top quark pairs
- **ALLEGRO (A Lepton coLlider Experiment with Granular calorimetry Read-Out)**, one of the proposed detectors, features a high granularity noble liquid electromagnetic calorimeter (ECAL) at its core





ALLEGRO detector layout with ECAL as the core housed inside the solenoid

Usage	Temperature	Detector Capacitance	Shaping Time	Noise	Dynamic Range
Allegro	89K/120K – 300K	TBD	100 ns – 200 ns	TBD	12 bits



High granularity noble liquid ECAL with PCB based electrodes

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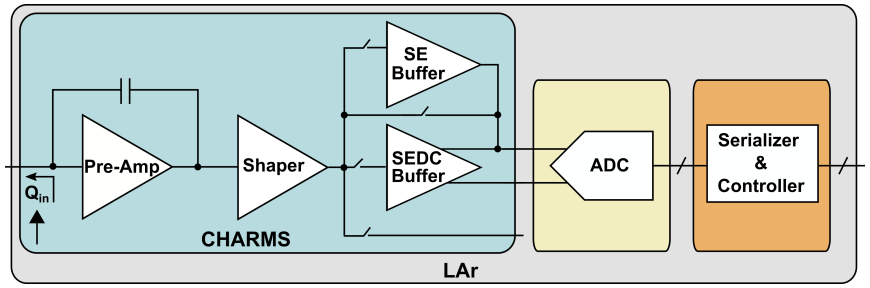
Planned specifications for CHARMS250

Technology	65 nm CMOS: 1-poly, 9-metal
Supply voltage	1.8 V
Temperature range	77 K – 300 K (optimized for 89 K)
Number of channels	16
Maximum single-ended output swing	1.4 V peak to peak
Gain	4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, 25 mV/fC
Full-scale input charge	300 fC, 180 fC, 100 fC, 56 fC
Baseline selection	200 mV (unipolar, collection mode), 900 mV (bipolar, induction mode)
Adaptive reset current	0.1 nA, 0.5 nA, 1 nA, 2 nA
Peaking time	250 ns, 500 ns, 1 µs, 2 µs
Output coupling	DC, AC
Output drive	Shaper, single-ended buffer, differential buffer
Integrated test capacitor	200 fF
Integrated pulse generator	10-bit DAC based
Configuration control	I^2C based for providing digital assistance (programmable gain, peaking time, baseline, RQI)

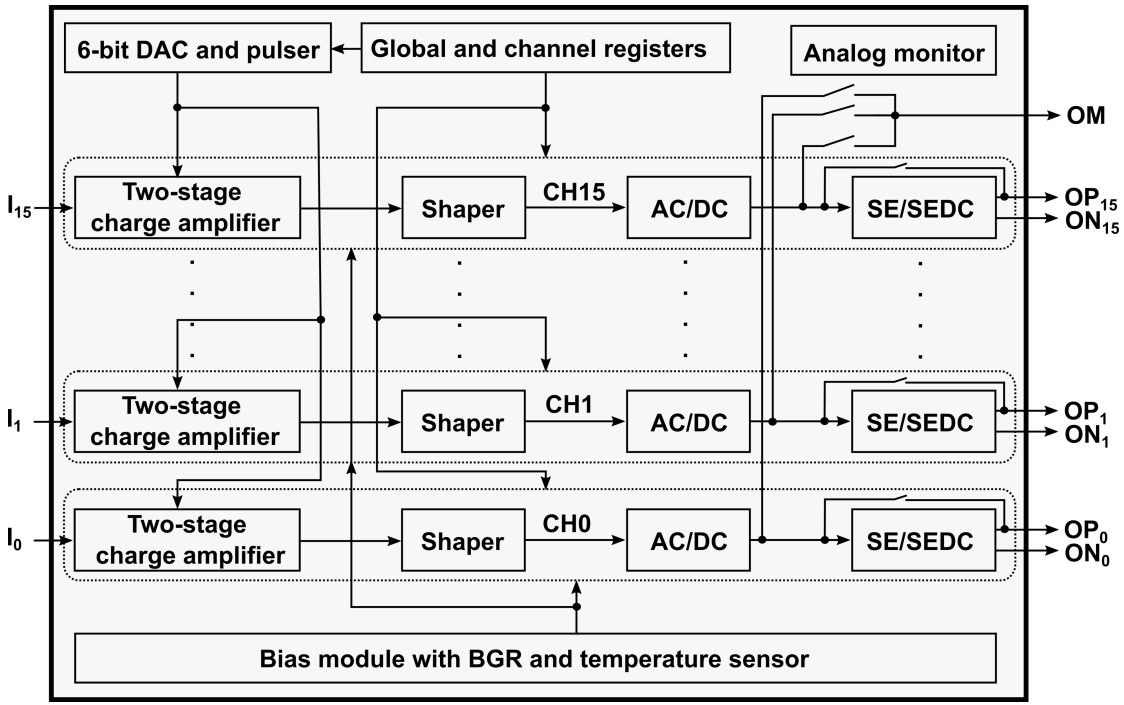
CHARMS10 (peaking time range 10-200 ns) also planned for development

- Key features and challenges
  - ***65 nm*** CMOS with ***thick oxide*** → To limit gate leakage current and ***parallel noise contribution***
  - ***Low*** power consumption → support detector electrodes with ***fine segmentations***
  - ***Cryogenic*** operation with ***long lifetime of electronics*** → achieve optimum ***SNR***
  - Long term goals: fast front-end architecture (***~GHz*** bandwidth) ⟶ support signal processing with stringent ***time resolution***

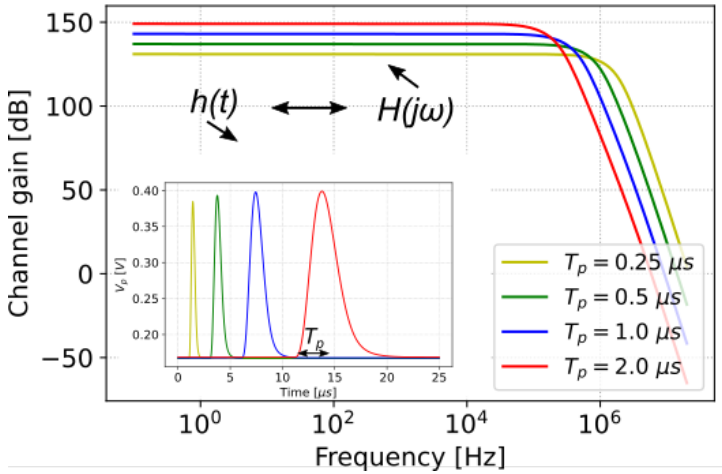
Architecture and functionality



3-ASIC solution



Top-level block diagram



Overall channel impulse response of CHARMS250 (acts as an anti-aliasing filter)

Peaking time (T_p)	Cut-of frequency (f_{-3dB})	Sampling frequency ($f_s = 2/T_p$)	Gain change at f_s
0.25 μs	820 KHz	4 MHz	-79 dB
0.5 μs	411 KHz	2 MHz	-71 dB
1.0 μs	205 KHz	1 MHz	-68 dB
2.0 μs	102 KHz	500 KHz	-66 dB

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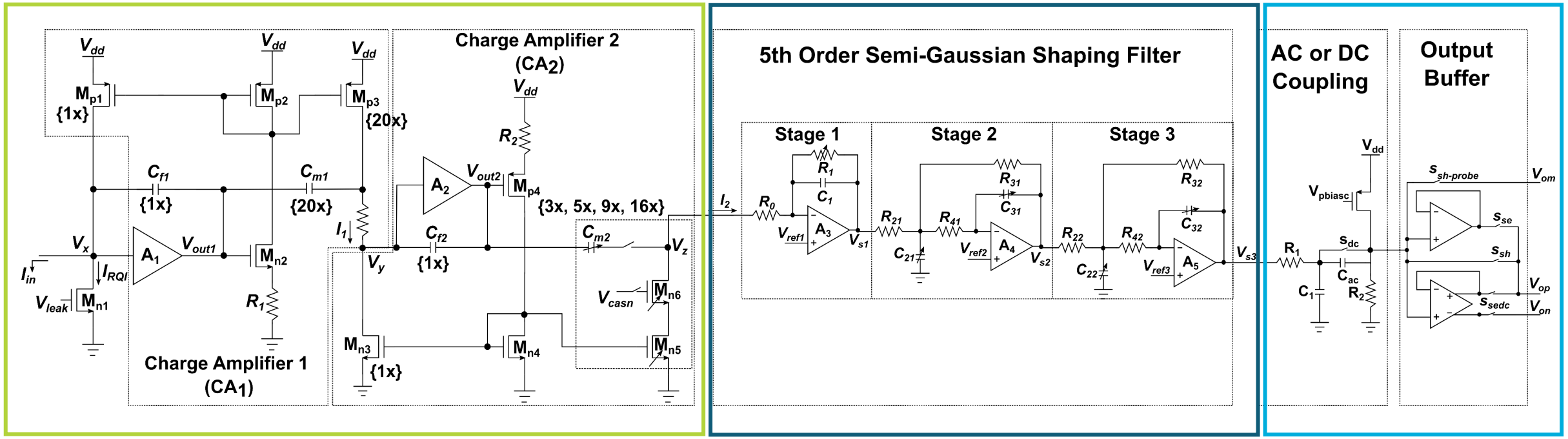
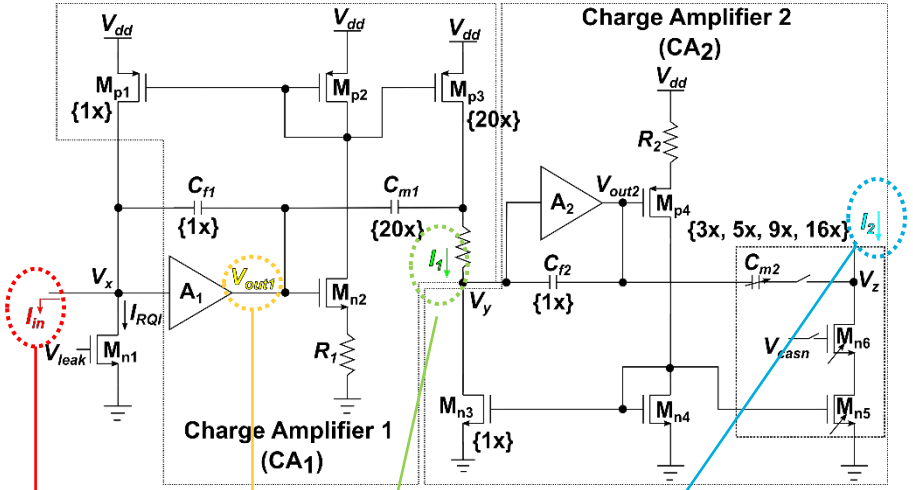
Core channel circuits

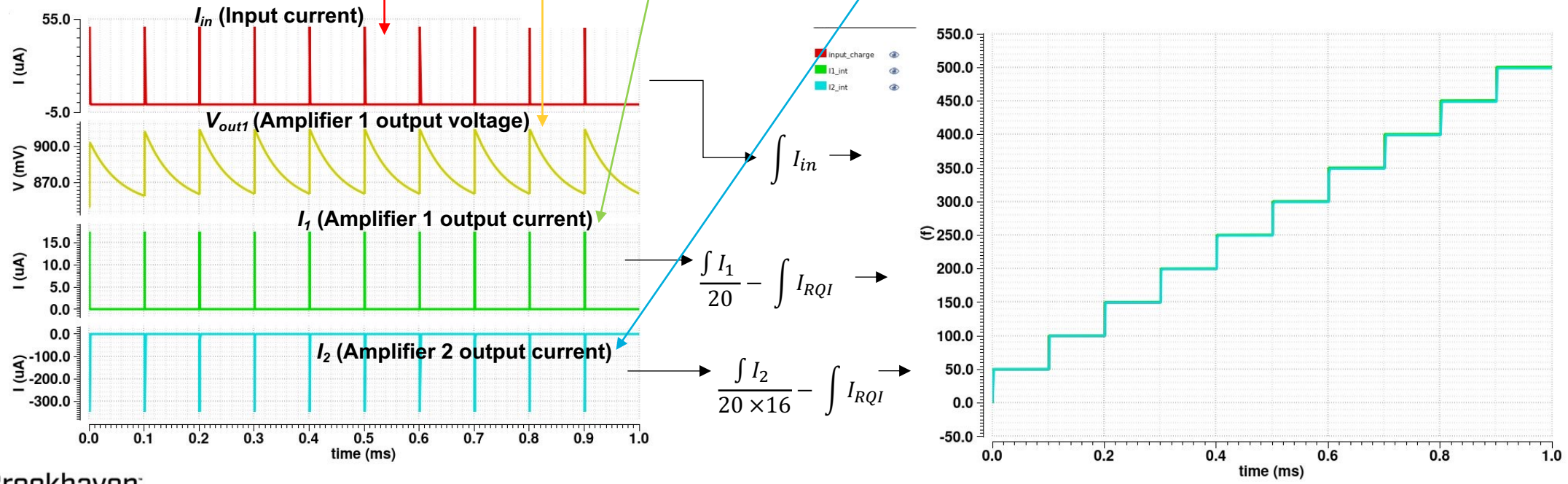


Charge amplifier design and transient response

- Charge amplifiers use current-mirror based adaptive continuous reset (I_{RQI} = 100 pA, 500 pA, 1 nA or 2 nA)
- Pole-zero cancellation implemented in each stage

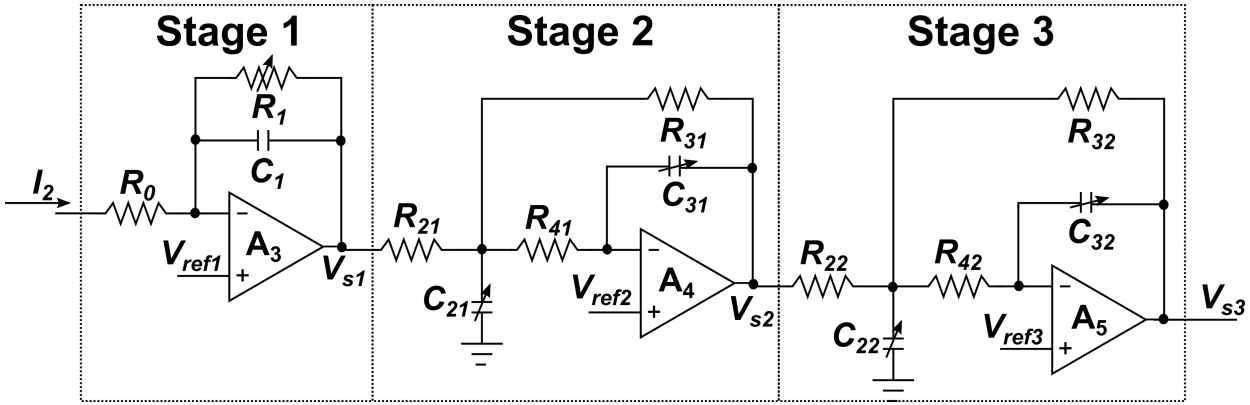


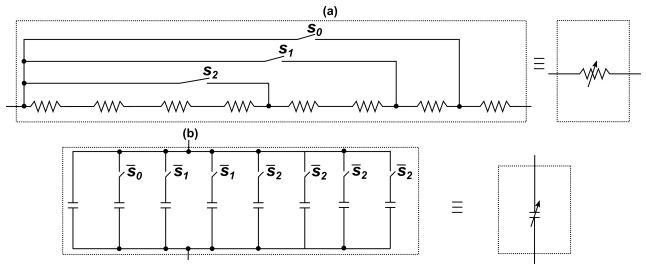
- A_1 and A_2: 3-stage amplifiers (> 100 dB gain for each, at both room and LAr temperatures)
- Charge gain provided by CSA_1 = 20
- Charge gain (programmable) provided by CSA_2 = 3 or 5 or 9 or 16



Ref: G. De Geronimo et. al., Front-End ASIC for a GEM based Time Projection Chamber

Shaping filter design





Resistor	Value (kΩ)	Capacitor	Value (pF)
R_0	0.3		
R_u (R_1)	7.5	C_1	11.9
R_{21}, R_{41}, R_{42}	18	C_u (C_{21})	5.9
R_{31}	60	C_u (C_{31})	1.39
R_{22}	36	C_u (C_{22})	5.5
R_{32}	39	C_u (C_{32})	1.13

$$V_{s1}(s) = -I_2(s)\frac{R_1}{(1+sC_1R_1)}$$

$$V_{s2}(s) = -V_{s1}(s)\frac{\frac{1}{R_{21}R_{41}C_{21}C_{31}}}{s^2 + s\left(\frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}}\right) + \frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar……

- Peaking time is programmable (0.25 μs – 2 μs)
- Lower series noise with longer shaping times
- Implemented shaper is a 5th order semi-gaussian filter with complex conjugate poles
- Semi-gaussian shaper has a faster return to baseline than a CR-RCⁿ shaping filter
- Faster tail lowers contribution of parallel noise
- Symmetric rising and falling edges also helpful for mitigating pile-up of events
- A_3, A_4, A_5 are two-stage miller compensated differential amplifiers
- V_{ref1}, V_{ref2}, V_{ref3} selected based on output baseline setting

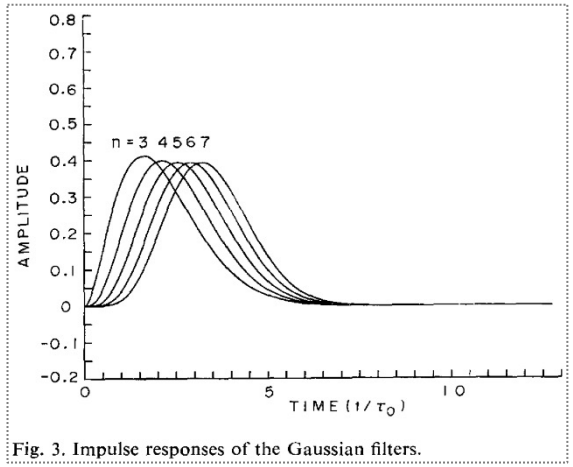
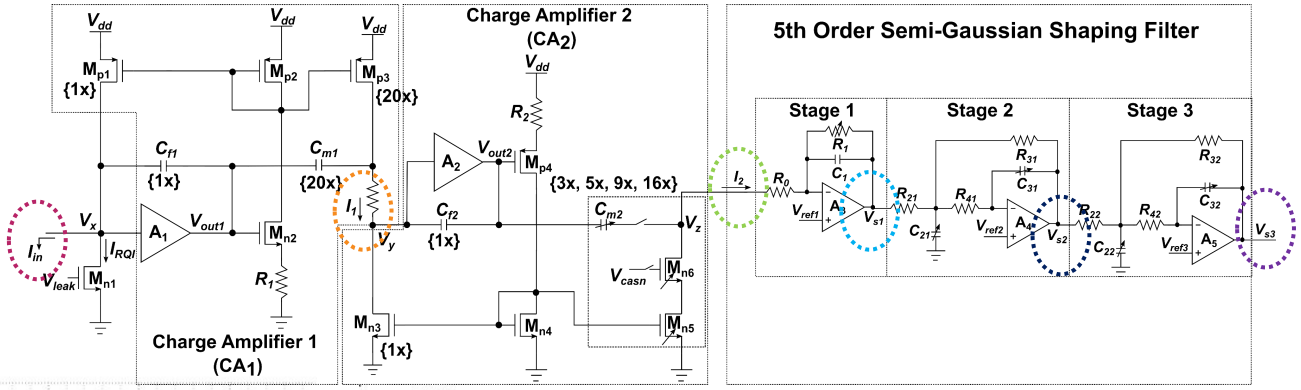


Fig. 3. Impulse responses of the Gaussian filters.

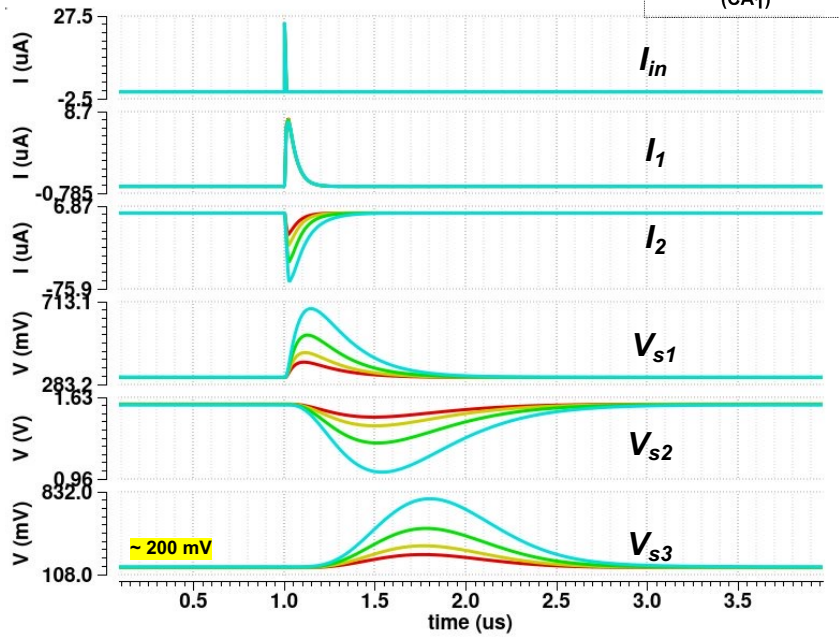
Ref: S. Ohkawa, M. Yoshizawa, K. Husimi, *Direct synthesis of the Gaussian filter for nuclear pulse amplifiers*.

Analog chain simulated impulse response at LArT

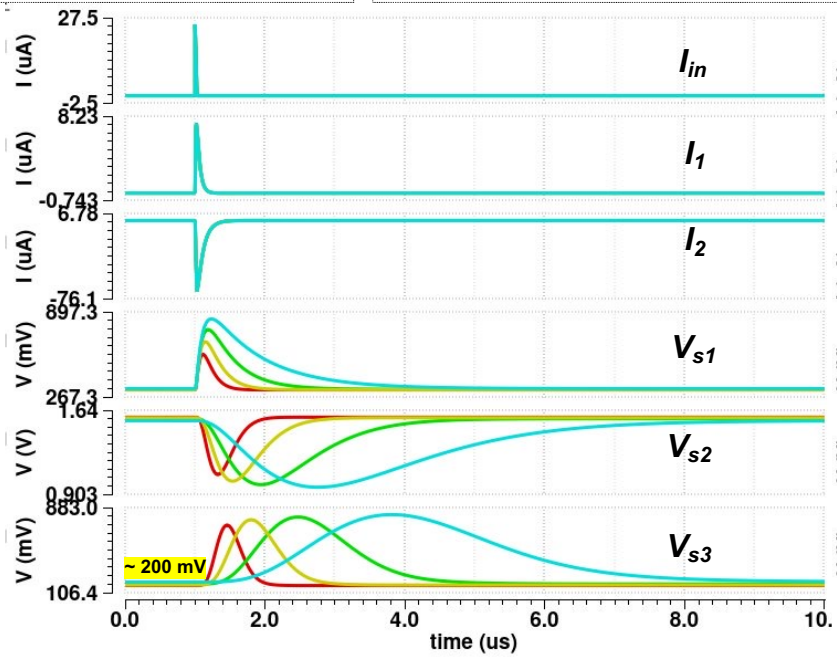
I_{in} : Input current
I_1 : Amplifier 1 output current
I_2 : Amplifier 2 output current



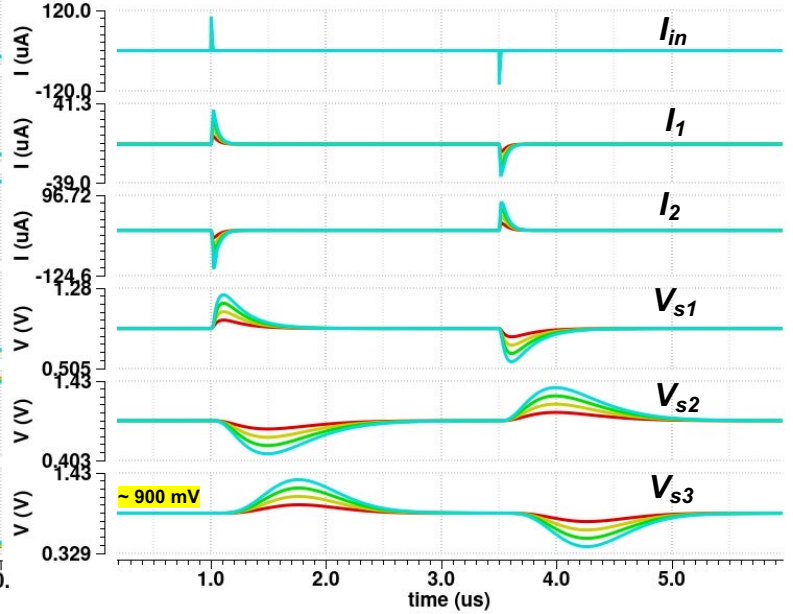
V_{s1} : Shaper stage 1 output voltage
V_{s2} : Shaper stage 2 output voltage
V_{s3} : Shaper stage 3 output voltage



Programmable gain
(4.7 mV/fC, 7.8 mV/fC,
14 mV/fC, 25 mV/fC)



Programmable peaking
time (0.25 µs, 0.5 µs,
1.0 µs, 2.0 µs)



Non-collecting mode
(Bipolar charges with
magnitude 25 fC, 50 fC,
75 fC, 100 fC)

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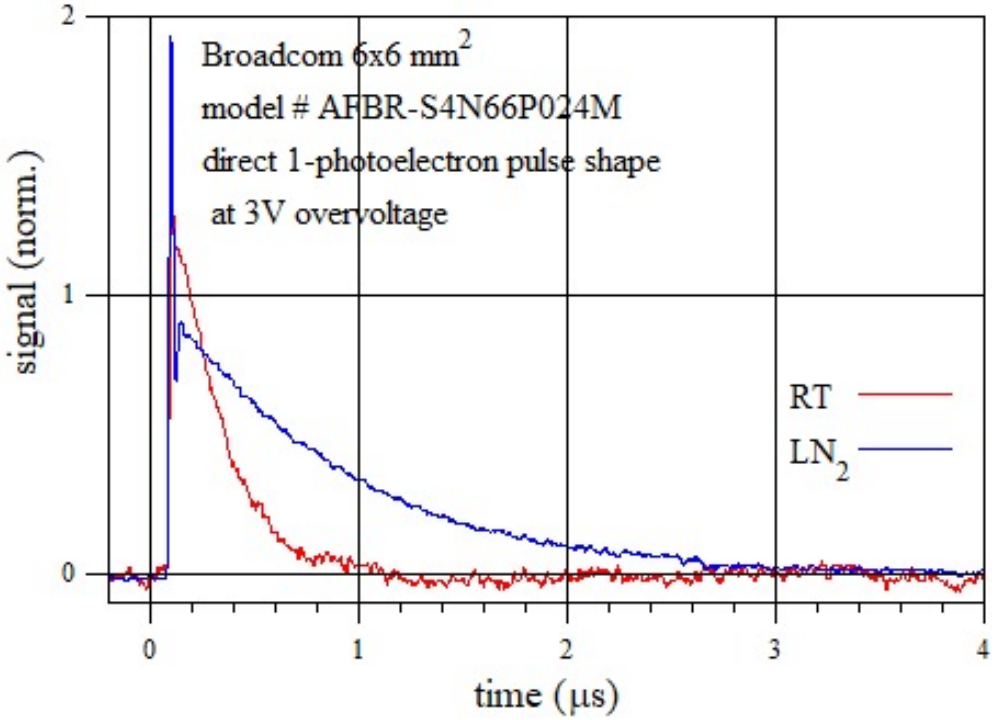
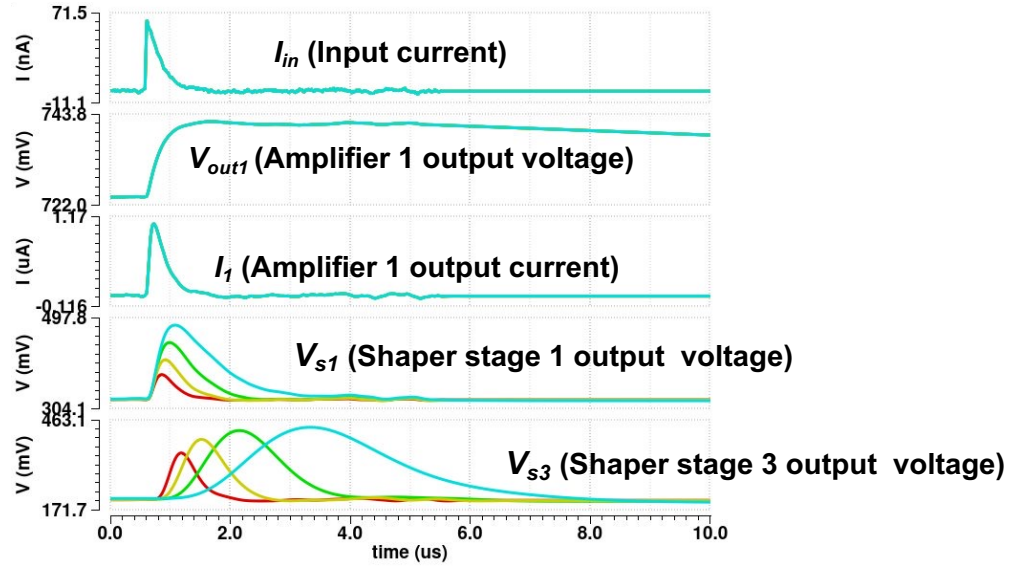
Analog chain simulated response to SiPM output

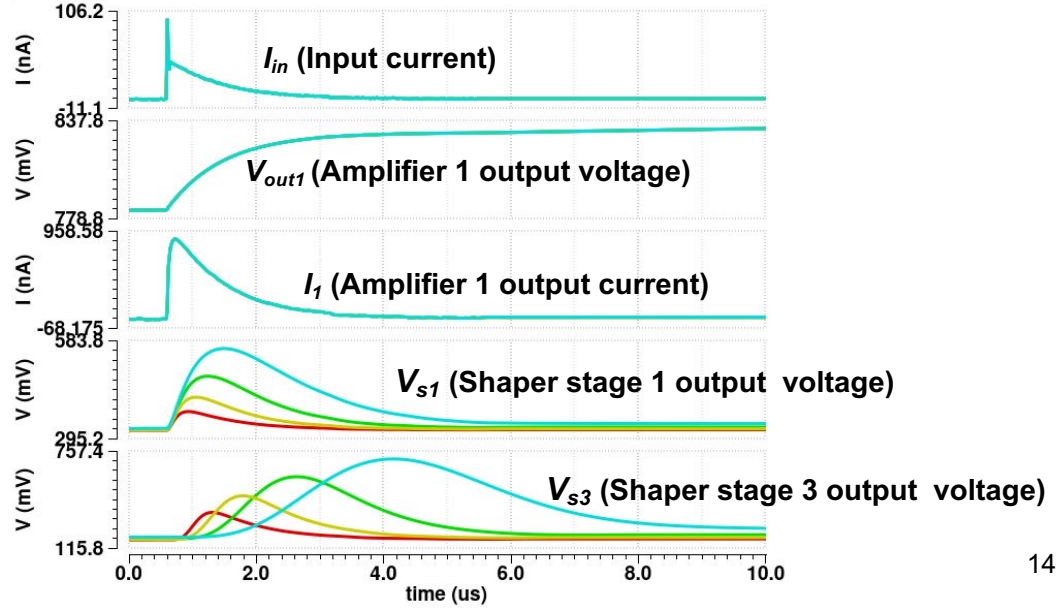


Courtesy: Thomas Tsang, Instrumentation Department, Brookhaven National Laboratory

Room temperature

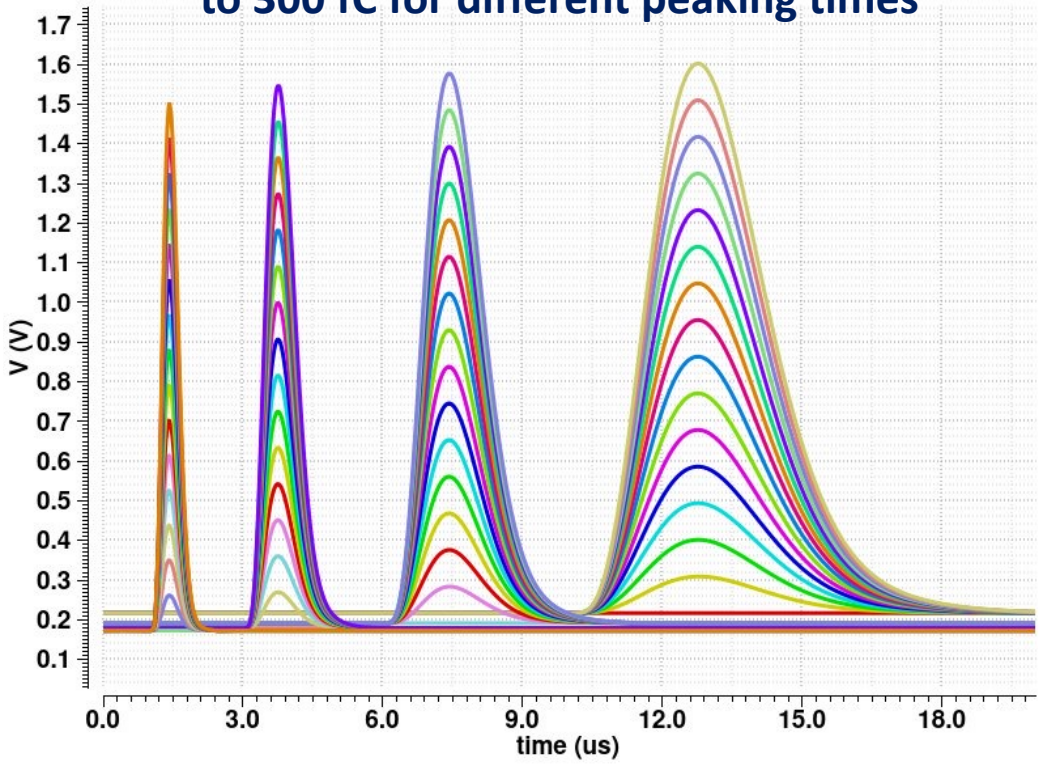


Liquid argon temperature

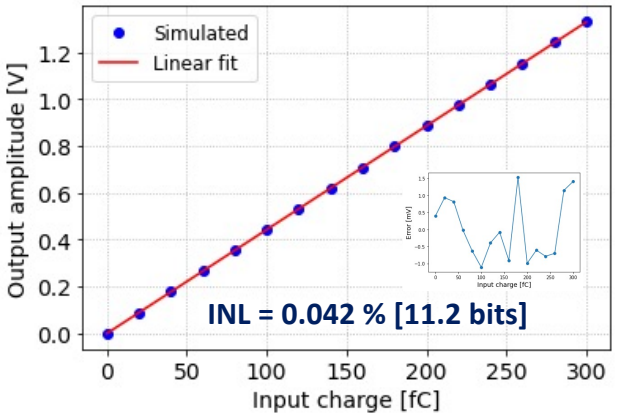


Simulated response for full-charge range and linearity

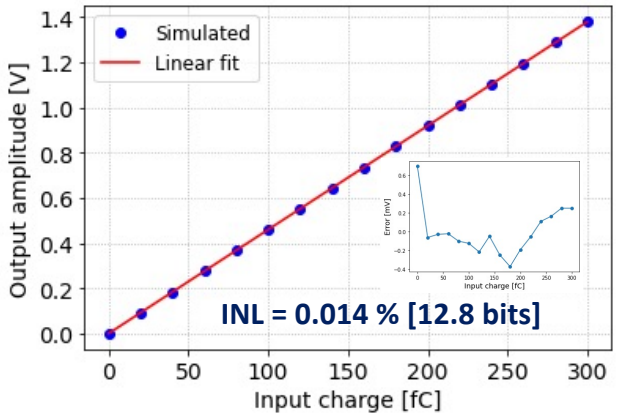
Shaping filter output (V_{s3}) for input charges up to 300 fC for different peaking times



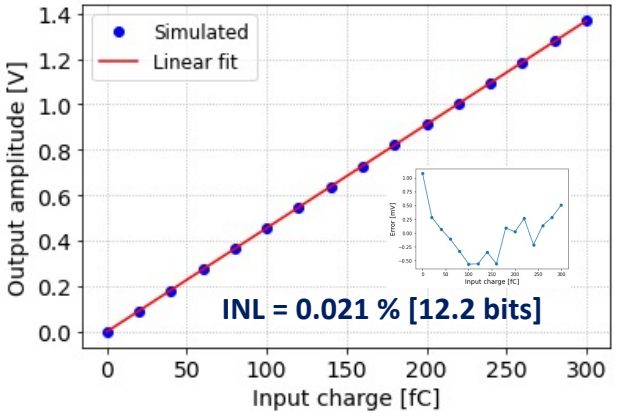
T_p = 0.25 µs



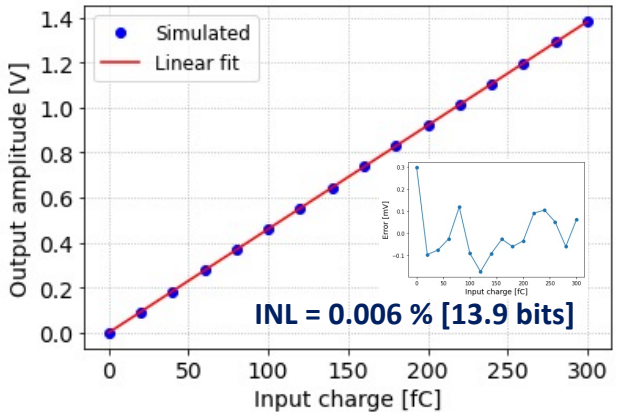
T_p = 1.0 µs



T_p = 0.5 µs



T_p = 2.0 µs



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Noise minimization strategy

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of white series noise, 1/f series noise and parallel noise components)

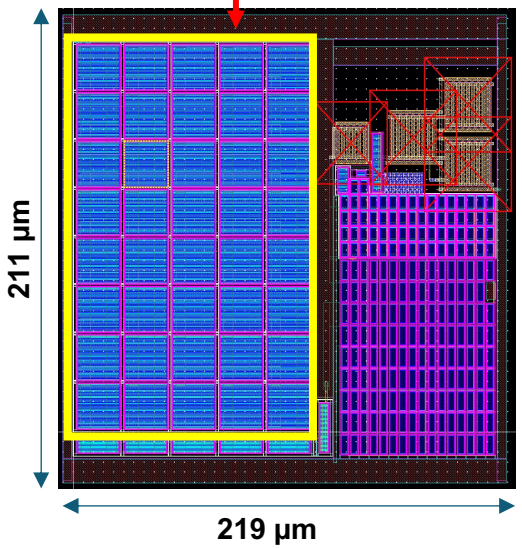
$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input stage transistor sized to have C_g ~ 40 pF, optimal choice for minimizing noise with C_{det} ~ 150 pF with given power budget

	Minimum allowable transistor length	Input transistor length	Input transistor width
180 nm (LArASIC)	180 nm	270 nm	20 mm
65 nm (CHARMS250)	280 nm	400 nm	24 mm

Input transistor implemented with 30 copies of transistors of width of 20 µm and 40 fingers



- **Input stage transistors for A_1 implemented using thick oxide (2.5 V) devices in 65 nm for CHARMS to limit leakage current and associated parallel noise**
- **Thin oxide device of the same dimensions has a gate leakage current of ≈ 20 nA, contributing almost 200 electrons to the ENC for 1 µs peaking time and triangular weighting function!**

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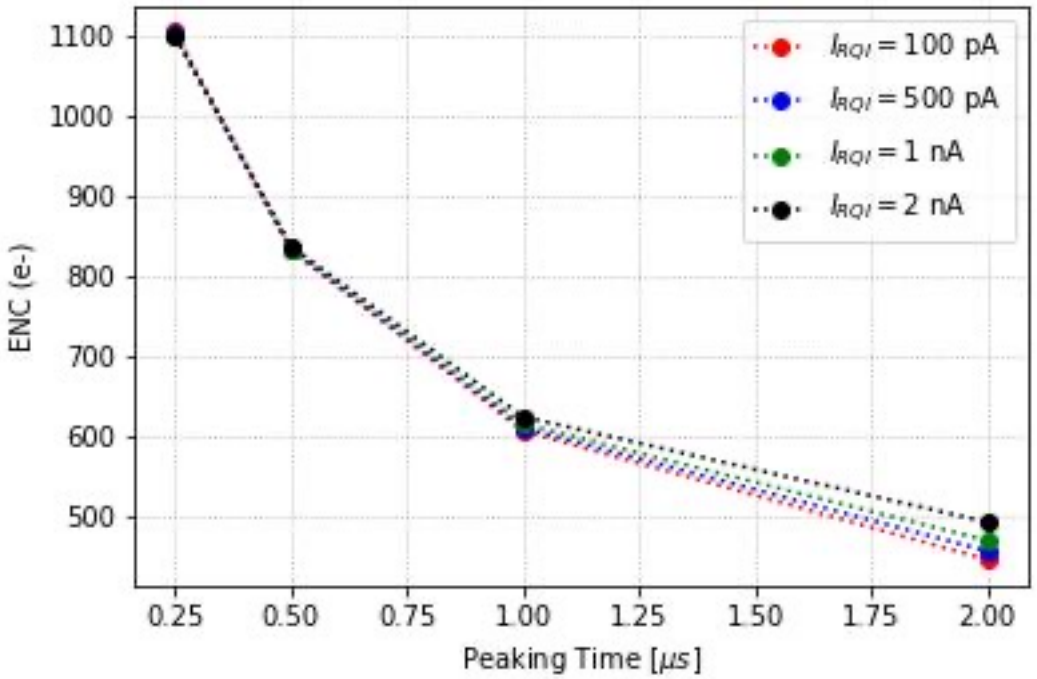
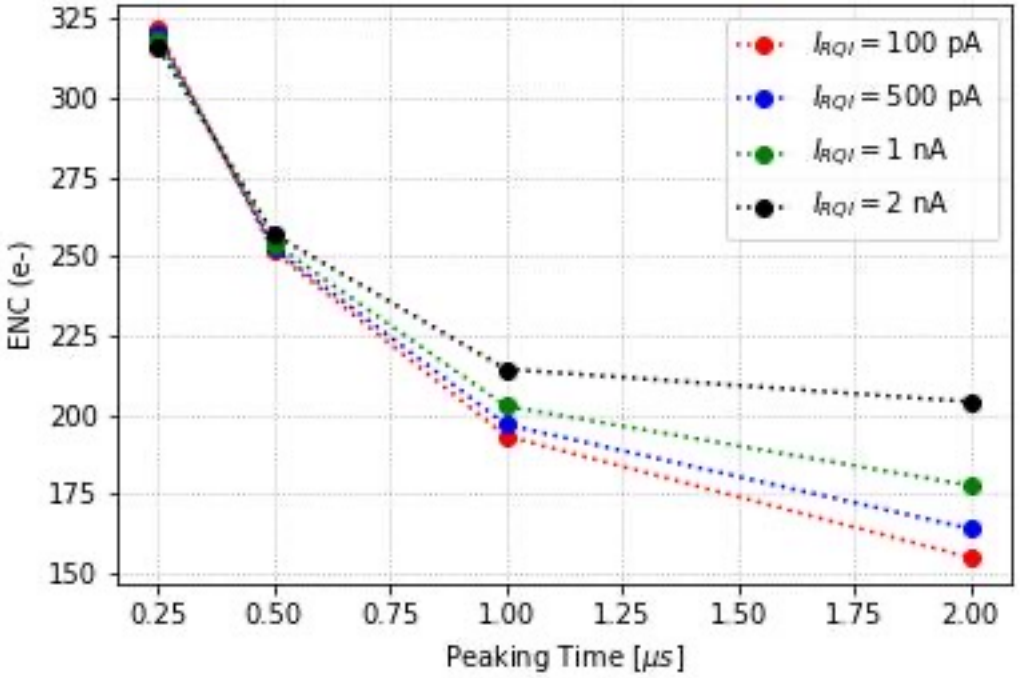
Ref: [1] Angelo Rivetti, Front-End Electronics for Radiation Sensors
[2] Veljko Radeka, Signal Processing for Particle Detectors

Noise (simulated) with C_d = 160 pF

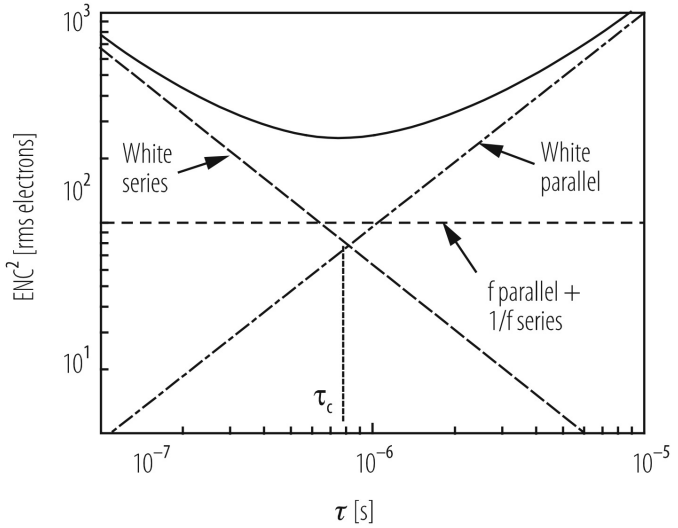
Room temperature



Liquid argon temperature



Ref: Veljko Radeka, Signal Processing for Particle Detectors



- 60-75% noise contribution is from the input transistor (thermal noise contribution dominates, flicker noise contribution is less than 5 %)
- Increased parallel noise contribution for longer peaking times and higher values of I_{RQI}
- For larger values of IRQI, parallel noise contribution from I_{RQI} is ~ 20 %
- Noise characterization needs to be done at liquid argon temperature

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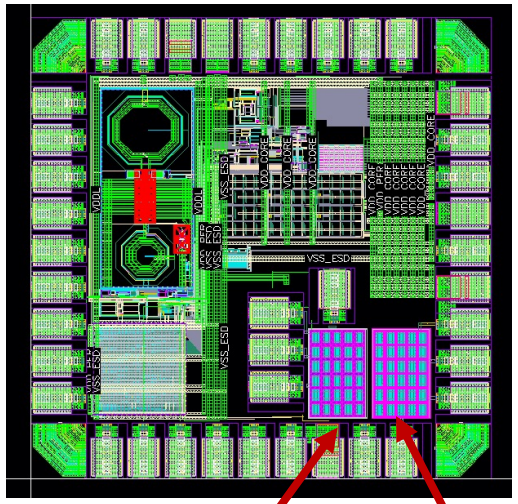
CHARMS250 status

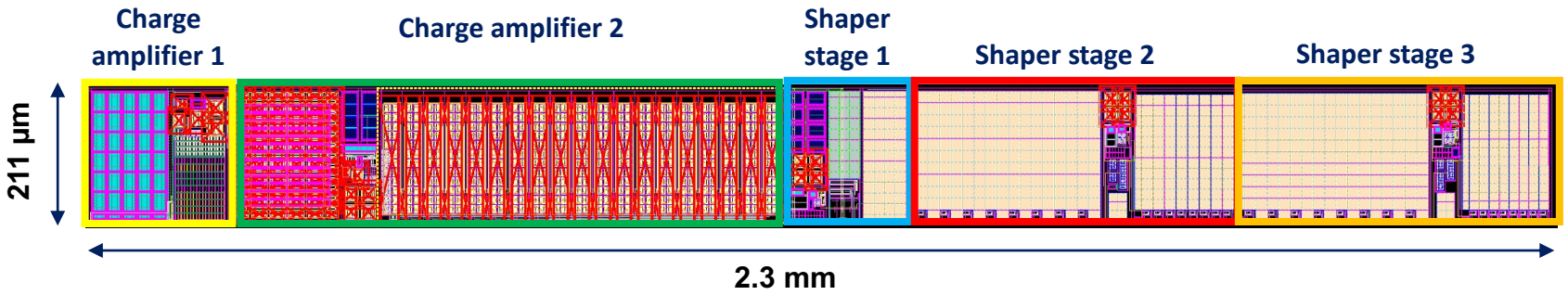
Transistor test structures with dimensions of the input transistor fabricated for characterization at room and cryogenic temperatures



Thick-oxide NMOS (L = 400 nm, W = 24 mm)

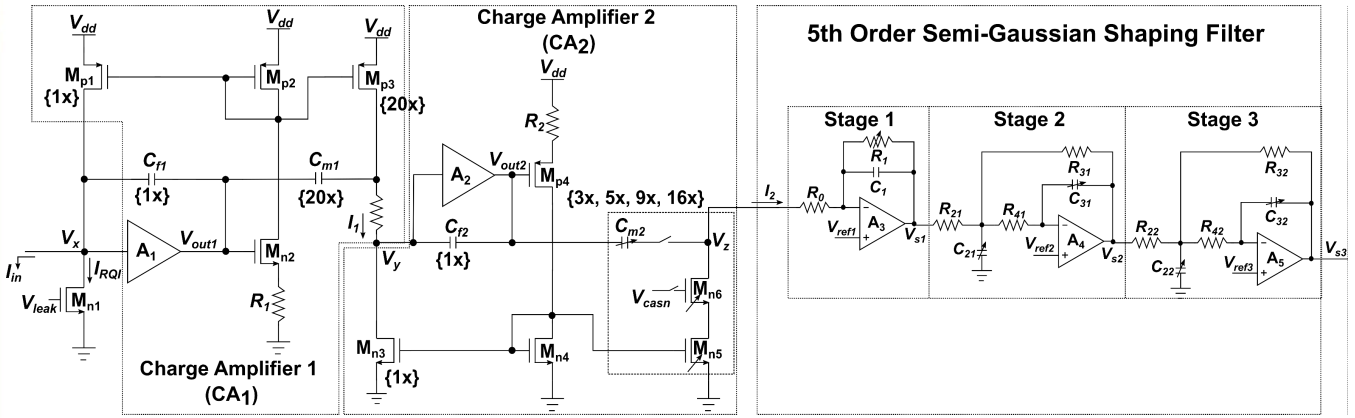
Thick-oxide PMOS (L = 400 nm, W = 24 mm)

Analog front-end layout



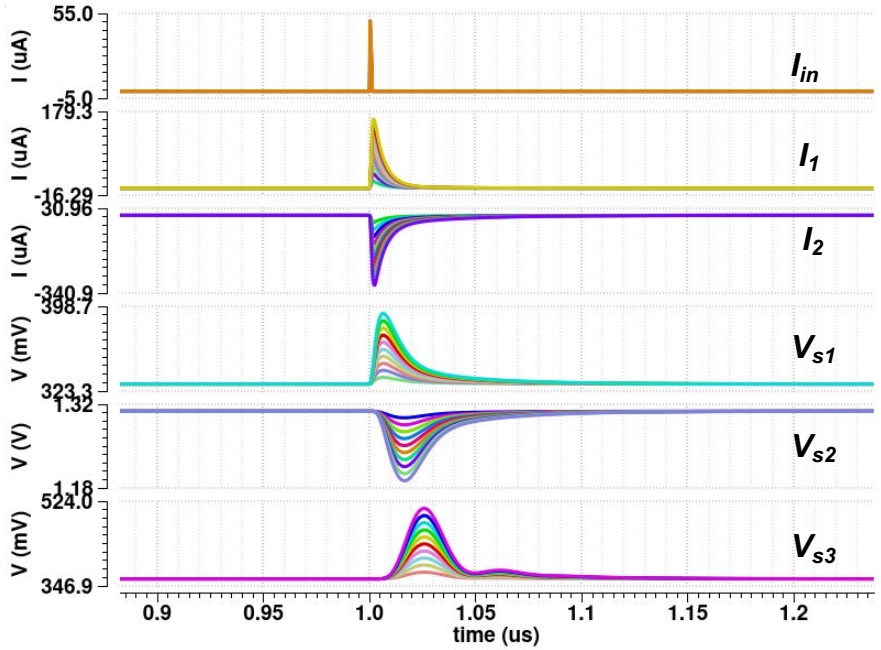
Prototype CHARMS250 chip to be submitted for fabrication

Plan for CHARMS10 (10 ns ≤ T_p ≤ 250 ns)



- Limited bandwidth of A_1 and A_2 disallows shaping times < 250 ns
- Currently, amplifiers A_1 and A_2 implemented as 3-stage amplifiers
- Difficult to achieve higher bandwidth without sacrificing stability
- CHARMS10 will incorporate current increase and topology modification for A_1 and A_2

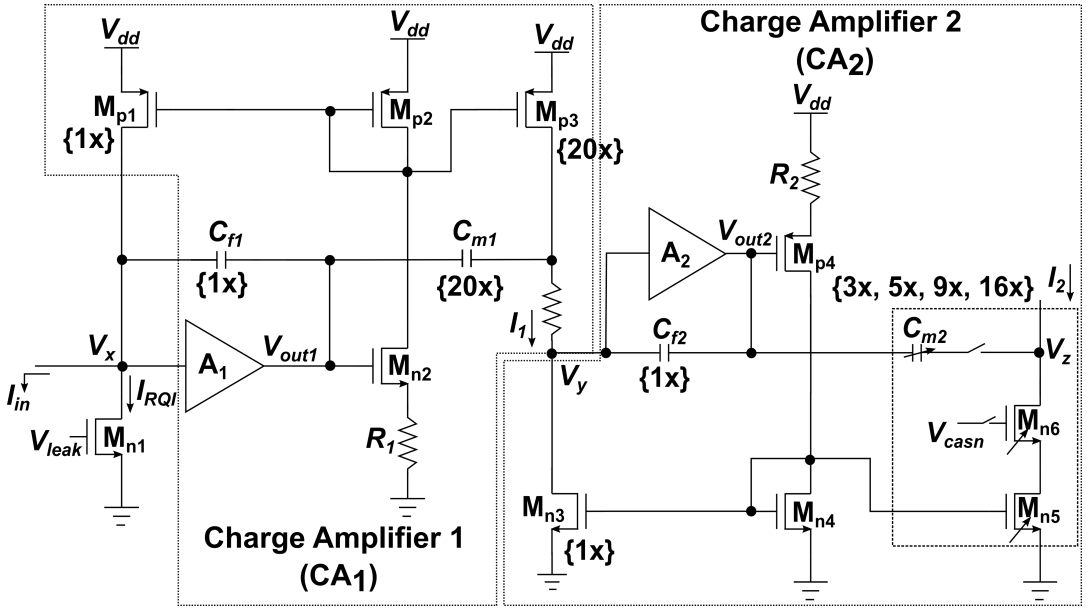
Transient response for variable input charge (50 fC – 300 fC) with A_1, A_2, A_3 modeled as ideal VCVS



Thank You

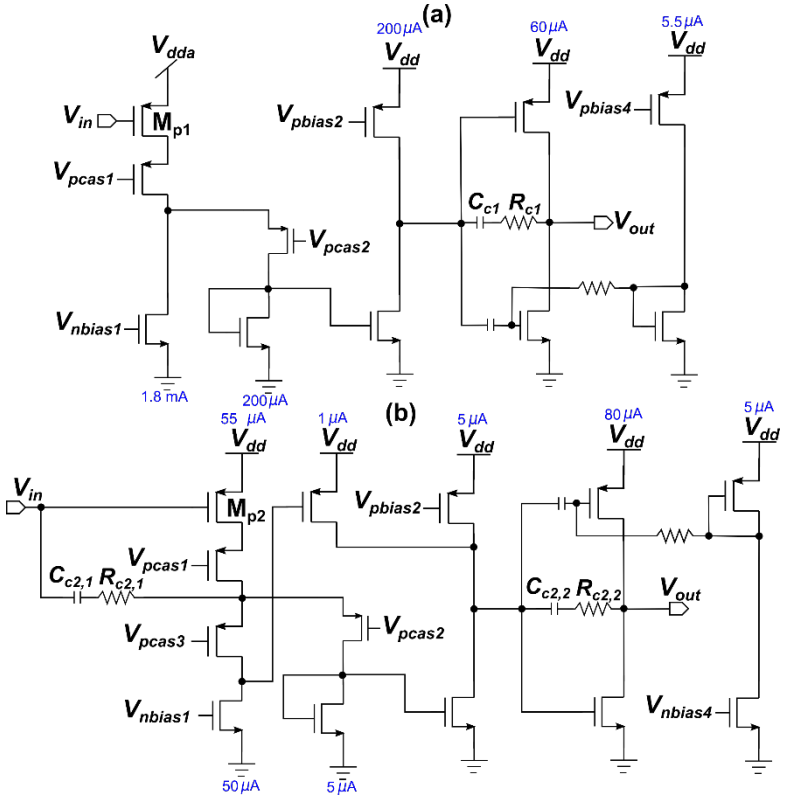
Backup Slides

Charge amplifier design



- Charge amplifiers use current-mirror based adaptive continuous reset (I_{RQI} = 100 pA, 500 pA, 1 nA or 2 nA)
- Pole-zero cancellation implemented in each stage
- Charge gain provided by CSA_1 = 20
- Charge gain (programmable) provided by CSA_2 = 3 or 5 or 9 or 16

A_1 schematic diagram



A_2 schematic diagram

- A_1 and A_2: 3-stage amplifiers (> 100 dB gain for each, at both room and LAr temperatures)

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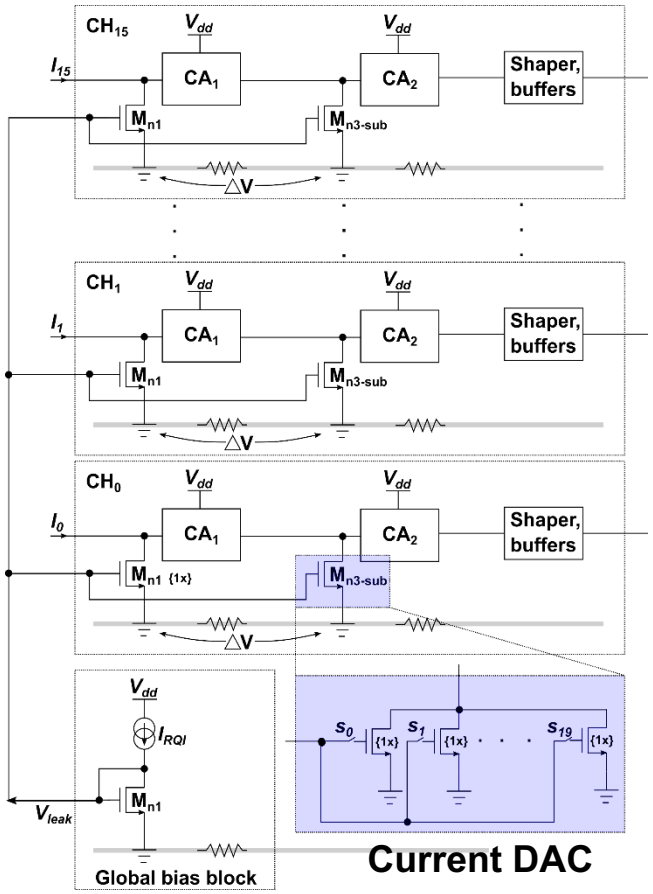
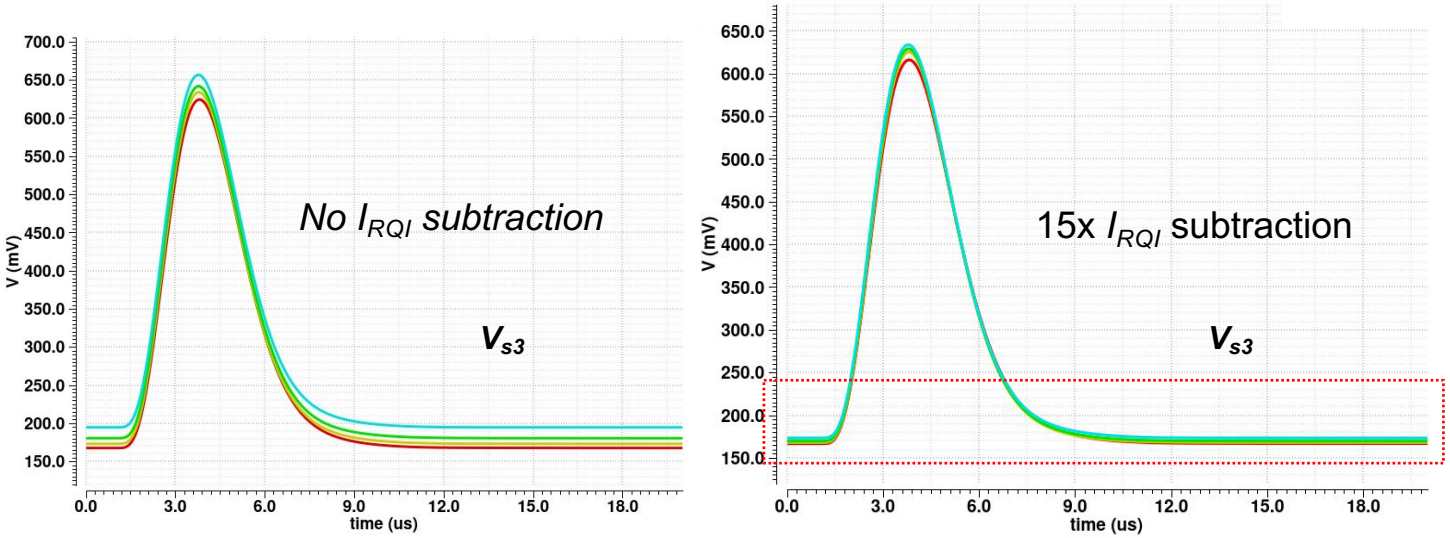
Ref: G. De Geronimo et. al., Front-End ASIC for a GEM based Time Projection Chamber

Programmable 5-bit RQI subtraction implemented in CHARMS250



Current DAC

Response with different values of I_{RQI}



Baseline drift reduced

- Programmable I_{RQI} subtraction provides immunity against process mismatches and layout induced non-ideality
- For M_{n1} and $M_{n3\text{-}sub}$ operating in deep-subthreshold ($I_{RQI} \propto e^{(Vgs\text{-}Vth)(q/\eta kT)}$), variance in at LNT almost 10x higher than at RT
- Previously, with fixed I_{RQI} subtraction, even few-millivolts of V_{gs} difference at M_{n1} and $M_{n3\text{-}sub}$ due to IR drop in ground rail was seen to cause subtraction to become > 20x and make the second stage reset mechanism non-operational

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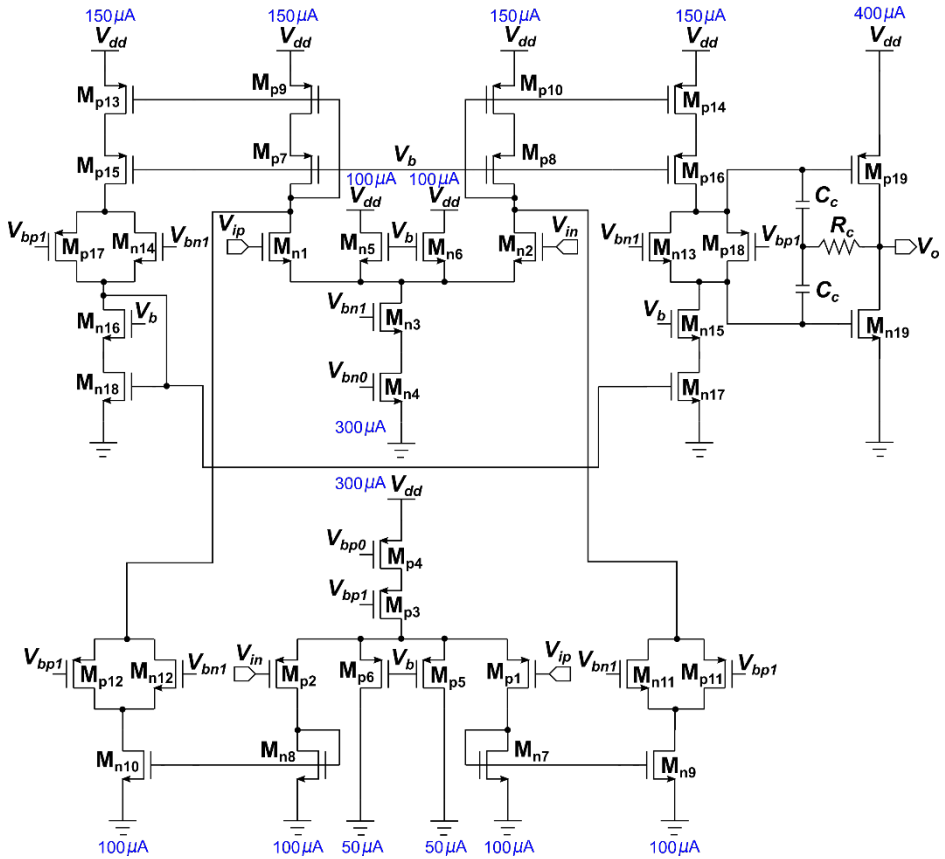
Output buffer design – single ended (SE) buffer



- Based on a folded-cascode current-mirror based operational transconductance amplifier
- Comprises of parallel NMOS and PMOS input pairs to support rail-to-rail operation
- Monticelli class-AB output stage used
- High open-loop DC gain (> 110 dB at LArT) ensures minimal introduction of distortions in the output signal
- Suitable to drive tens of pF of capacitance load (chip-to-chip trace)

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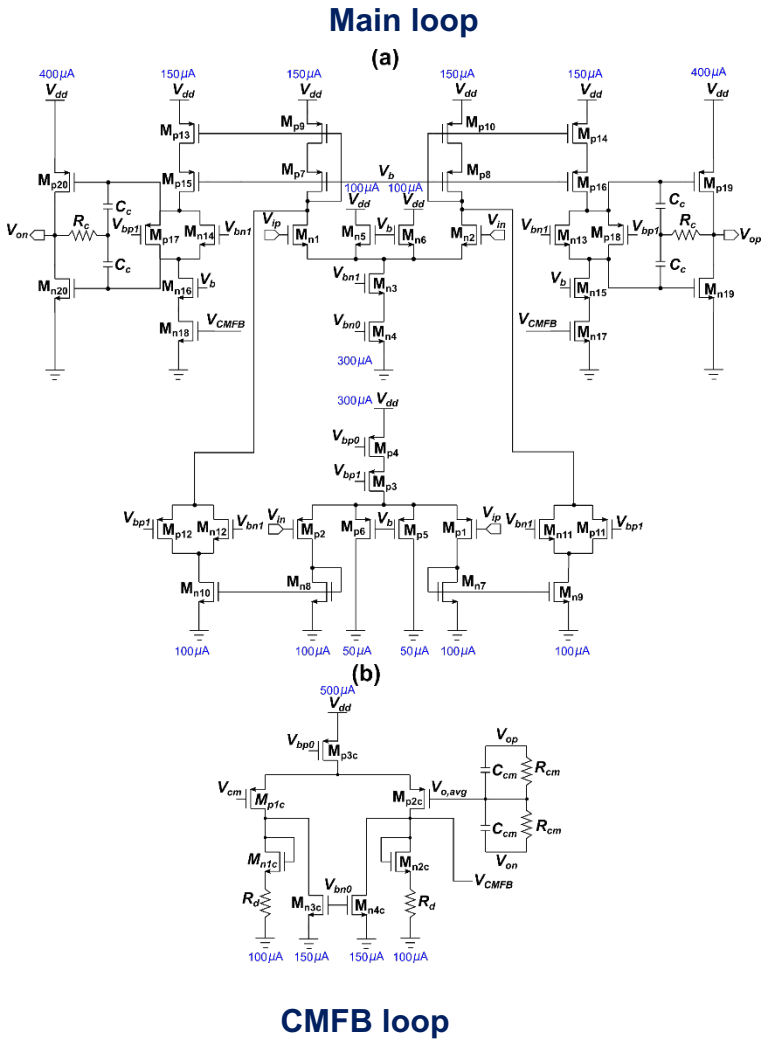
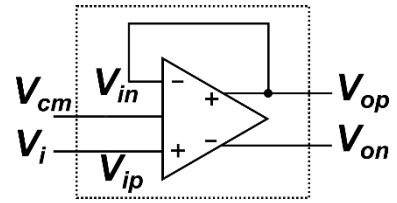
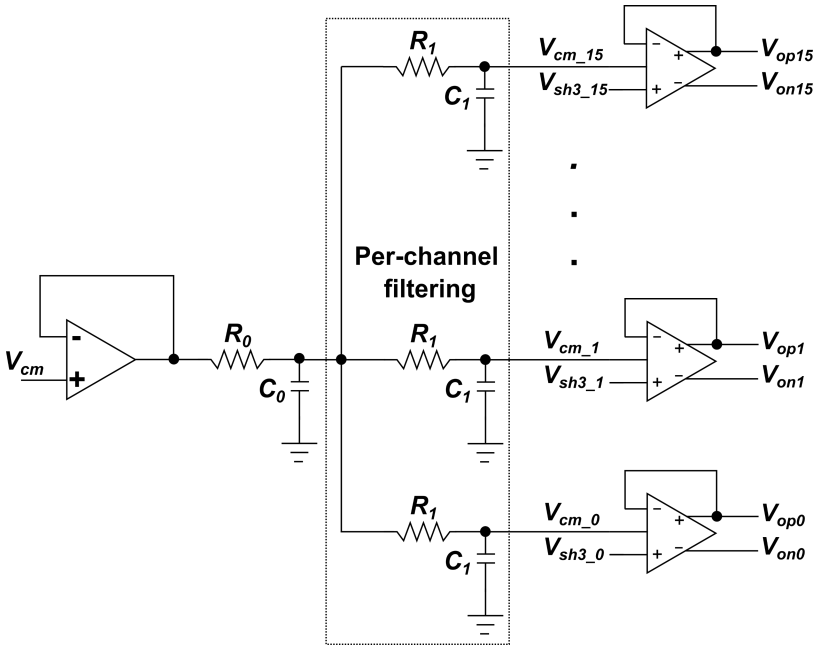
Output buffer design – single ended (SEDC) buffer



- Simpler, more compact and power-efficient compared to resistor or 3-operational amplifier based SEDC designs
- Circuit implementation similar to SE buffer, but core is fully-differential (inputs and outputs)
- Noise transferred from common-mode input signal (V_{cm}) to the output with 6 dB gain
- Global and local noise filtering implemented for V_{cm}
- Both common-mode and differential paths have high open loop DC voltage gains (> 110 dB) and comparable bandwidths (≈100 MHz) at LArT
- Helps with crosstalk cancellation





Status of LArASIC

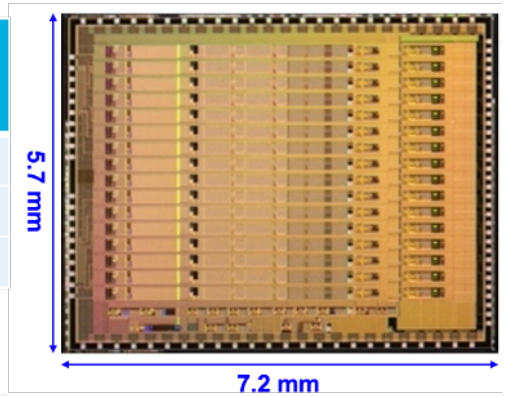
LArASIC MPW met all the DUNE requirements → fabricated ~1800 P5 and 1800 P5B (180 nm) chips (eng. run) for ProtoDUNE II

LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5	RT	49	49	100 %
P5B	**RT**	**1642**	**1635***	**~99.57 %**
P5B	**LNT**	**317**	**317**	**100 %**

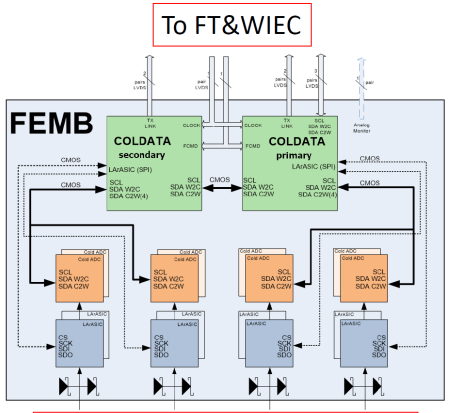
P5B has improved input ESD protection compared to P5

*Only 1 out of 16 channels in each of the two chips are non-functional

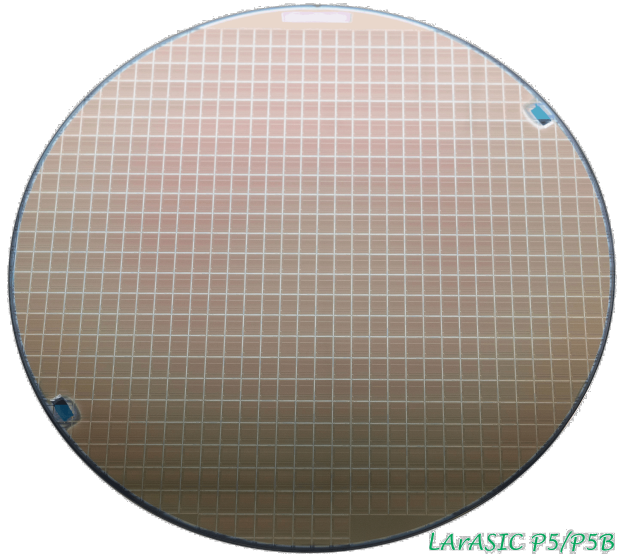
>1 year ago, now more statistics is available



LArASIC performance with differential interface



24 FEMBs arrived at CERN for ProtoDUNE-II installation



250 wafers LArASIC production run for DUNE 75k P5 and 75k P5B chips

8” wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

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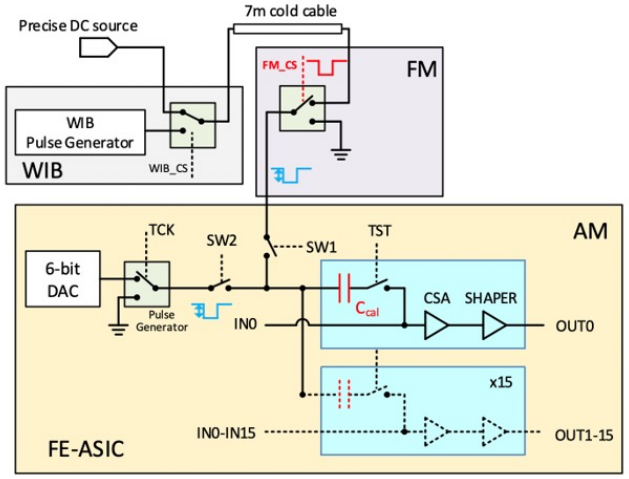
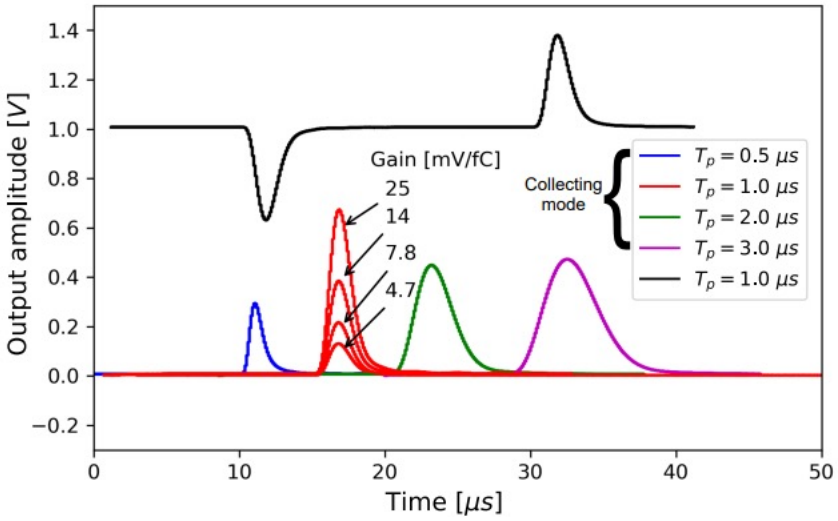
LArASIC measurement results [1]

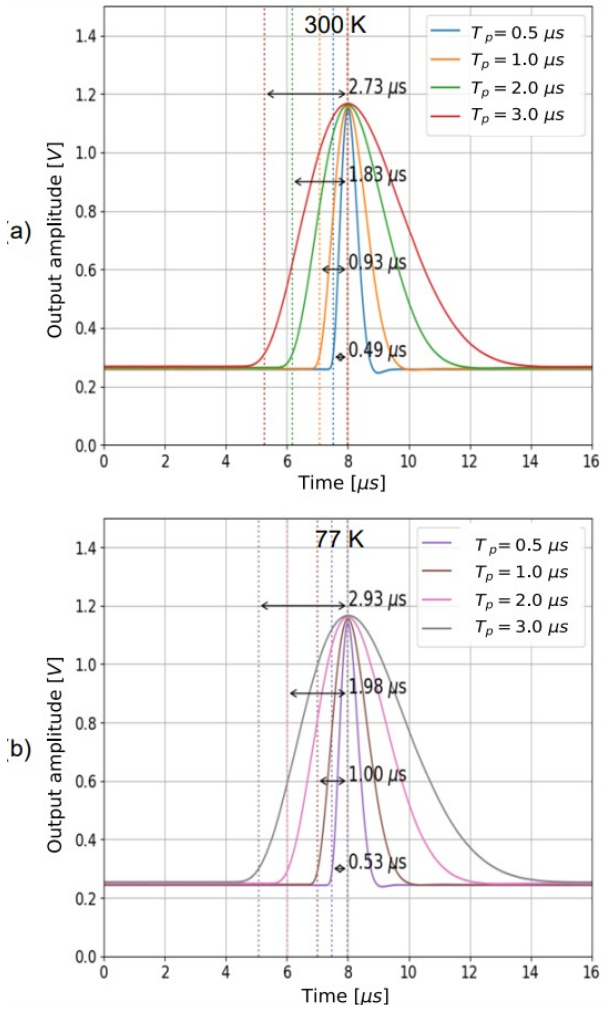


Measurement setup



Oscilloscope outputs at 77 K

- Test pulse charge inputs with programmable amplitudes provided either by on-chip 6-bit DAC or external source
- On-chip MiM capacitor calibrated to be 186 fF with less than 1% channel-to-channel dispersion at RT and LNT included in test input path
- Application of variable-amplitude voltage pulse injects known charge into the channel
- Full-scale range of DAC programmable based on gain setting
- **Very small deviations seen between RT and LNT in the measured peaking time and channel gain (< 2%)**



Measured peaking times

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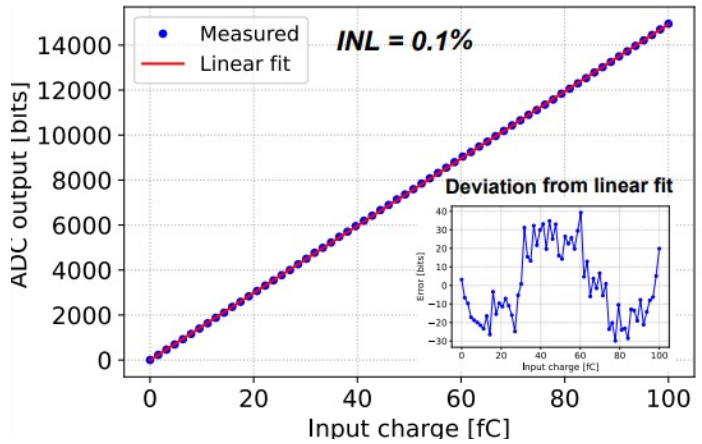
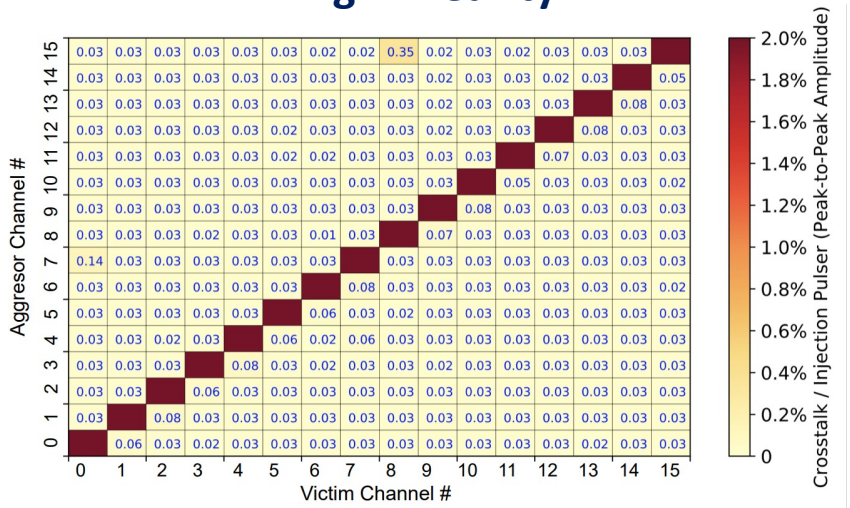
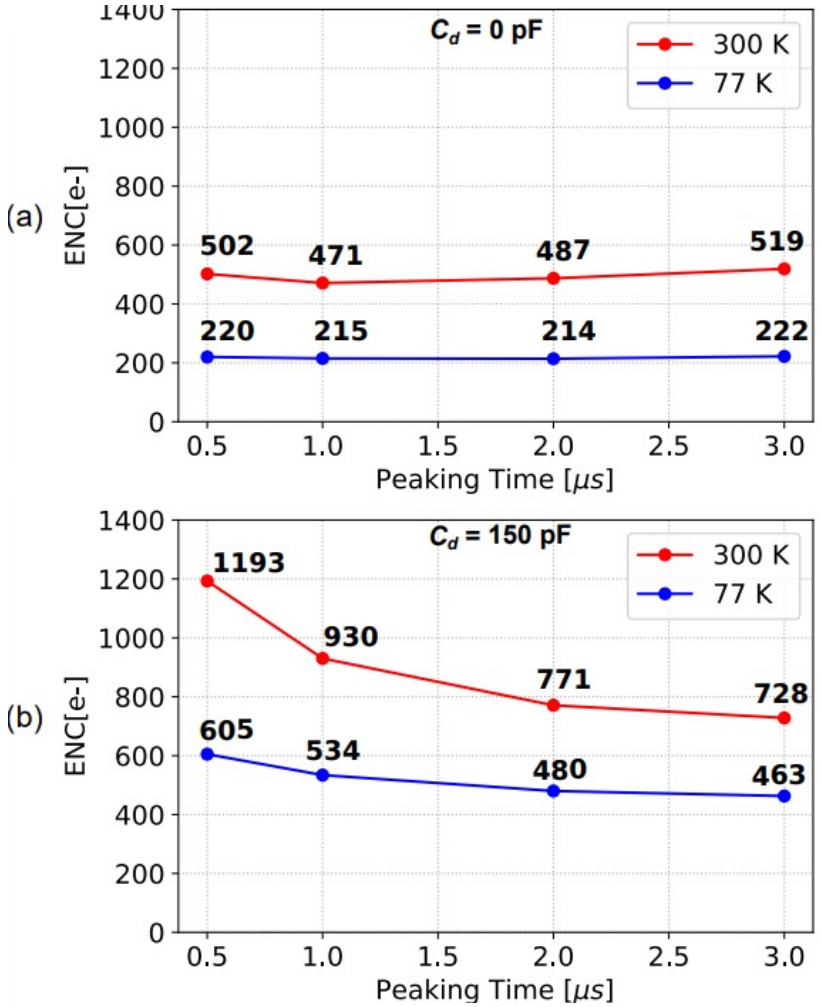
LArASIC measurement results [2]



High linearity



Low crosstalk (mean: 0.04%)



Low noise

Temperature	Baseline	Power consumption (mW)		
		Buffers off	SE on	SEDC on
300 K	200 mV	5.6	9.0	10.7
77 K	200 mV	5.3	8.8	10.8
300 K	900 mV	5.8	9.5	10.6
77 K	900 mV	5.5	9.1	10.5

Power consumption

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