

# Core Column Issue: Pixel Test

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# Pixel Level Issues

For chips with pixel-level issues, I have seen two types of issues:

## Threshold-Dependent Issue

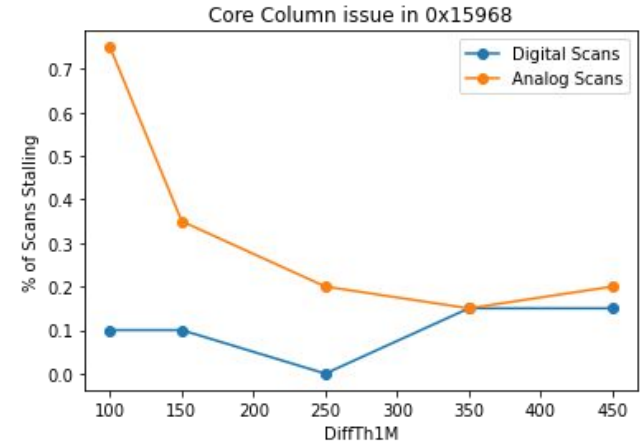
- Standard Analog and Digital scans **fail <100%** of the time, Analog scan failure rate depends on threshold
- **Can** send and read triggers when no pixels turned on in CC
- **Can** send and read triggers when all pixels turned on in CC

## Threshold-Independent Issue

- Standard Analog and Digital Scans in YARR **fail 100%** of the time, often at same mask loop
  - **Can** send and read triggers when no pixels turned on in CC
  - **Cannot** send and read triggers when all pixels turned on in CC
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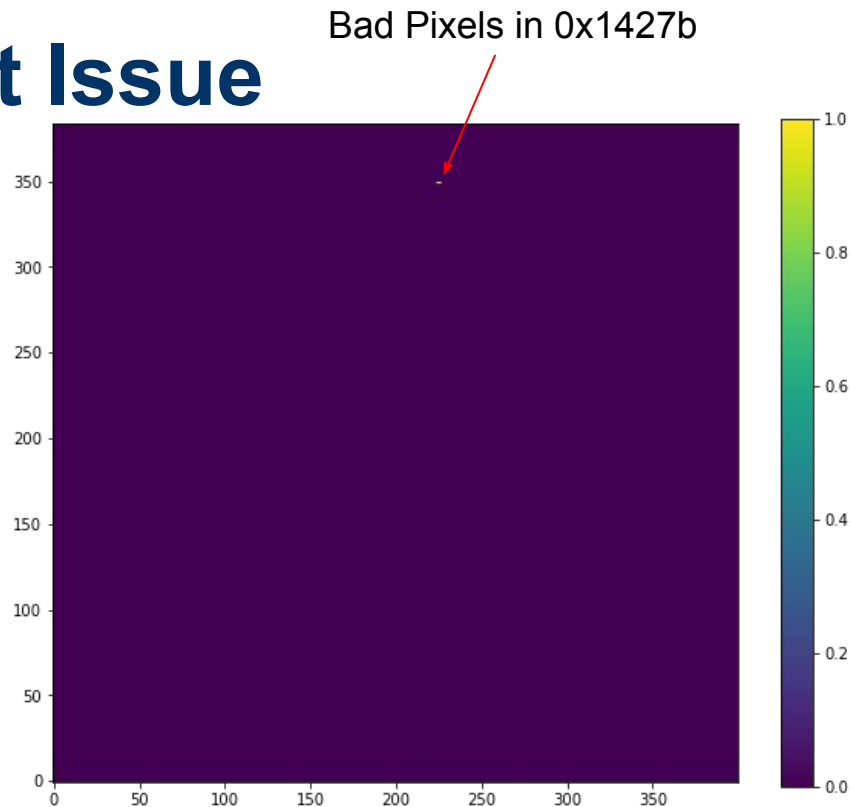
# Threshold-Dependent Issue

- Standard analog and digital scans (i.e. masking pixels and injecting charge into analog and digital parts of circuit) fail some % of the time
- The mask stage that scans fail at changes
- Analog scans fail more often than digital
- Analog scan failure rate increases as threshold lowers
- Current hypothesis: there are some number of noisy pixels. When enough fire or some hit pattern fires causes failure



# Threshold Independent Issue

- Standard analog and digital scans fail all of the time
- Can loop through pixels and identify ones where, when enabled and trigger is sent, no data is read back
- Procedure done in one chip, pixels in one memory cores (i.e. 4 pixels) are broken
  - I.e. when any of these pixels are enabled, can't read triggers
- Disabling these pixels manually in standard and digital scans allows scan to run
- Need to test on more chips, looks promising!



# Conclusion

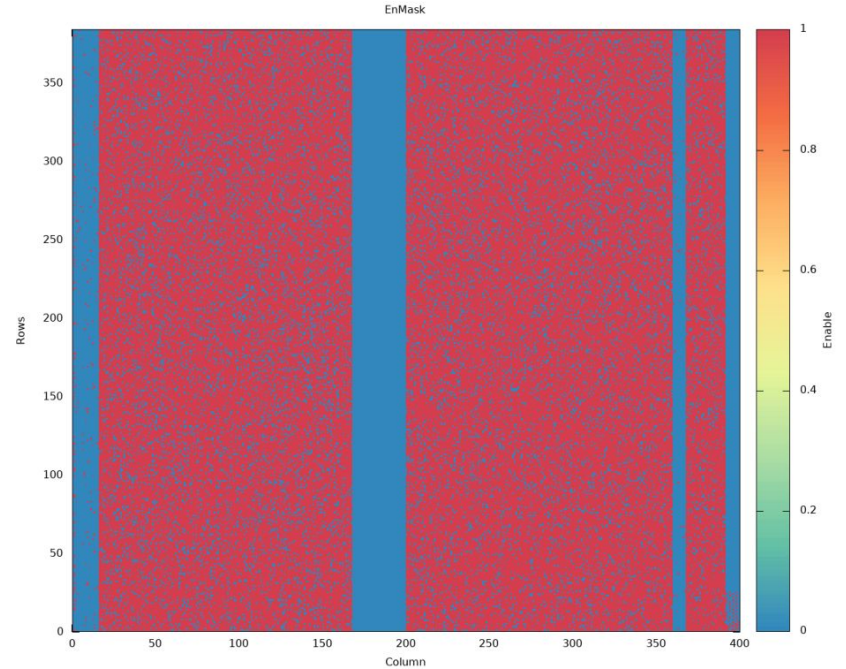
- Lots more data was taken to understand this issue, more needed still
  - Can make some changes to the way YARRR scans handle pixel masks to work around the “Bad Pixel Region Issue”
  - More investigation needed into the “Noisy Pixel Issue”
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**Backup**

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# Description of Issue

- Scans will fail in Yarr (DAQ SW) unless certain core columns are disabled in chip config
- We believe the issue manifests in two different ways:
  - Core Column issue: all pixels can be disabled within a core column, and still can't read data correctly from core column
  - Pixel issue: One (or a few) specific pixels can be disabled in the core column, and can communicate with core column
- Issue not seen in wafer probing - happens in dicing or some time after\*
- Not a DAQ issue \*

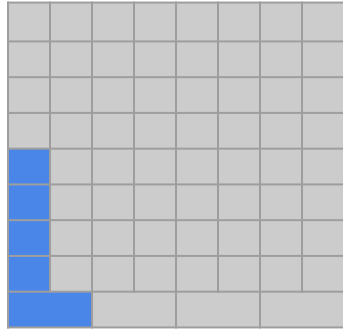


Ex: In ptot digital scan, columns ~160-200 need have the entire column broken, whereas other columns have some number of pixels that are broken





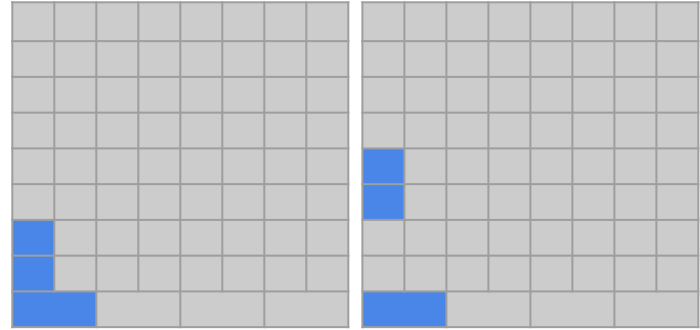
# Pixel Test Schematic



First stage in Pixel Scan

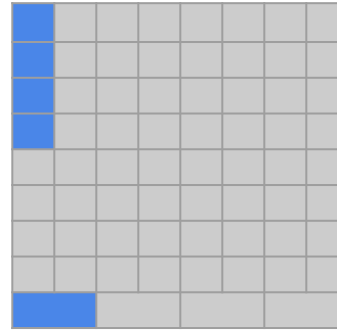
Are tags  
read the  
same as  
tags sent?

No



Next two stages in Pixel Scan

Yes



Next stage in Pixel Scan