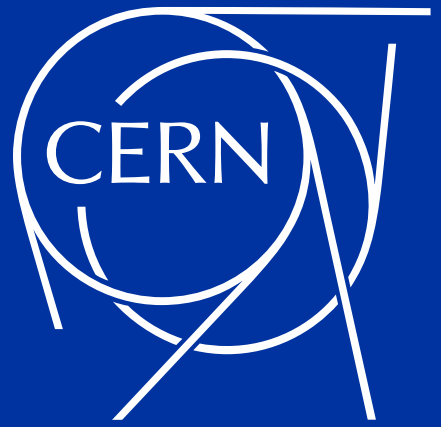

SoM specifications' review

(Manoel Barros Marin & Kiran Mushtaq Ahmed)

21/03/2024 – BI Technical Board

Outline

- Introduction
- SoM specifications
- Development status
- Summary & Outlook

Introduction

BI projects

- **New BI projects for LS3 (BGI, …) and LS4 (LHC BPM cons, …)**

BI projects

- **New BI projects for LS3 (BGI, …) and LS4 (LHC BPM cons, …)**
- **Need of a common solution to:**
  - Minimize: development time, cost, maintenance effort, …
  - Maximize: reliability, compatibility, optimization, …

BI projects

- **New BI projects for LS3 (BGI, …) and LS4 (LHC BPM cons, …)**
- **Need of a common solution to:**
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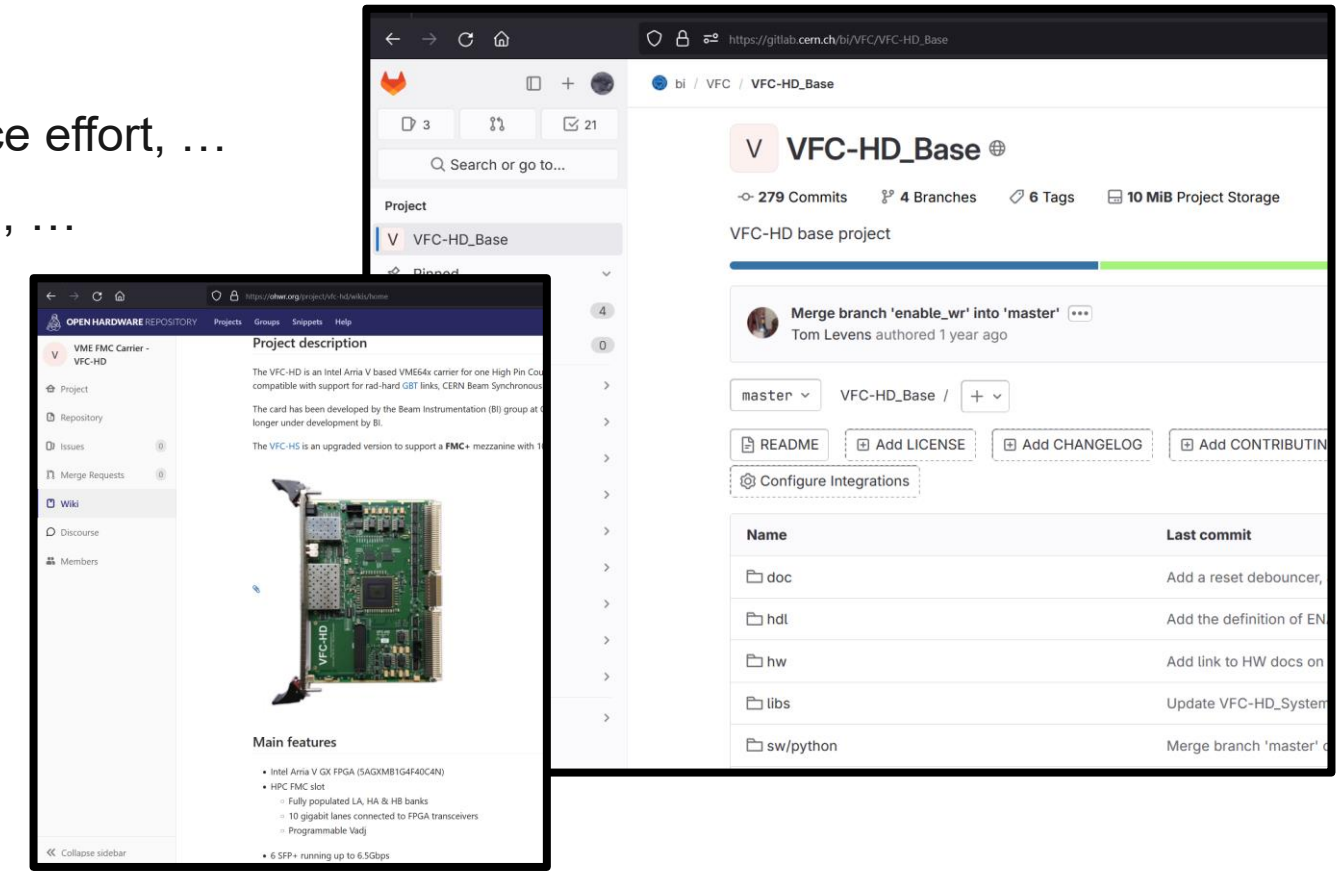
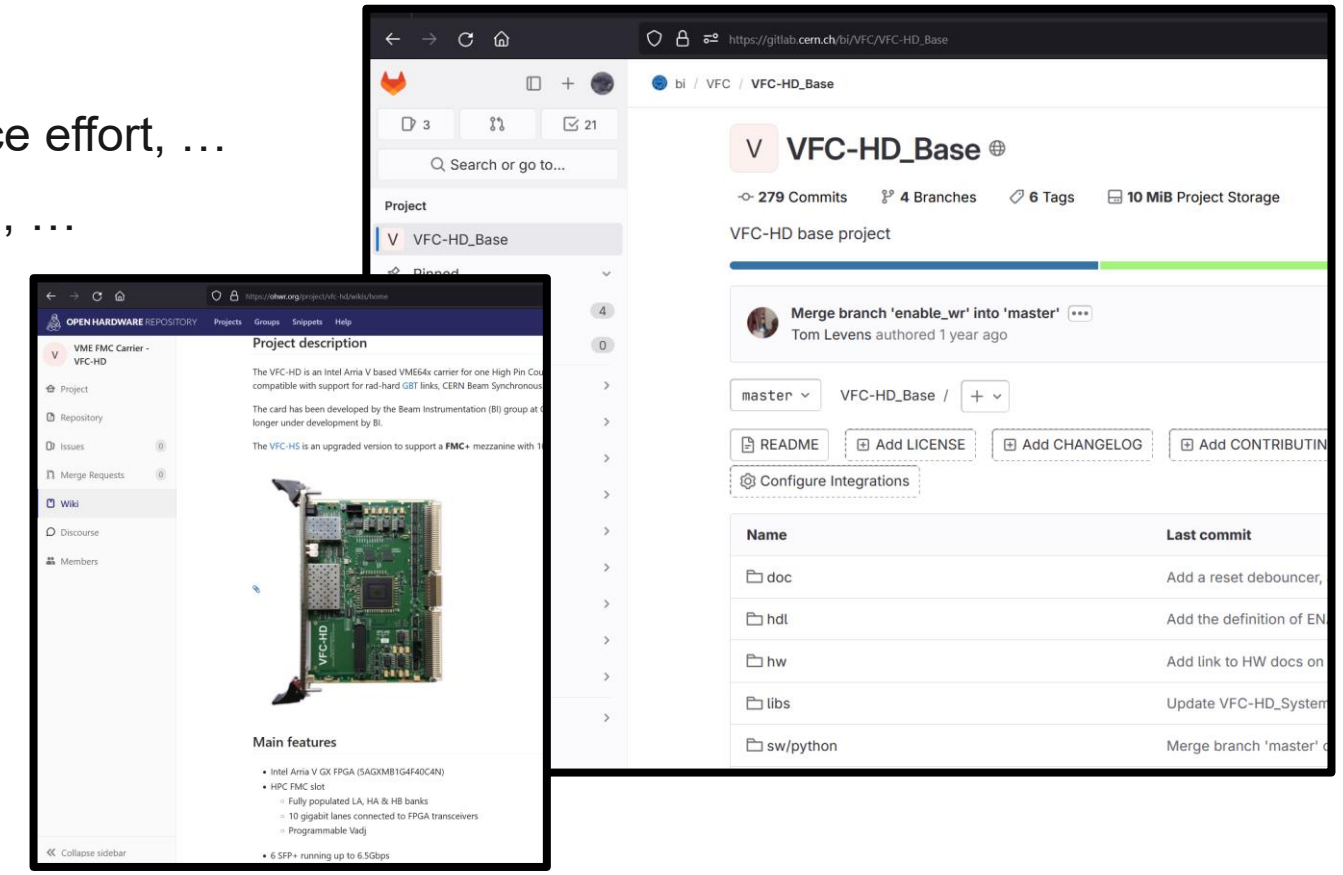
- **Following the example of the VFC-HD**



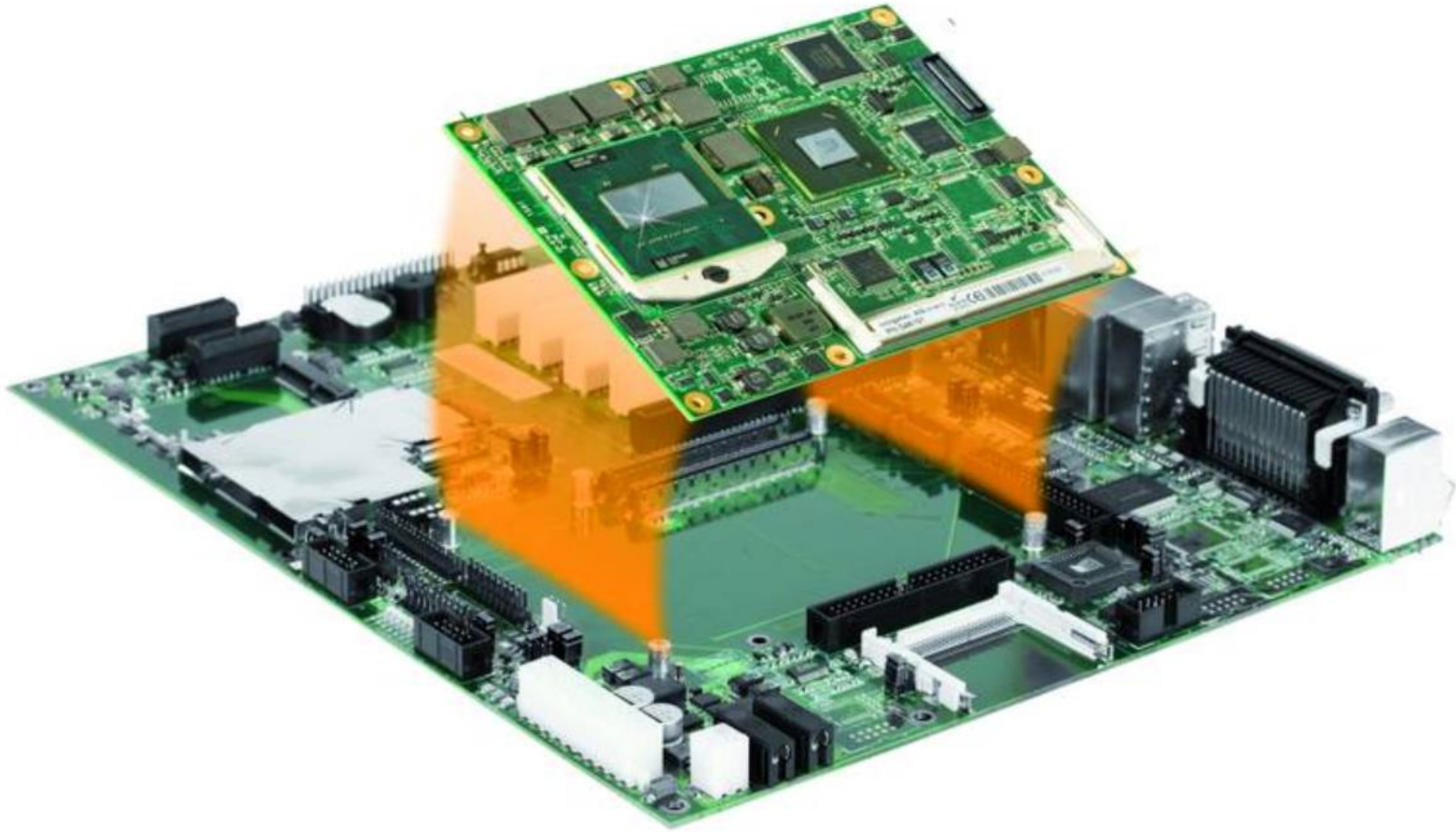
BI projects

- **New BI projects for LS3 (BGI, …) and LS4 (LHC BPM cons, …)**
- **Need of a common solution to:**
  - Minimize: development time, cost, maintenance effort, …
  - Maximize: reliability, compatibility, optimization, …
- **Following the example of the VFC-HD**

But more versatile



SoM



SoM specifications

Specifications from BI (and EPC)

System On Chip (SoC)

BI

	Parameter	Minimum	Preferred	Notes
Processing Sub-System PS	Device Family	AMD/Xilinx Zynq UltraScale+		
	Central Processor Family	A53		
	Central Processor Cores	4		
	Processor Core Clock	1.2GHz	1.3GHz	-3 not available for RFSoC
	Real Time Processor Family	-		TBD
	Graphics Processor Family	-		not required
	Clock (PS_REF_CLK)	33.3, 100 and 125 (MHz)		programmable
	Clock (PS_GTR_REFCLK)	125MHz ±20ppm		fixed or Tuneable: VCXO/DAC (i2C/SPI)
	External Memory	4GB		
	External Memory Type	DDR4		
	PS-GTR (6 Gbps)	TBD		
A-D	12-bit / 14-bit RF ADC	-		not required
	14-bit RF DAC	-		not required
Programmable Logic PL	12.5 Gb/s serial links	16 for DAQ + 2 Timing		GTH equivalent
	32.75 Gb/s serial links	-		not required (GTY equivalent)
	System Logic Cells	>500k		
	DSP Slices	>500		
	Clock (PL_CLK)	40 MHz, 125MHz ±controllable, Clock Synthesizer, BST Clock		Tuneable: VCXO/DAC (i2C/SPI)
	Internal Memory (Block / Ultra)	> 3MB		
	External Memory	>1GB		
	External Memory Type	DDR4		
	Flash Memory	>= 2 x Conf.		golden PL configuration, …
	Embedded Multimedia Card Size	4GB		LINUX + PL configurations, …

		System On Chip (SoC)					
		BI			EPC		
	Parameter	Minimum	Preferred	Notes	Minimum	Preferred	Notes
Processing Sub-System PS	Device Family	AMD/Xilinx Zynq UltraScale+			AMD/Xilinx Zynq UltraScale+		
	Central Processor Family	A53			A53		
	Central Processor Cores	4			4		
	Processor Core Clock	1.2GHz	1.3GHz	-3 not available for RFSoC	1.2GHz	1.3GHz	
	Real Time Processor Family	-		TBD	-		not required
	Graphics Processor Family	-		not required	-		not required
	Clock (PS_REF_CLK)	33.3, 100 and 125 (MHz)		programmable	50MHz ±20ppm		fixed
	Clock (PS_GTR_REFCLK)	125MHz ±20ppm		fixed or Tuneable: VCXO/DAC (i2C/SPI)	125MHz ±20ppm		fixed or Tuneable: VCXO/DAC (i2C/SPI)
	External Memory	4GB			4GB		
	External Memory Type	DDR4			DDR3	DDR4	
	PS-GTR (6 Gbps)	TBD					
A-D	12-bit / 14-bit RF ADC	-		not required	-		not required
	14-bit RF DAC	-		not required	-		not required
Programmable Logic PL	12.5 Gb/s serial links	16 for DAQ + 2 Timing		GTH equivalent	2		GTH equivalent
	32.75 Gb/s serial links	-		not required (GTY equivalent)	-		not required ()
	System Logic Cells	>500k			150k	250k	
	DSP Slices	>500			200	1200	
	Clock (PL_CLK)	40 MHz, 125MHz ±controllable, Clock Synthesizer, BST Clock		Tuneable: VCXO/DAC (i2C/SPI)	125MHz ±controllable		Tuneable: VCXO/DAC (i2C/SPI)
	Internal Memory (Block / Ultra)	> 3MB			0 to 2.5MB	6MB	internal + external must be ≥2.5MB
	External Memory	>1GB			0 to 2.5MB	-	internal + external must be ≥2.5MB
	External Memory Type	DDR4			SRAM	-	needed if internal RAM <2.5MB
	Flash Memory	>= 2 x Conf.		golden PL configuration, ...	1 x Conf.	3 x Conf.	golden PL configuration, ...
	Embedded Multimedia Card Size	4GB		LINUX + PL configurations, ...	4GB		LINUX + PL configurations, ...

Same requirements
TBD by BI
Different requirements

	Carrier Interface		
	BI		
Parameter	Minimum	Preferred	Notes
SoM VCC	5V		from carrier or SoM (SoM general power)
PS VCCIO	2.5V		from carrier or SoM (PS I/O power)
PL VCCIO	1.5V or 2.5V or 3.3V		from carrier or SoM (PL I/O power)
Power supply sequencing	un-sequenced		carrier does not sequence VCC-VCCIO
PS – I/O Pins to Carrier	TBD	TBD	In addition to: ≥1 x Debug UART ≥2 x SPI ≥4 x I2C ≥1 x S/RGMII for Ethernet PHY + if installed on carrier: 1 x PS_REF_CLK 1 x PS_GTR_REFCLK
PL – I/O Pins to Carrier	FMC Plus compatible (160 GPIO + 20 MGT + clocks + ctrl)	2 x FMC HPC compatible (2x (160 GPIO + 10 MGT + clocks + ctrl)	in addition to: 1 x JTAG port I/O + if installed on carrier: PL_CLKs

	Carrier Interface					
	BI			EPC		
Parameter	Minimum	Preferred	Notes	Minimum	Preferred	Notes
SoM VCC	5V		from carrier or SoM (SoM general power)	5V		from carrier (SoM general power)
PS VCCIO	2.5V		from carrier or SoM (PS I/O power)	2.5V		from carrier (PS I/O power)
PL VCCIO	1.5V or 2.5V or 3.3V		from carrier or SoM (PL I/O power)	1.5V or 2.5V or 3.3V		from carrier (PL I/O power)
Power supply sequencing	un-sequenced		carrier does not sequence VCC-VCCIO	un-sequenced		carrier does not sequence VCC-VCCIO
PS – I/O Pins to Carrier	TBD	TBD	In addition to: ≥1 x Debug UART ≥2 x SPI ≥4 x I2C ≥1 x S/RGMII for Ethernet PHY + if installed on carrier: 1 x PS_REF_CLK 1 x PS_GTR_REFCLK	≥46 (≥48)	≥54	In addition to: ≥1 x Debug UART ≥2 x SPI ≥4 x I2C ≥1 x S/RGMII for Ethernet PHY + if installed on carrier: 1 x PS_REF_CLK 1 x PS_GTR_REFCLK NB: DAC would use existing SPI/I2C
PL – I/O Pins to Carrier	FMC Plus compatible (160 GPIO + 20 MGT + clocks + ctrl)	2 x FMC HPC compatible (2x (160 GPIO + 10 MGT + clocks + ctrl)	in addition to: 1 x JTAG port I/O + if installed on carrier: PL_CLKs	≥150 (≥155)	≥290	in addition to: ≥2 x GTH link I/O 1 x JTAG port I/O + if installed on carrier: 1 x PL_CLK + DAC

Same requirements
TBD by BI
Different requirements

	Physical		
	BI		
Parameter	Application Baseline		Notes
Anticipated Power Dissipation	TBD		design objective
Anticipated Cooling Scheme	Natural or Forced Convection		passive heat sink OR heat sink + fan
Operation Environment Range	Commercial grade (0-85C)	Extended grade (0-100C)	
Installation Environment	Crate or Stand-alone		stationary, no vibration
Radiation Environment	Radiation-Free		surface level equivalent risks
Hot swap	-		no specific requirement
Dimensions	TBD		W x D x H
Mounting points	TBD		grounded stand-off mounts
Connector Type / Location	Separaded connectors for PS and PL		Ideally compatible with existing SoM

	Physical				
	BI			EPC	
Parameter	Application Baseline		Notes	Application Baseline	Notes
Anticipated Power Dissipation	TBD		design objective	50W	design objective
Anticipated Cooling Scheme	Natural or Forced Convection		passive heat sink OR heat sink + fan	Natural Convection	passive heat sink
Operation Environment Range	Commercial grade (0-85C)	Extended grade (0-100C)		0 – 55°	industrial temperature range
Installation Environment	Crate or Stand-alone		stationary, no vibration	Fixed: Rack/Chassis/Cassette	stationary, no vibration
Radiation Environment	Radiation-Free		surface level equivalent risks	Radiation-Free	surface level equivalent risks
Hot swap	-		no specific requirement	-	no specific requirement
Dimensions	TBD		W x D x H	≤(90mm x 90mm x 25mm)	W x D x H (see below)
Mounting points	TBD		grounded stand-off mounts	≥3	grounded stand-off mounts
Connector Type / Location	Separaded connectors for PS and PL		Ideally compatible with existing SoM	-	no specific requirement

Same requirements
TBD by BI
Different requirements

Combined specifications from BI/EPC

	Parameter	System On Chip (SoC)	
		BI	EPC
Processing Sub-System PS	Device Family	AMD/Xilinx Zynq UltraScale+	
	Clock (PS_REF_CLK)	50MHz ±20ppm (xtal) & Clock Synthesizer	
	Clock (PS_GTR_REFCLK)	125MHz ±20ppm (tuneable: VCXO/DAC (i2C/SPI))	
	External Memory	4GB	
	External Memory Type	DDR4	
	PS-GTR (6 Gbps)	TBD	
Programmable Logic PL	12.5 Gb/s serial links (GTH)	16 (DAQ) & >= 2 (Timing/Trigger/Control)	
	System Logic Cells	>500k	
	DSP Slices	>500	
	Clock (PL_CLK)	40 MHz, 125MHz ±controllable, Clock Synthesizer, BST Clock (tuneable: VCXO/DAC (i2C/SPI))	
	Internal Memory (Block / Ultra)	6MB (internal + external must be ≥2.5MB)	
	External Memory	>1GB (DDR4)	0 to 2.5MB (SRAM) (needed if internal RAM <2.5MB) (SoC (ZU17EG) features 7MB in BRAMs)
	Flash Memory	3 x Conf. (golden PL configuration, ...)	
	Embedded Multimedia Card Size	4GB (LINUX + PL configurations, ...)	

Same requirements
TBD by BI
Different requirements

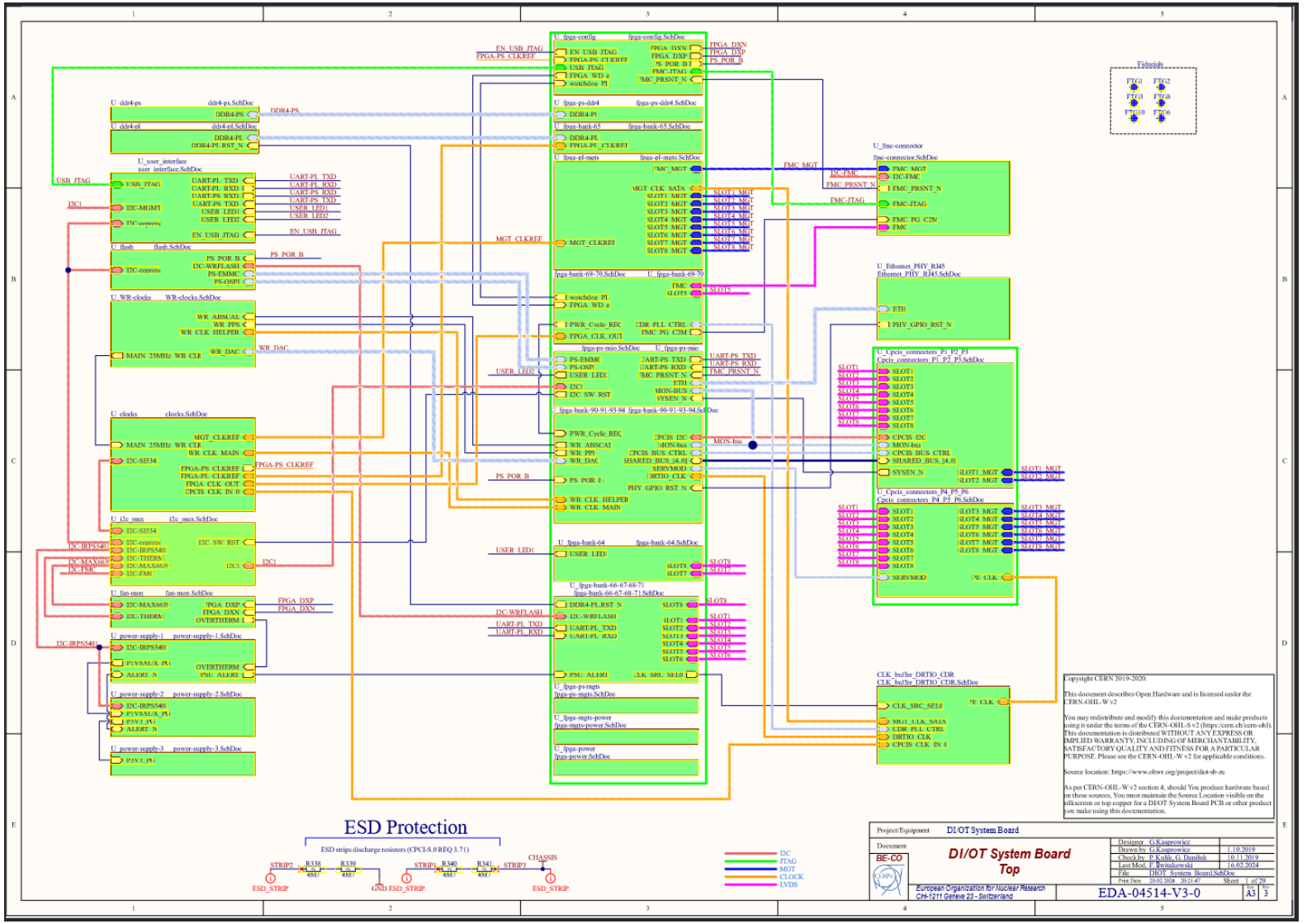
Parameter	Carrier Interface	
	BI	EPC
SoM VCC	5V (from carrier or SoM (SoM general power))	
PS VCCIO	2.5V (from carrier or SoM (PS I/O power))	
PL VCCIO	1.5V or 2.5V or 3.3V (from carrier or SoM (PL I/O power))	
Power supply sequencing	un-sequenced (carrier does not sequence VCC-VCCIO)	
PS – I/O Pins to Carrier	≥46 (min) ≥54 (preferred)	In addition to: ≥1 x Debug UART ≥2 x SPI ≥4 x I2C ≥1 x S/RGMII for Ethernet PHY + if installed on carrier: 1 x PS_REF_CLK 1 x PS_GTR_REFCLK NB: DAC would use existing SPI/I2C
PL – I/O Pins to Carrier	160 GPIO + clocks + ctrl (FMC Plus compatible) (2x FMC Plus compatible under study)	in addition to: 1 x JTAG port I/O + if installed on carrier: 1 x PL_CLK + DAC
PL-GTH/GTY	20 (40?)	

Same requirements
TBD by BI
Different requirements

	Physical	
Parameter	BI	EPC
Anticipated Power Dissipation	50W (design objective)	
Anticipated Cooling Scheme	Forced convection if needed (heatsink + fan)	
Operation Environment Range	Commercial grade (0-85C)	
Installation Environment	Crate or Stand-alone (stationary, no vibration)	
Radiation Environment	Radiation-Free (surface level equivalent risks)	
Hot swap	no specific requirement	
Dimensions	≤ (90mm x 90mm x 25mm) (W x D x H)	
Mounting points	≥ 3 (grounded stand-off mounts)	
Connector Type / Location	Ideally compatible with existing SoM	

Same requirements
TBD by BI
Different requirements

DIOT System board v3



Zynq® UltraScale+™ MPSoCs: EG Devices

		Device Name[1]	ZU1EG	ZU2EG	ZU3EG	ZU3TEG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.5GHz												
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB												
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 600MHz												
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core												
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz												
		Memory	L2 Cache 64KB												
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC												
		Static Memory Interfaces	NAND, 2x Quad-SPI												
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet												
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO												
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains												
		Security	RSA, AES, and SHA												
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor												
PS to PL Interface			12 x 32/64/128b AXI Ports												
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	157	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	37	47	71	72	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8[2]	2x Gen3x8[2]	-	1x Gen3x16 & 1x Gen3x8[3]	-	2x Gen3x16 & 2x Gen3x8[3]	-	3x Gen3x16 & 1x Gen3x8[3]	3x Gen3x16 & 2x Gen3x8[3]
		150G Interlaken	-	-	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	2	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	-	8	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[4]	-1 -2 -2L				-1 -2 -2L -3						-1 -2 -2L -3		
		Industrial	-1 -1L -2												

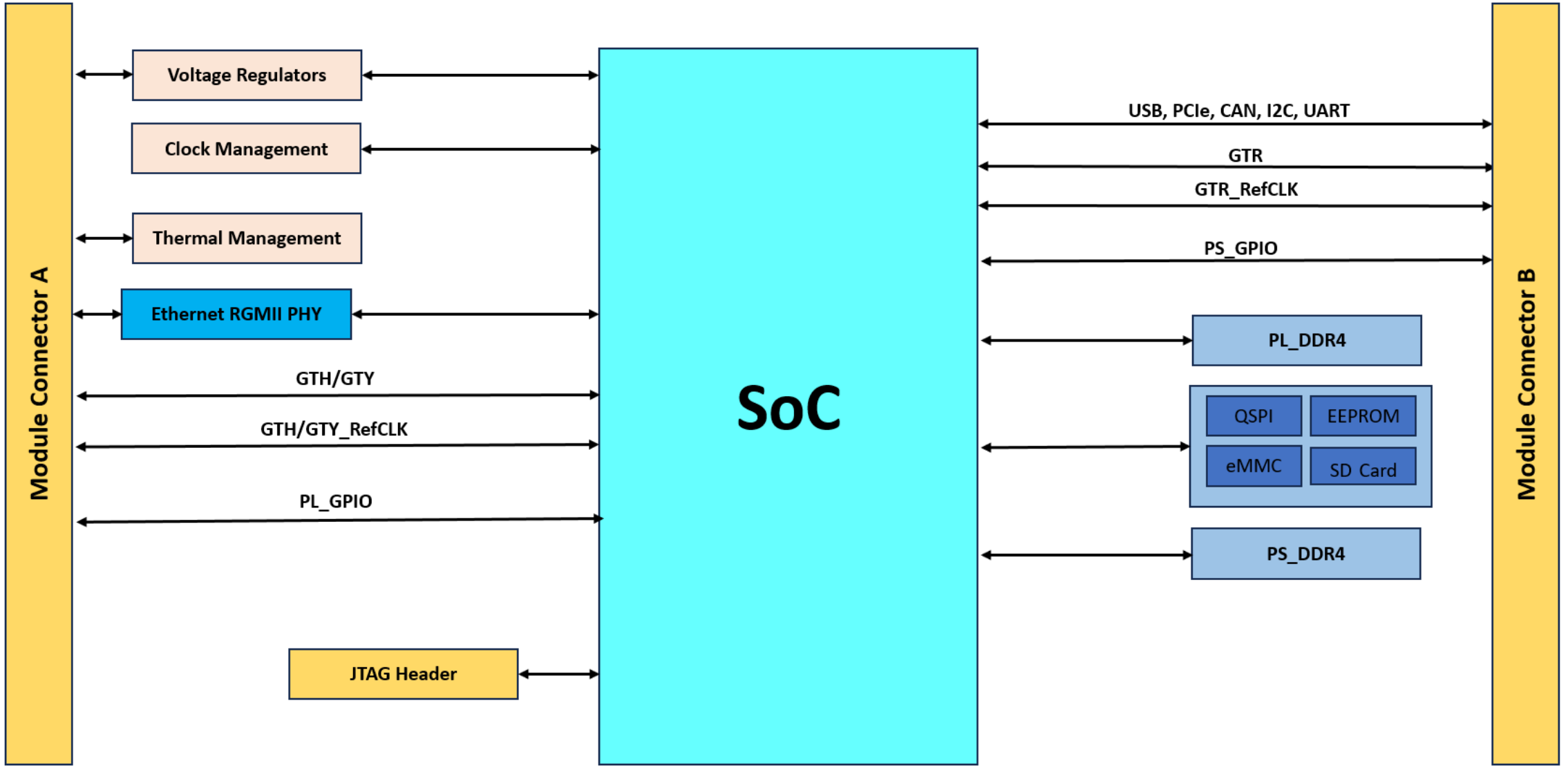
Zynq® UltraScale+™ MPSoCs

PS I/Os[1], 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os

PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 32.75Gb/s

Pkg Footprint[2,3]	Dimensions (mm)	Ball Pitch (mm)	ZU1	ZU2	ZU3	ZU3T	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
A484	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A494	9.5x15	0.5	170, 24, 58 4, 0, 0												
A530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A625	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0										
C784[4]	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 72, 52 4, 4, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
D784[4]	23x23	0.8				214, 72, 52 4, 8, 0									
B900	31x31	1.0					214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31	1.0							214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35	1.0							214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35	1.0								214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40	1.0										214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40	1.0								214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5	1.0										214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5	1.0												214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45	1.0												214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

SoM trends in the market



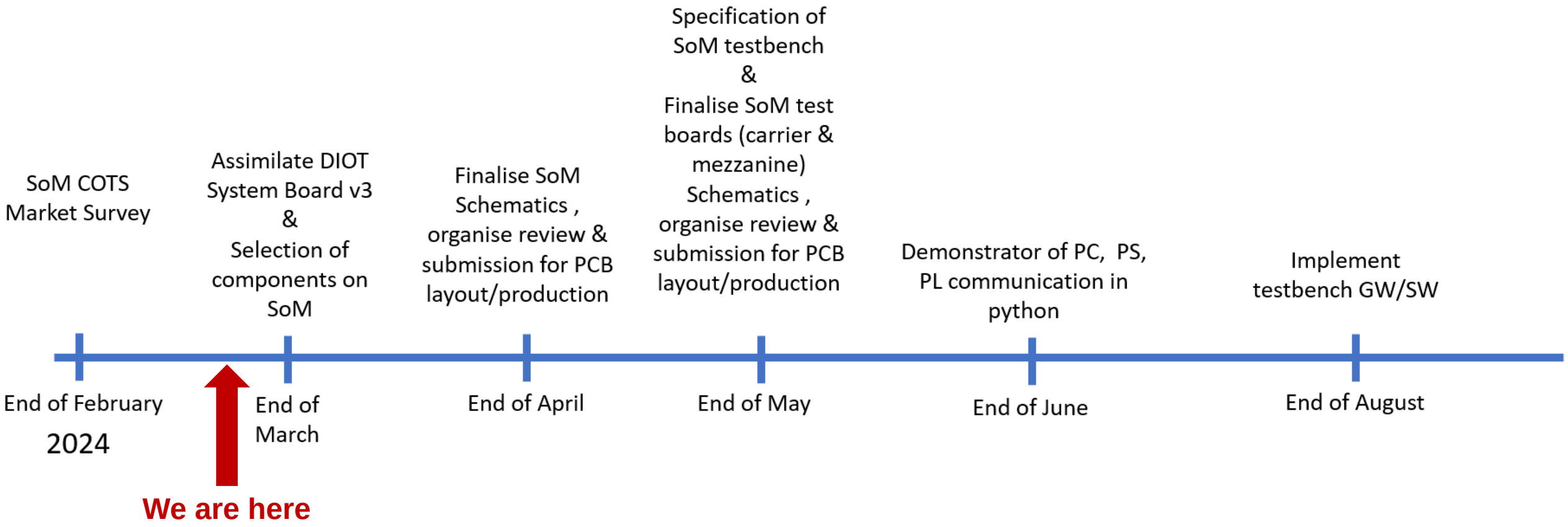
A General Hardware Block Diagram of System on Module

SoM	Connector		Form Factor
	Type	Height	
Avnet UltraZed EV Board	• 2x 200-pin: Samtec 0.8mm SEARAY Ultra-High Density Open-Pin-Field • 1x 120-pin: Samtec 0.8mm SEARAY Ultra-High Density Open-Pin-Field	7mm and 10mm	57.15mm x 101.6mm
i-Wave G30M	• 2x 240-pin: Samtec high speed ruggedized terminal strip connectors (QTH-120-01-L-D-A) • 14-pin JTAG header: Molex 877601416	5mm	95mm x 75mm
Enclustra Mercury+ XU8	3x 168-pin: Hirose FX10 0.5 mm pitch (FX10A-168S-SV, FX10A-168P-SV (71))	4mm and 5mm	74mm × 54mm
i-Wave G35M	• 2x 240-pin: Samtec high speed ruggedized terminal strip connectors (QTH-120-01-L-D-A) • 1x 240-pin: Samtec High-Speed High-Density connector (ADM6-60-01.5-L-4-2-A) • 1x 80-pin: Samtec High-Speed High-Density connector for interfaces expansion. (ADM6-20-01.5-L-4-2-A)	5 mm	110mm x 75mm
Enclustra Andormeda-XZU90	6x 240-pin: Samtec High-Speed High-Density connector (ADM6-60-01.5-L-4-2-A)	5 mm	80mm x 64mm
BI/EPC Requirements			TBD / ≤(90mm x 90mm x 25mm)

Development status

Timeline

SoM developed by BI/EPC (optimistic timeline)



SoM as part of the DIOT ecosystem

- **Ideal solution for BI:**
  - SoM supported by CEM (HW, GW & SW)
  - Potential interest at ATS level (maximizing synergies)
  - BI may provide resources for the development (e.g. manpower)
- **Conversations with CEM ongoing**
- **If agreed, timeline and work distribution still to be defined**

Summary & Outlook

Summary

BI projects need next-gen back-end for LS3 & LS4

- VFC-HD was as successful approach but with rigid form-factor
- SoM would increase flexibility

Similar SoM requirements for BI & EPC

SoM based on DIOT System Board V3 under development (very early stage)

SoM as part of DIOT ecosystem would be ideal for BI

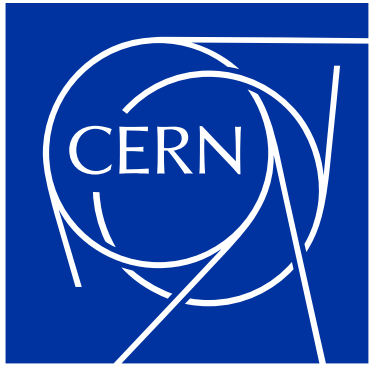
- SoM supported by CEM (HW, GW & SW)
- BI may provide resources for the development (e.g. manpower)
- Discussion with CEM ongoing

Outlook

Try to find an agreement with CEM to adopt SoM as part of the DIOT ecosystem

- Define timeline and work distribution
- Define scope of the project (group or sector level)

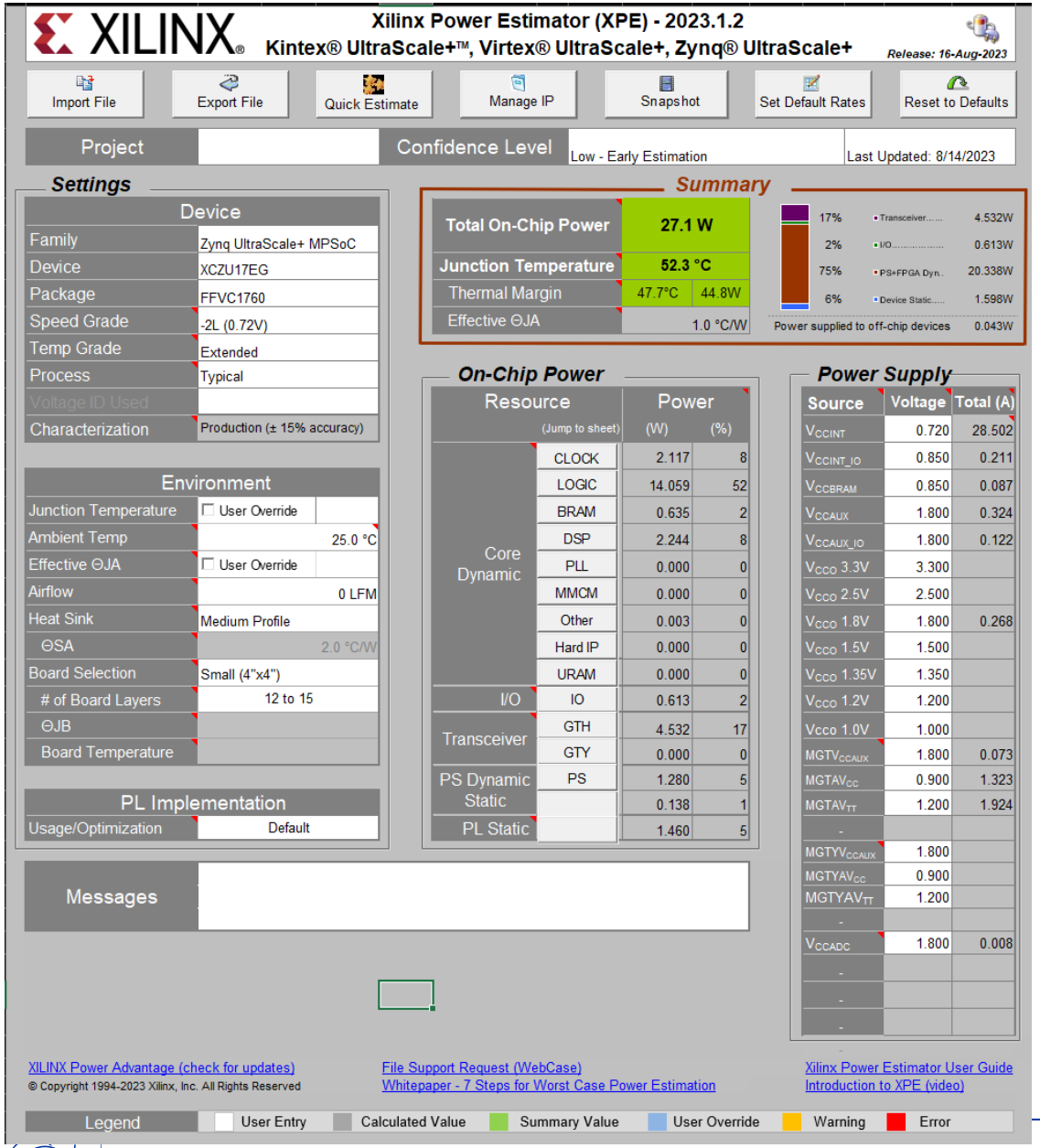
Otherwise continue with the SoM development as planned



Contact: manoel.barros.marin@cern.ch

home.cern

BI



XILINX

Xilinx Power Estimator (XPE) - 2023.1.2

Kintex® UltraScale+™, Virtex® UltraScale+, Zynq® UltraScale+

Release: 16-Aug-2023

Import File | Export File | Quick Estimate | Manage IP | Snapshot | Set Default Rates | Reset to Defaults

Project | Confidence Level: Low - Early Estimation | Last Updated: 8/14/2023

Settings

Device	
Family	Zynq UltraScale+ MPSoC
Device	XCZU17EG
Package	FFVC1760
Speed Grade	-2L (0.72V)
Temp Grade	Extended
Process	Typical
Voltage ID Used	
Characterization	Production (± 15% accuracy)

Environment		
Junction Temperature	☐ User Override	
Ambient Temp		25.0 °C
Effective ΘJA	☐ User Override	
Airflow		0 LFM
Heat Sink		Medium Profile
ΘSA		2.0 °C/W
Board Selection		Small (4"x4")
# of Board Layers		12 to 15
ΘJB		
Board Temperature		

PL Implementation	
Usage/Optimization	Default

Summary

Total On-Chip Power	27.1 W	
Junction Temperature	52.3 °C	
Thermal Margin	47.7°C	44.8W
Effective ΘJA	1.0 °C/W	

17%	Transceiver.....	4.532W
2%	I/O.....	0.613W
75%	PS+FPGA Dyn..	20.338W
6%	Device Static.....	1.598W
Power supplied to off-chip devices		0.043W

On-Chip Power

Resource		Power (W)	Power (%)
Core Dynamic	CLOCK	2.117	8
	LOGIC	14.059	52
	BRAM	0.635	2
	DSP	2.244	8
	PLL	0.000	0
	MMCM	0.000	0
	Other	0.003	0
	Hard IP	0.000	0
	URAM	0.000	0
I/O	IO	0.613	2
Transceiver	GTH	4.532	17
	GTY	0.000	0
PS Dynamic Static	PS	1.280	5
		0.138	1
PL Static		1.460	5

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	0.720	28.502
V_{CCINT_IO}	0.850	0.211
V_{CCBRAM}	0.850	0.087
V_{CCAUX}	1.800	0.324
V_{CCAUX_IO}	1.800	0.122
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	0.268
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
V_{CCO} 1.0V	1.000	
$MGTV_{CCAUX}$	1.800	0.073
$MGTAV_{CC}$	0.900	1.323
$MGTAV_{TT}$	1.200	1.924
-		
$MGTYV_{CCAUX}$	1.800	
$MGTYAV_{CC}$	0.900	
$MGTYAV_{TT}$	1.200	
-		
V_{CCADC}	1.800	0.008
-		
-		
-		

Messages

XILINX Power Advantage (check for updates)

File Support Request (WebCase)

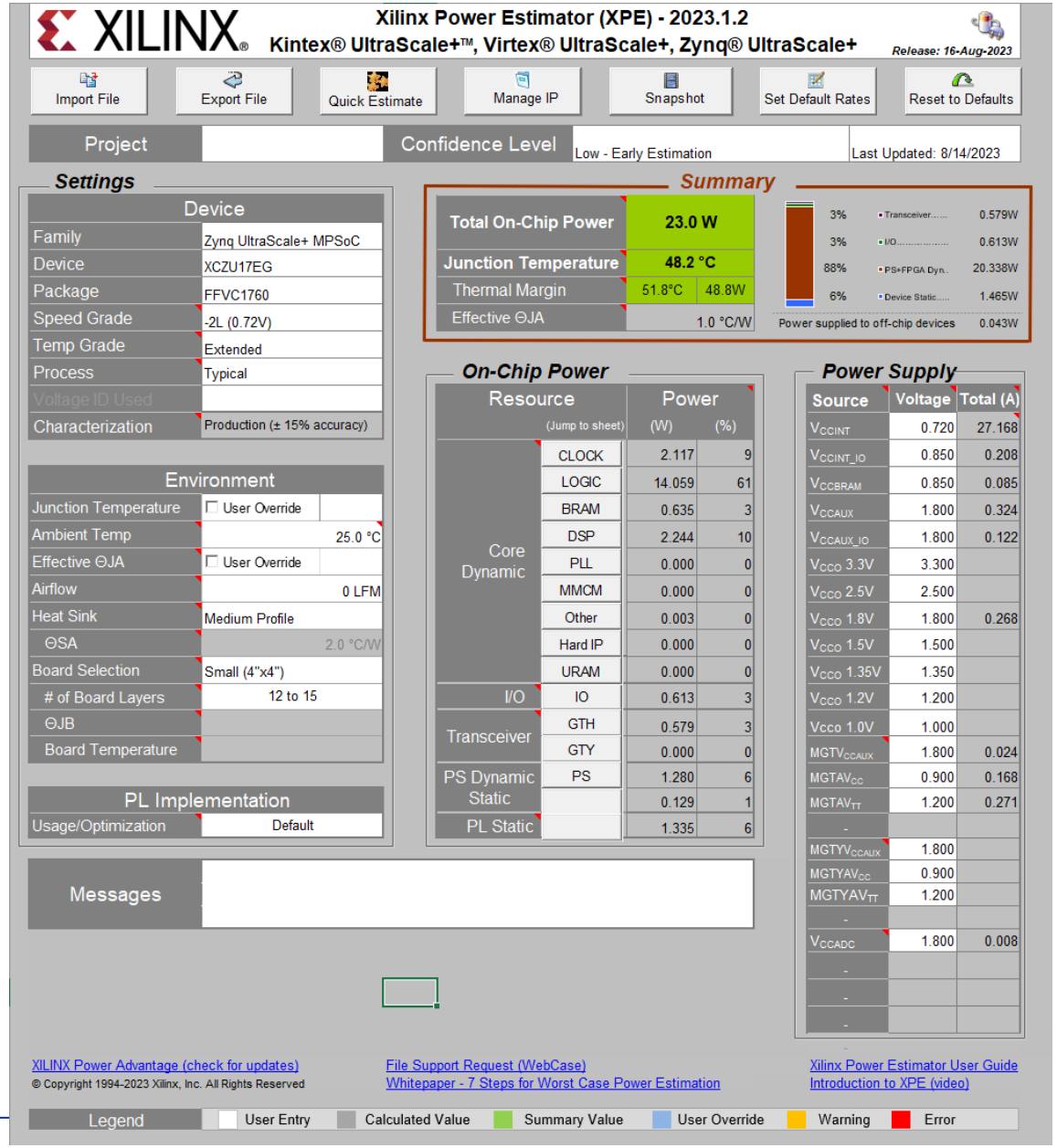
Whitepaper - 7 Steps for Worst Case Power Estimation

Xilinx Power Estimator User Guide

Introduction to XPE (video)

Legend: User Entry | Calculated Value | Summary Value | User Override | Warning | Error

EPC



XILINX

Xilinx Power Estimator (XPE) - 2023.1.2

Kintex® UltraScale+™, Virtex® UltraScale+, Zynq® UltraScale+

Release: 16-Aug-2023

Import File | Export File | Quick Estimate | Manage IP | Snapshot | Set Default Rates | Reset to Defaults

Project | Confidence Level: Low - Early Estimation | Last Updated: 8/14/2023

Settings

Device	
Family	Zynq UltraScale+ MPSoC
Device	XCZU17EG
Package	FFVC1760
Speed Grade	-2L (0.72V)
Temp Grade	Extended
Process	Typical
Voltage ID Used	
Characterization	Production (± 15% accuracy)

Environment		
Junction Temperature	☐ User Override	
Ambient Temp		25.0 °C
Effective ΘJA	☐ User Override	
Airflow		0 LFM
Heat Sink		Medium Profile
ΘSA		2.0 °C/W
Board Selection		Small (4"x4")
# of Board Layers		12 to 15
ΘJB		
Board Temperature		

PL Implementation	
Usage/Optimization	Default

Summary

Total On-Chip Power	23.0 W	
Junction Temperature	48.2 °C	
Thermal Margin	51.8°C	48.8W
Effective ΘJA	1.0 °C/W	

3%	Transceiver.....	0.579W
3%	I/O.....	0.613W
88%	PS+FPGA Dyn..	20.338W
6%	Device Static.....	1.465W
Power supplied to off-chip devices		0.043W

On-Chip Power

Resource		Power (W)	Power (%)
Core Dynamic	CLOCK	2.117	9
	LOGIC	14.059	61
	BRAM	0.635	3
	DSP	2.244	10
	PLL	0.000	0
	MMCM	0.000	0
	Other	0.003	0
	Hard IP	0.000	0
	URAM	0.000	0
I/O	IO	0.613	3
Transceiver	GTH	0.579	3
	GTY	0.000	0
PS Dynamic Static	PS	1.280	6
		0.129	1
PL Static		1.335	6

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	0.720	27.168
V_{CCINT_IO}	0.850	0.208
V_{CCBRAM}	0.850	0.085
V_{CCAUX}	1.800	0.324
V_{CCAUX_IO}	1.800	0.122
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	0.268
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
V_{CCO} 1.0V	1.000	
$MGTV_{CCAUX}$	1.800	0.024
$MGTAV_{CC}$	0.900	0.168
$MGTAV_{TT}$	1.200	0.271
-		
$MGTYV_{CCAUX}$	1.800	
$MGTYAV_{CC}$	0.900	
$MGTYAV_{TT}$	1.200	
-		
V_{CCADC}	1.800	0.008
-		
-		
-		

Messages

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