EP R&D Days
WP1.1 Silicon Hybrid Detector

Victor Coco, Paula Collins, **Morag Williams** (WP1.1 GRAP), Federico de Bennedetti (WP1.1 DOCT), Heinrich Schindler, Viros Sriskaran (WP1.1 FELL), Raphael Dumps, Wiktor Byczinski.
…. and a big thanks to collaborating institutes PSI, Nikhef, CNM, IGFAE-USC, CPPM, University of Oxford, …

Motivations

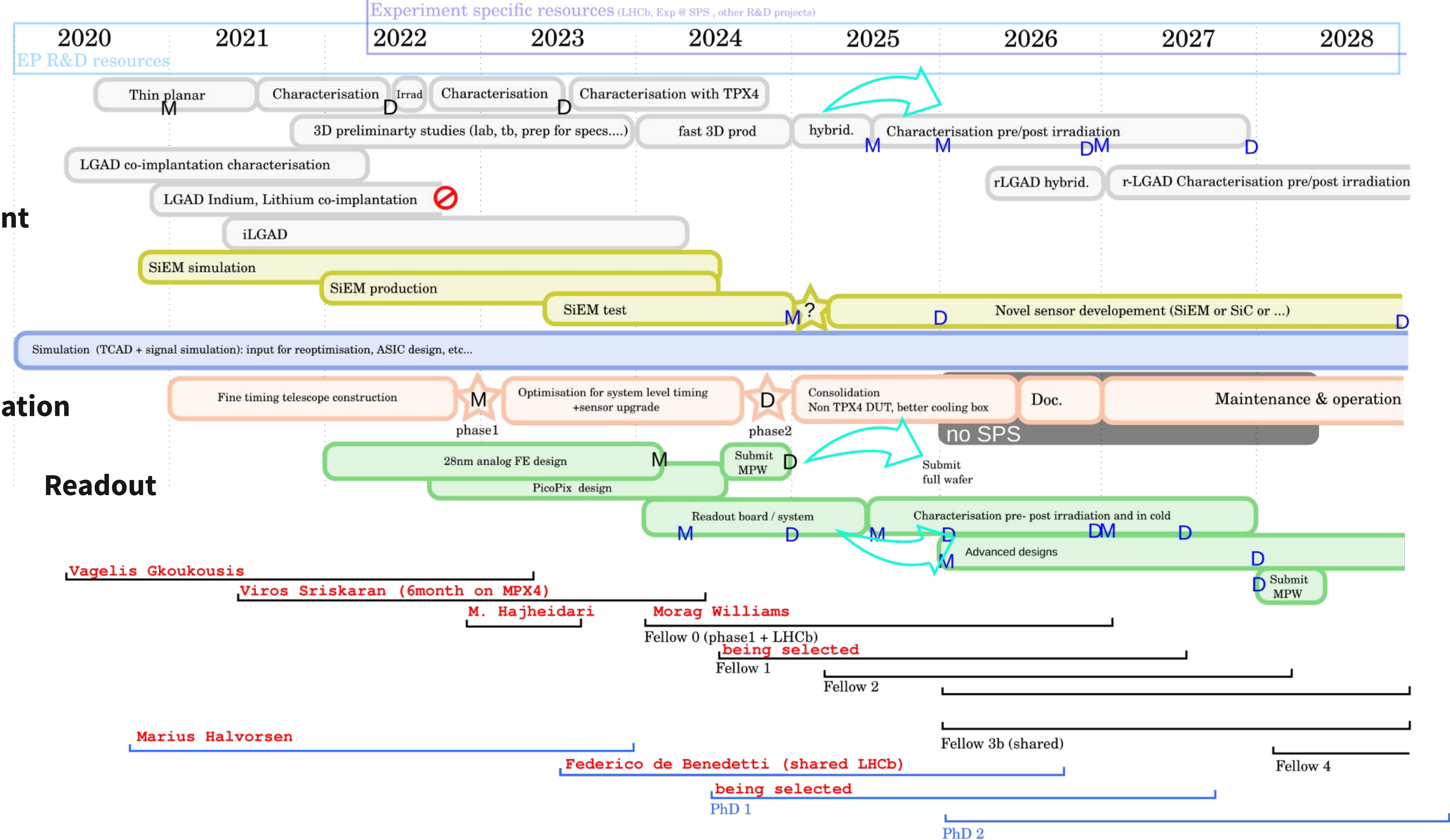
MIP detection in next generation of collider experiments

from the CERN Strategic R&D Programme on Technologies for Future Experiments [CERN-OPEN-2018-006]

[fineprint in CERN-OPEN-2018-006]	**HL-LHC**	**SPS**	**FCC-ee**	**FCC-hh**
Total fluence [$n_{eq} cm^{-2} s^{-1}$]	$5x10^{16}$	10^{17}	10^{10}	10^{17}
Max Hit rate [$cm^{-2} s^{-1}$]	2-4G	8G	20M	20G
Material budget per layer [X_0]	0.1-2%	2%	0.3%	1%
Pixel size [μm^2] inner trackers	50x50	50x50	25x25	25x25
Temporal hit resolution [ps] inner trackers	~50	~40	-	~10

- **Time resolution 10 - 50 ps**
- **Pixel pitches down to 25 µm**
- **Fluences up to 10^{17} $n_{eq}/cm^2/y$**
- **Max hit rate up 20 $G/cm^2/s$**

Challenges for sensor
Challenges for front-end electronics



Experiment specific resources (LHCb, Exp @ SPS , other R&D projects)

2020 2021 2022 2023 2024 2025 2026 2027 2028

EP R&D resources

Sensor development

Thin planar M

Characterisation D

Irrad

Characterisation D

Characterisation with TPX4

3D preliminarty studies (lab, tb, prep for specs....)

fast 3D prod

hybrid. M

Characterisation pre/post irradiation M DM D

LGAD co-implantation characterisation

LGAD Indium, Lithium co-implantation 🚫

rLGAD hybrid.

r-LGAD Characterisation pre/post irradiation

iLGAD

SiEM simulation

SiEM production

SiEM test M

?

Novel sensor developement (SiEM or SiC or ...) D D

Simulation and characterisation

Simulation (TCAD + signal simulation): input for reoptimisation, ASIC design, etc...

Fine timing telescope construction

M phase1

Optimisation for system level timing +sensor upgrade

D phase2

Consolidation
Non TPX4 DUT, better cooling box

Doc.

Maintenance & operation

no SPS

Readout

28nm analog FE design M

PicoPix design

Submit MPW D

Submit full wafer

Readout board / system M D

Characterisation pre- post irradiation and in cold M D DM D

Advanced designs M D

D Submit MPW

Vagelis Gkoukousis

Viros Sriskaran (6month on MPX4)

M. Hajheidari

Morag Williams

Fellow 0 (phase1 + LHCb)

being selected

Fellow 1

Fellow 2

Fellow 3b (shared)

Fellow 4

Marius Halvorsen

Federico de Benedetti (shared LHCb)

being selected

PhD 1

PhD 2

Evolution since proposal of phase 2

- **The readout part of the project relies on the development of 28 nm IC for fast timing (σ_t~30 ps) and small pitch (~50 µm)**
- **Thanks to collaboration with EP-ESE, EP-LBD, WP 5 and 6, the FE readout part of the project has progressed and evolved since the start of phase 1:**
  - Originally planned small MPW on block design of analog FE and later TDC
  - Then "small" 64x64 pixel full featured ASIC but still based on MPW

  } only based on EP R&D WP1.1 funds

  - Now considering large array fully featured ASIC
- **Has impact on the overall project schedule**
  - MPW version had planned submission Q2 2024
  - Full wafer version submission is planned end of 2025
  - Activities that were planning to use sensor bonded to readout get pushed-back too

    ⇒ mitigated by performing studies based on Timepix4
- **Overall better scientific output expected and much more useful for the R&D community beyond CERN**

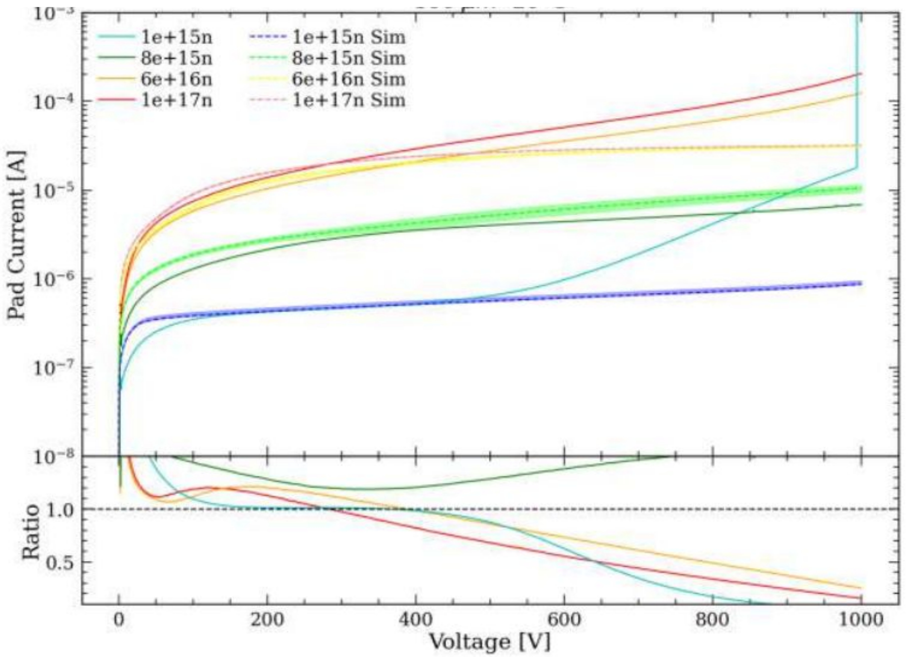
Planar sensors characterisation

- **Production from beginning of phase 1:**
  - Various thicknesses (50, 100, 200 and 300 µm)
  - Various form factors : test structures, full sensors: TPX3, TPX4, TDCpix
  - Irradiation campaign : neutron (JSI) up to 10^{17} and proton (IRRAD) up to $8 \times 10^{16}\,n_{eq}cm^{-2}$

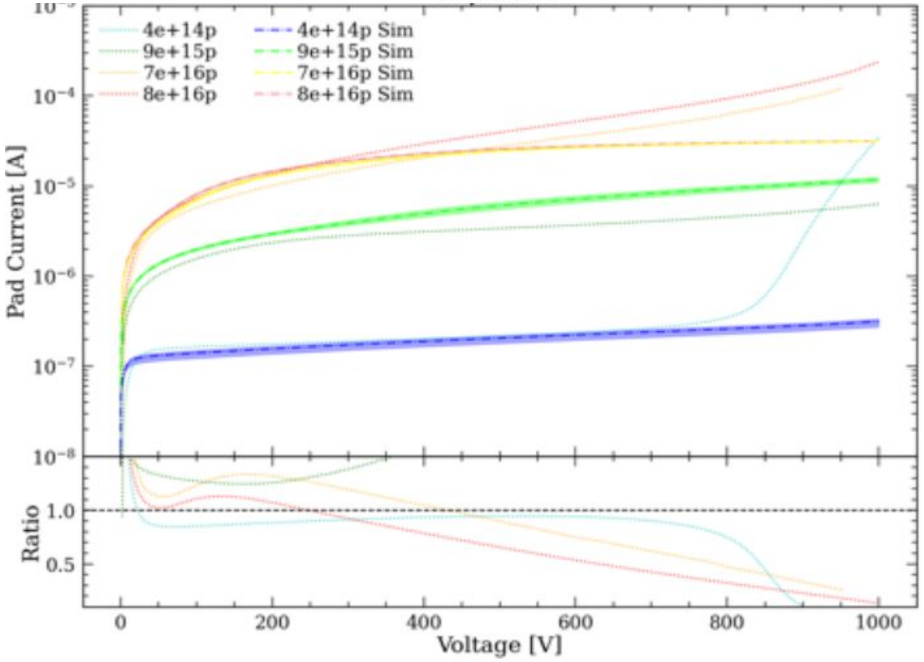
- **Various measurements and simulations to understand that production:**
  - SIMS to measure the doping
  - IV, CV, TCAD simulations to understand their behaviour
  - Simulation including radiation effects
  - Testbeam campaign to measure signal characteristic
    - CCE
    - timing behaviour

All studies are documented in J. Haimberger's thesis

IV of 100um neutron irradiated diodes



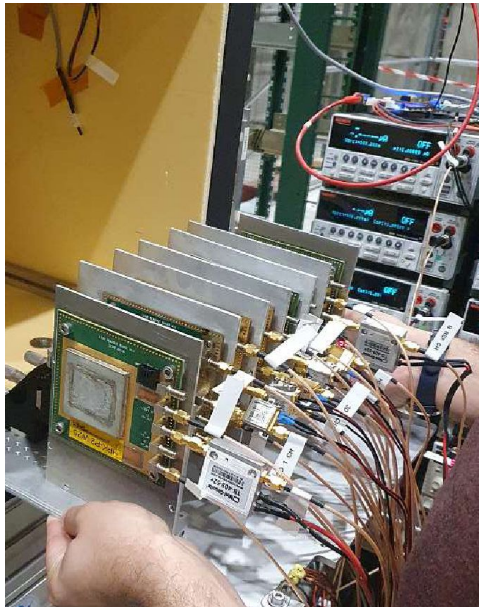
IV of 100um proton irradiated diodes



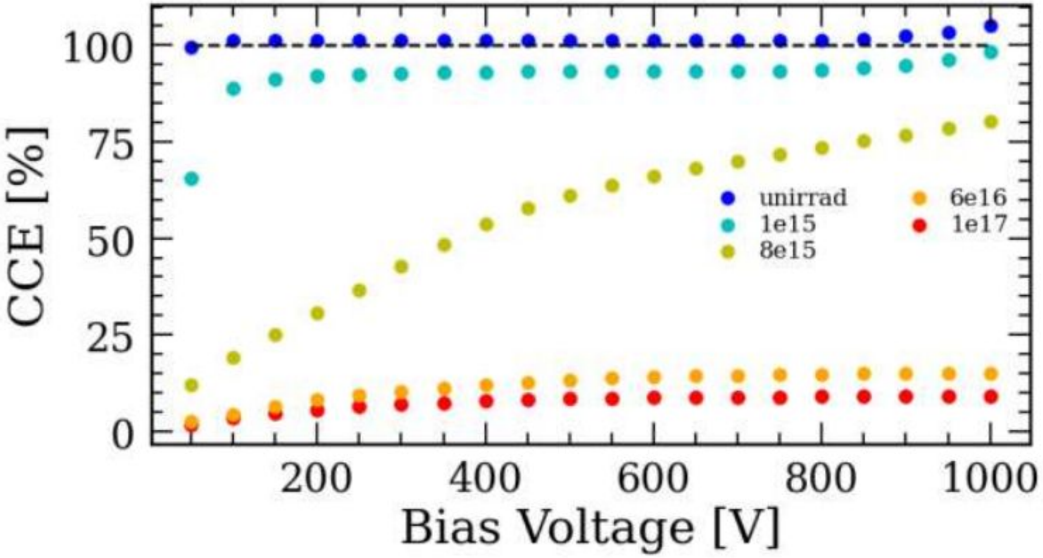
Planar sensors characterisation

- **Collected charge significantly reduced at high radiation.**
  - Trapping distances estimated at ~10-20 µm
  - At highest irradiation, collected charge roughly independent of sensor thickness
- **Signal shape remains good but signal amplitude is likely too low**
  - To be exploited in IC sensor with good time resolution needs low capacitance AND high collected charges
  - Planar sensor at the edge of usable timing capabilities when irradiated ⇒ likely insufficient for 4D tracking at $10^{17} n_{eq} cm^{-2}$
  - Study with pads, does not account for effect of pixelation on timing performances

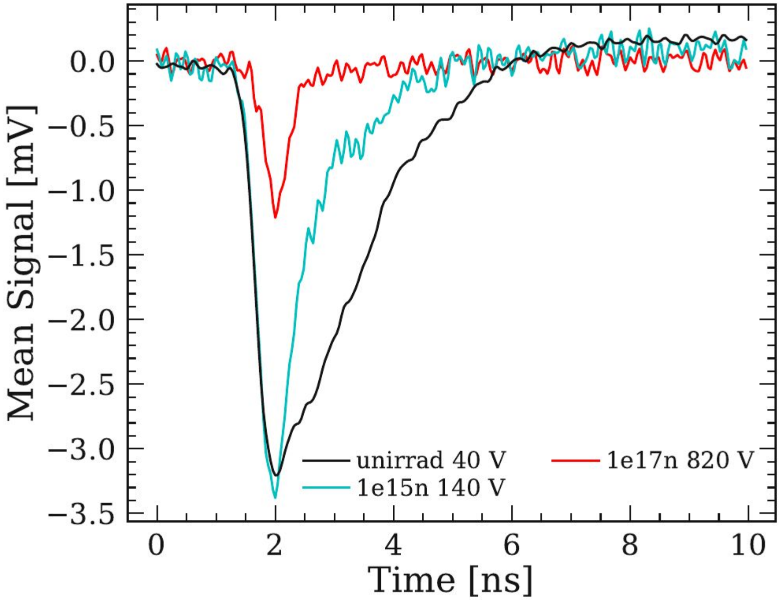
Test beam setup @ SPS



Simulated CCE for 100 µm sensor



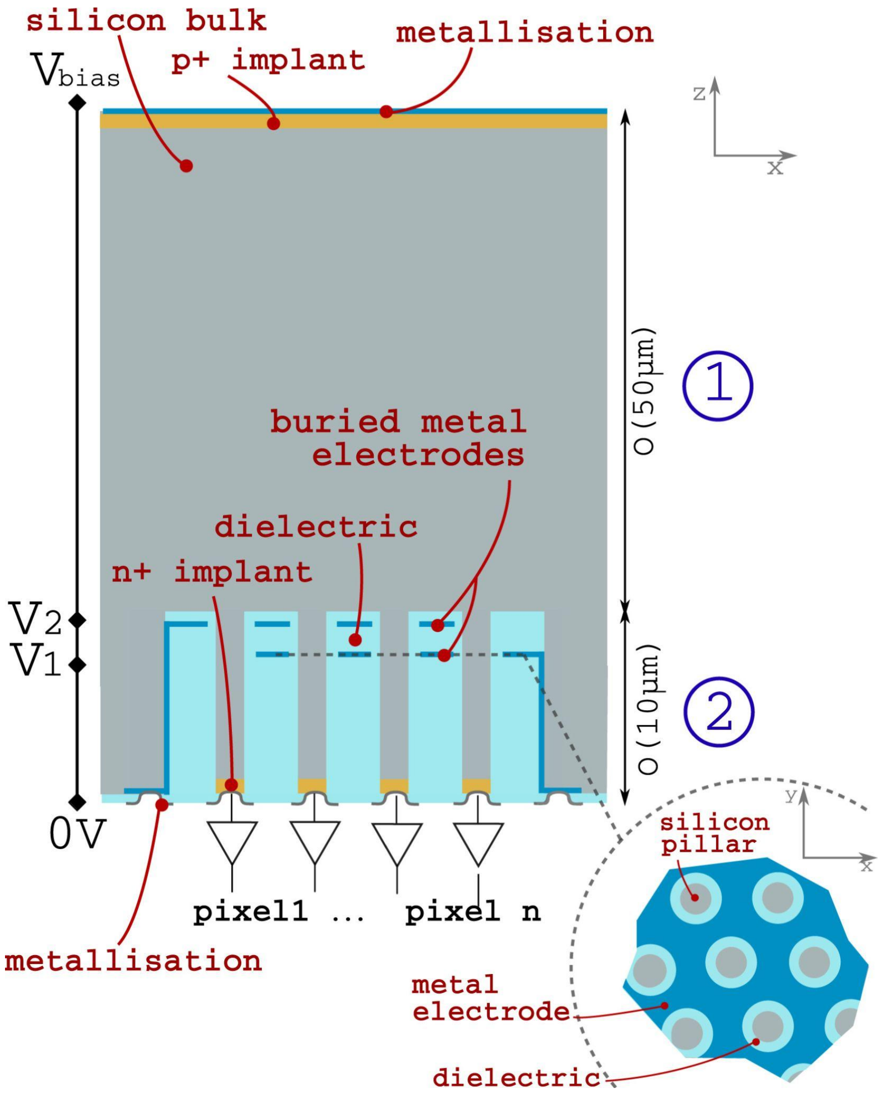
Average pulse shape from MIP of 100 µm sensor



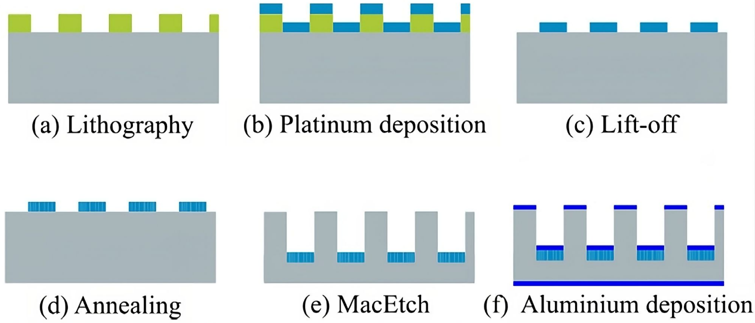
Silicon Electron Multiplier (SiEM)

- **Primary charges generated by ionisation in the conversion and drift region (1).**
- **High electric field region generated by applying a difference of potential to a set of metallic electrodes**
  - GEM-like structure (two grids separated by a dielectric)
  - Micromegas-like (single grid)
- **Electrons drifting in amplification and induction region (2) are multiplied and induced signal on the readout electrode**
  - Can be readout individually (small pitch ~5-10 µm)
  - Can be interconnected (large pitch ~50 µm)
- **Expect gain mechanism to be "radiation hard"**
  - Described NIMA 1041(2022)167325

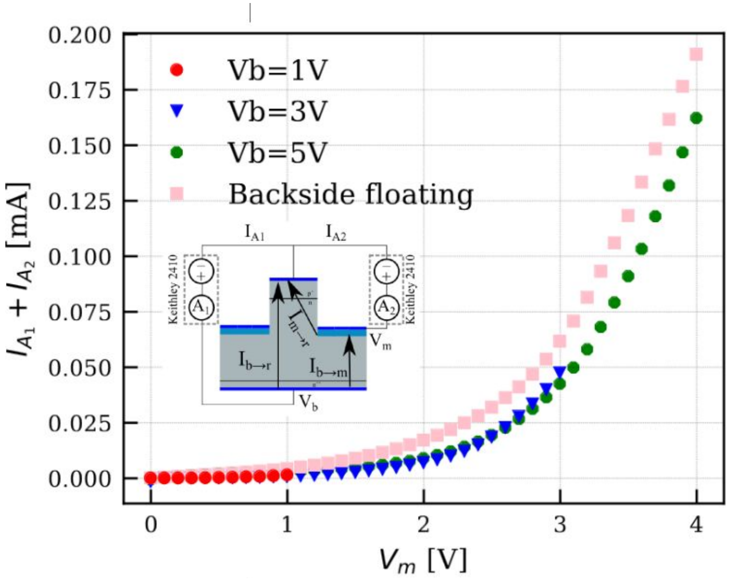
- **Two production processes under investigation:**
  - Metal assisted chemical etching (MacEtch): cheap but experimental ⇒ project with PSI
  - Deep reactive ion etching (DRIE): more complex but well mastered ⇒ project with CNM (AIDAinnova Blue sky R&D)

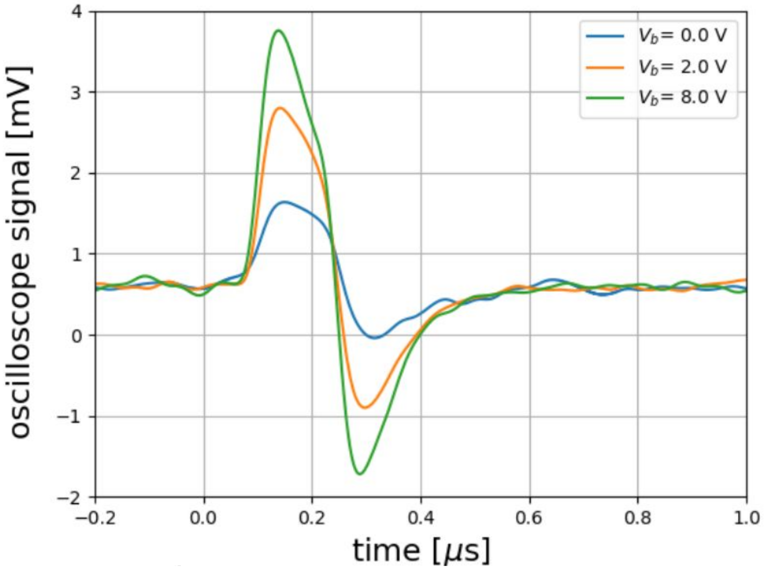


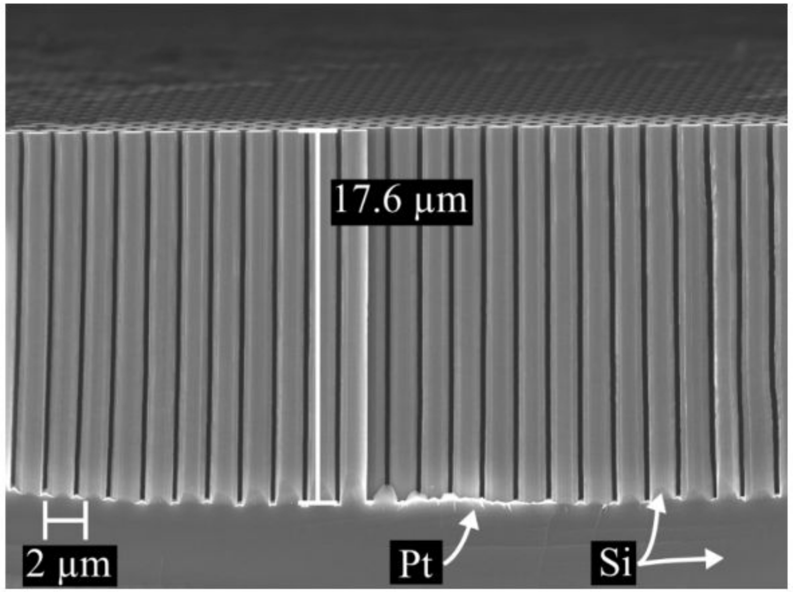
SiEM MacEtch Demonstrator



- **Metal assisted etching based process produced with PSI:**
  - I-V characteristics studied ⇒ pn-junction characteristics conserved
  - Showed the process can be used with active component
  - Limited to study amplification: collecting holes (p-in-n) and schottky diode between bulk and multiplication electrode leading to large current and limit usable HV
- **Studied transient charge response using infrared laser and 16 ch-board**
  - Signal from a SiEM strip increases with increasing bias voltage most likely due to increasing the size of the depletion volume
- **Production method and characterization documented in NIMA 1060(2024)169046**



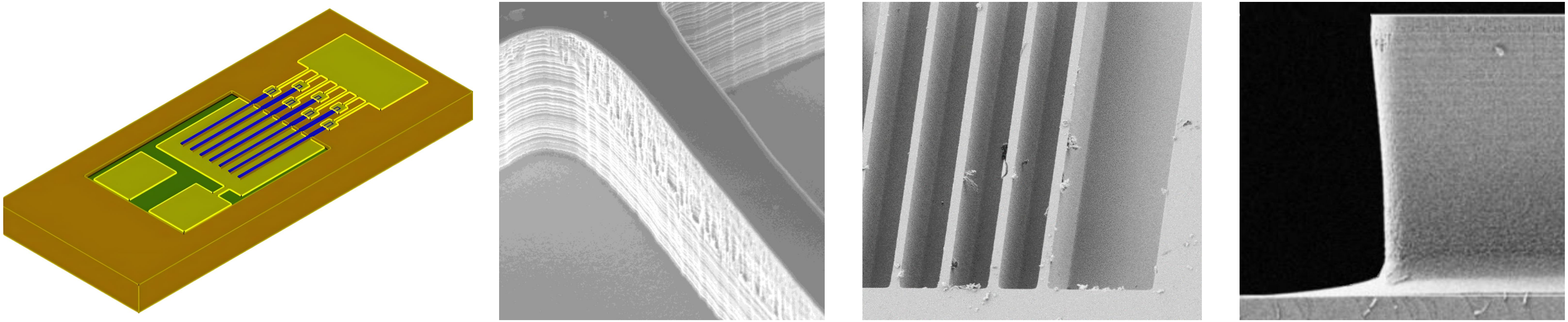




A slice of the MacEtch based demonstrator

SiEM DRIE Demonstrator

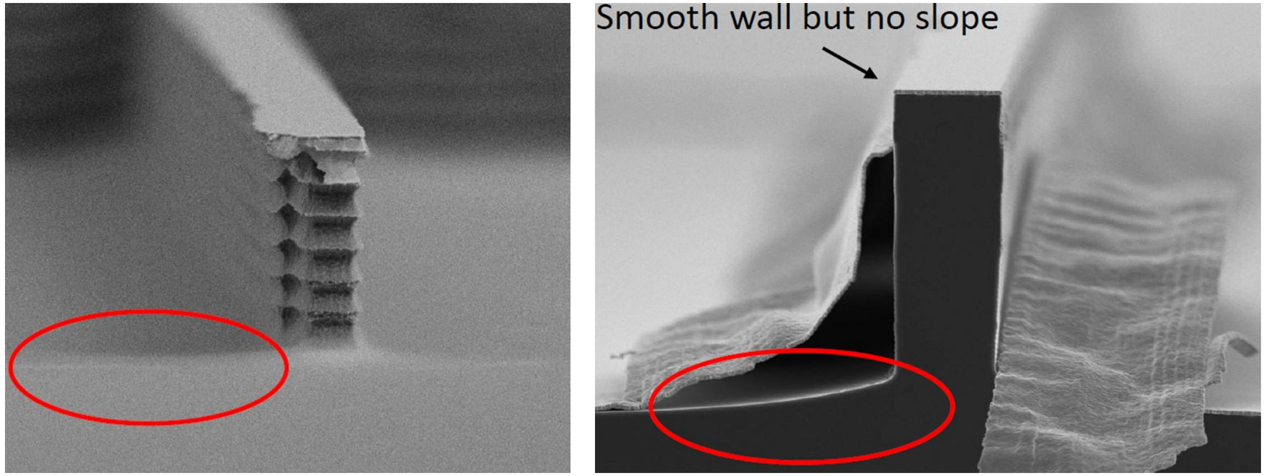
- **A silicon strip demonstrator is being manufactured in collaboration with CNM**
    - Two multiplication electrodes configuration
    - Aim at demonstrating the sensor concept
- **In order to have fast turn-around during R&D period decided to use laser photo-lithography**
    - Pillar base width need to be 1 or 2 um to maximize the electric field
    - Laser photolithography limited to 2-4um for top of pillar ⇒ proposed inverted pyramid pillar
- **Metal electrodes deposited using an evaporative Aluminum process.**
    - Electrode 1 deposited in the trench on top of an Atomic Layer Deposition (ALD) of HfO_2
    - Electrode 2 deposited on top of electrode 1 using SiO_2 as insulator

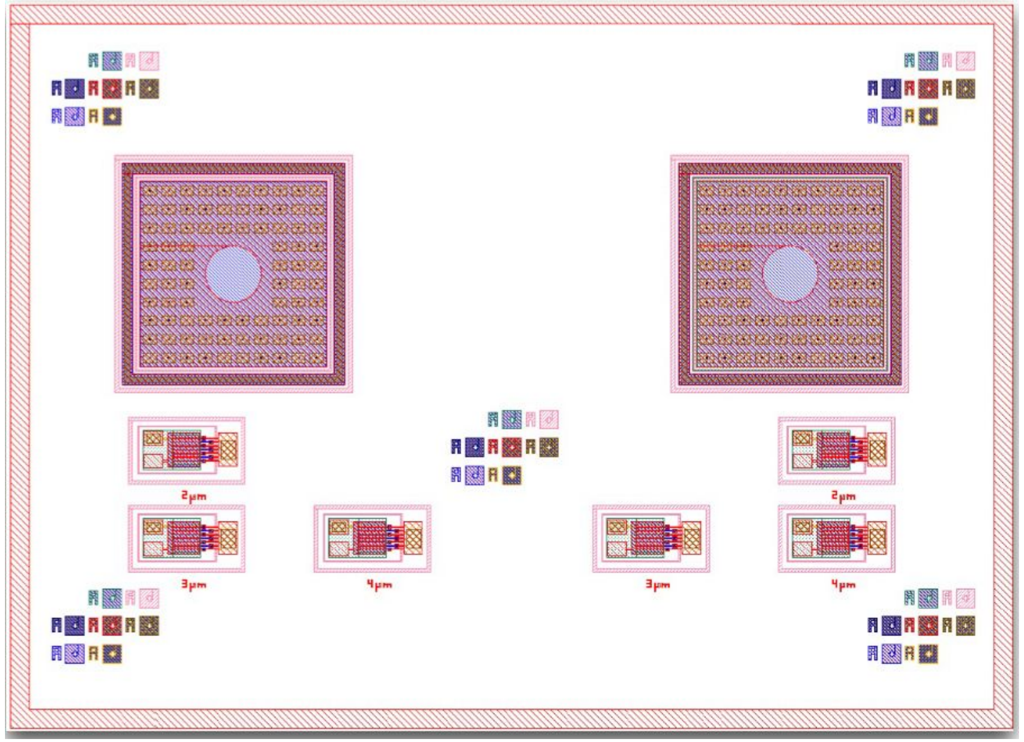


SiEM DRIE Demonstrator

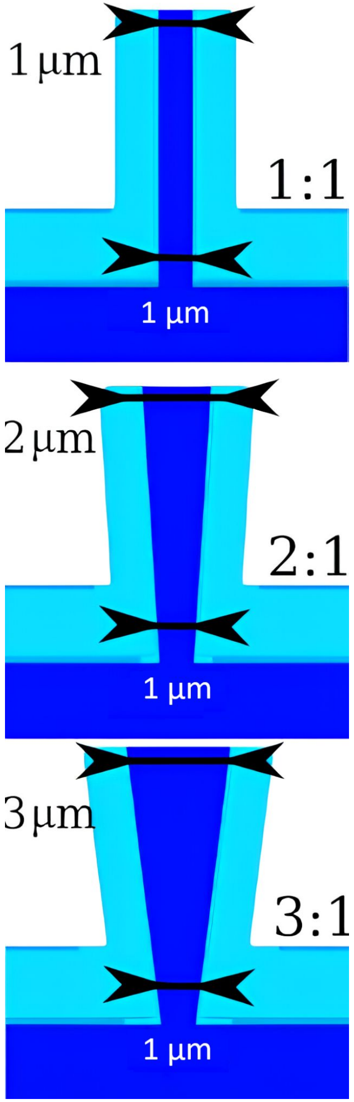
- **Several round of test to optimise the DRIE**
  - Balance between scalloping and speed + slanted wall more complicated to achieve than anticipated
- **Layout of the demonstrator finalised in Jan**
- **Implantation performed**
- **Non-planarity of the production wafer complicates the process (laser photolithography need to be re-focussed for each positions)**
  - Will produce mask, not ready before next month

See F.De Benedetti talk at AIDAInnova 3rd Annual Meeting

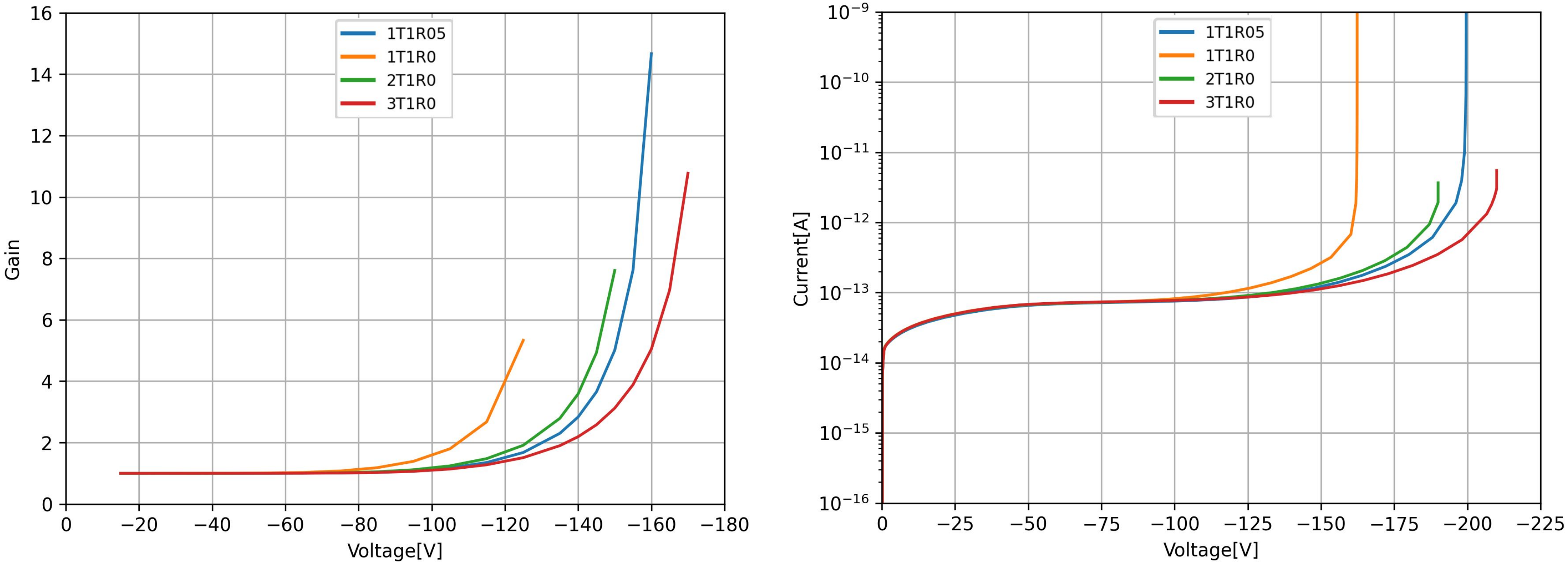




SiEM Simulations to validate CNM process

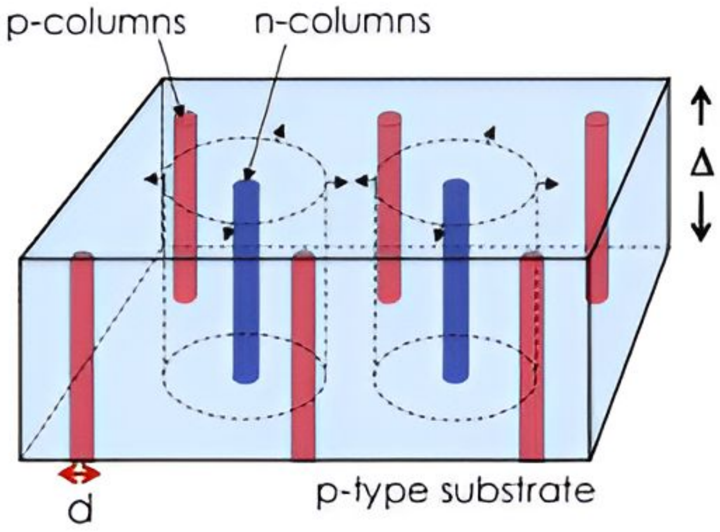


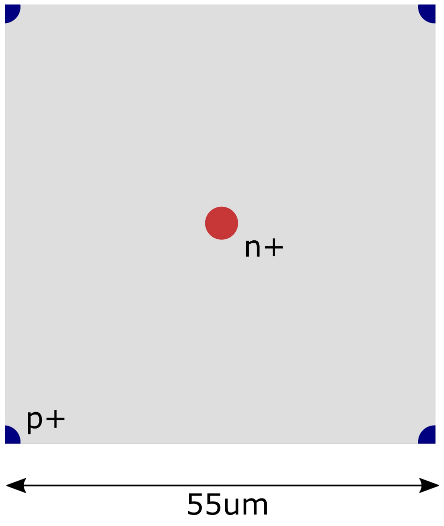
- **Updated TCAD model to the materials and geometry used at CNM**
  - Plus improvement in meshing and parametrability of the TCAD implementation
- **Investigated impact of the inverted pyramid geometry on the performances**
  - Quasistationary simulations are performed to study the electric field
  - Transient simulations are performed to study the MIP response
  - Gain > 10 can still be achieved
  - Difference dominated by the electrode retraction from the pillar ⇒ higher HV needed

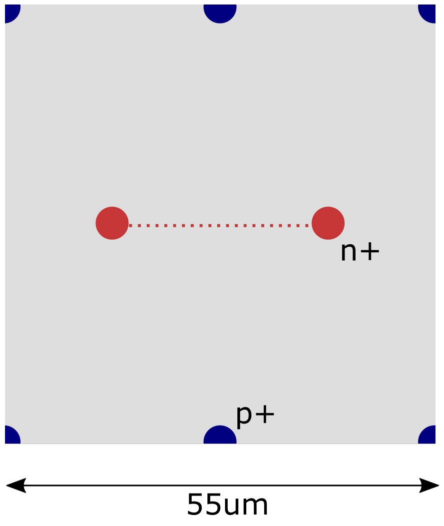


3D sensor production

- **Procurement of 3D column sensors within WP 1.1 ongoing**
- **Investigating 3D sensors with different column geometries and pitches (~48-55 µm), and from different vendors**
  - Sensor design takes into account the pitches that can be achieved in Picopix, the fast timing requirements (~50 ps), and target radiation hardness of $5\text{x}10^{16}$-10^{17}
  - Production includes large number of 4x4 test structures and larger pixel matrices of 64x64 and 256x256, latter compatible with Timepix3/4 ASICs
- **Some of the structure to also be included in AIDA innova production by CNM**







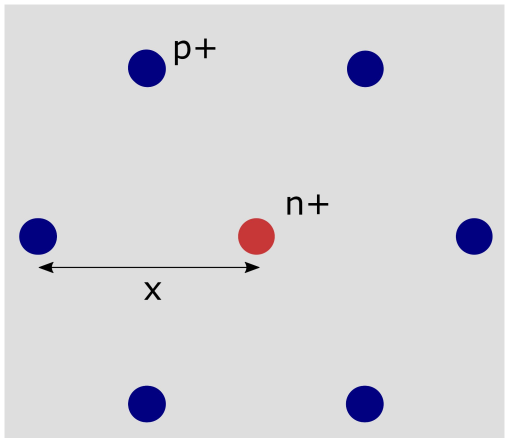


Image credit (left): 3D silicon pixel sensors, M. M. Obertino, TREDI 2014

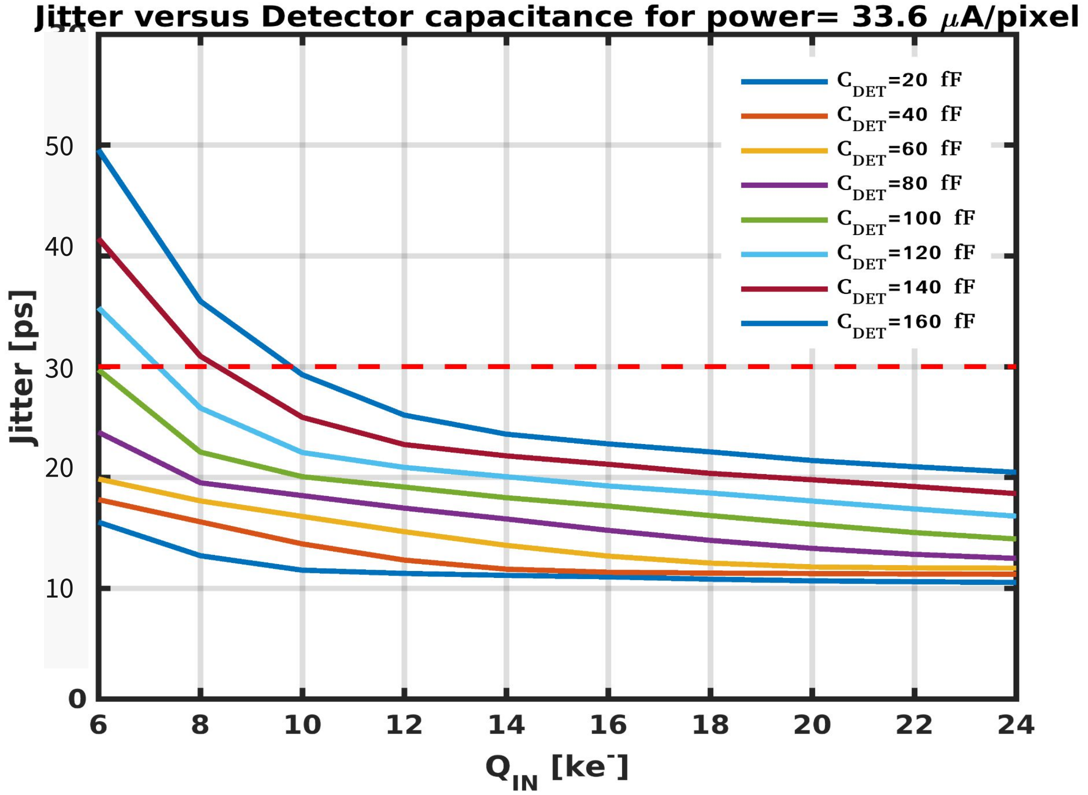
3D sensor toy simulation

- **In parallel, studying impact of 3D sensor design through a toy simulation:**
  - Aim: better understand how variables of 3D sensor design interact with each other vs impact angle and pixel pitch, with a fast and configurable software
  - Approximated 3D sensors with dead areas, different column geometries, reduced diffusion

- **Timing threshold also implemented:**
  - For timing jitter of <30 ps, need minimum amount of deposited charge

    → timing threshold to identify reliable timestamps
  - Timing threshold is function of input capacitance, therefore depends on sensor design

from V. Sriskaran picopix analog FE simulations

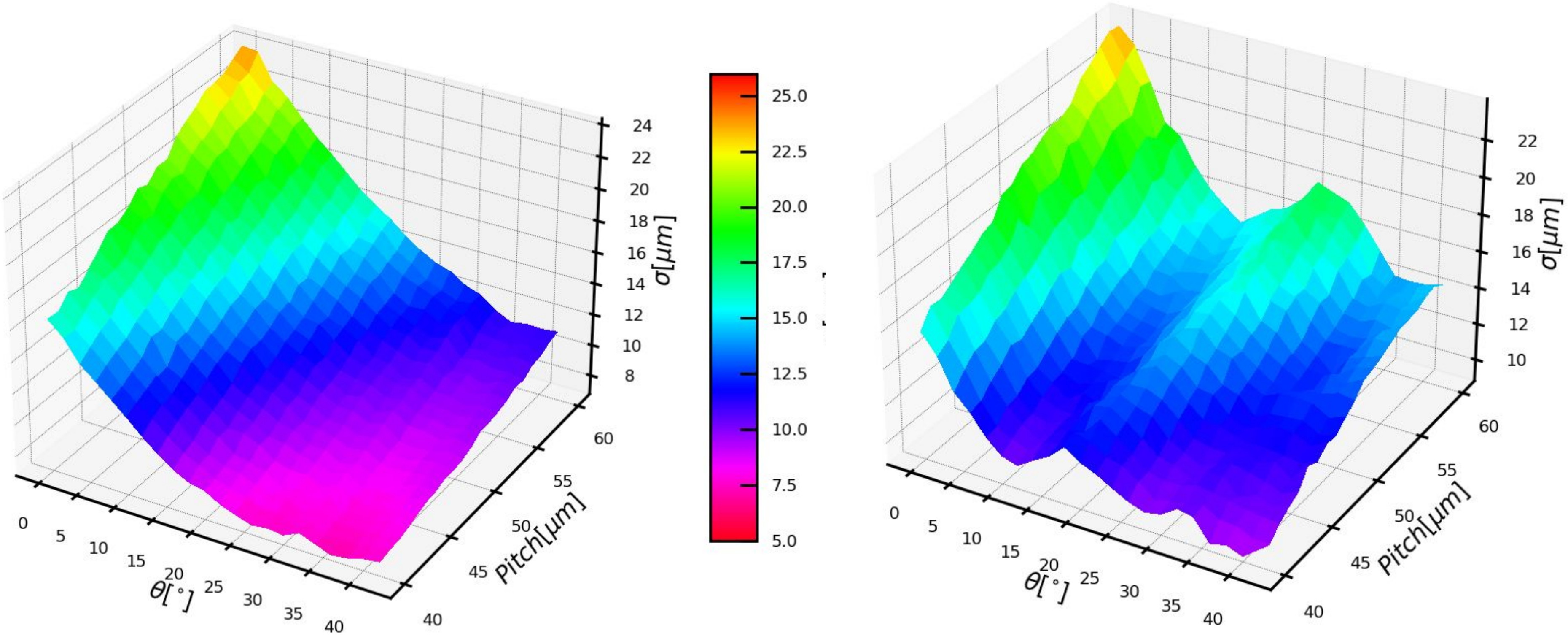


3D sensor resolution studies

Effect of different ASIC readout modes also investigated through a toy simulation:

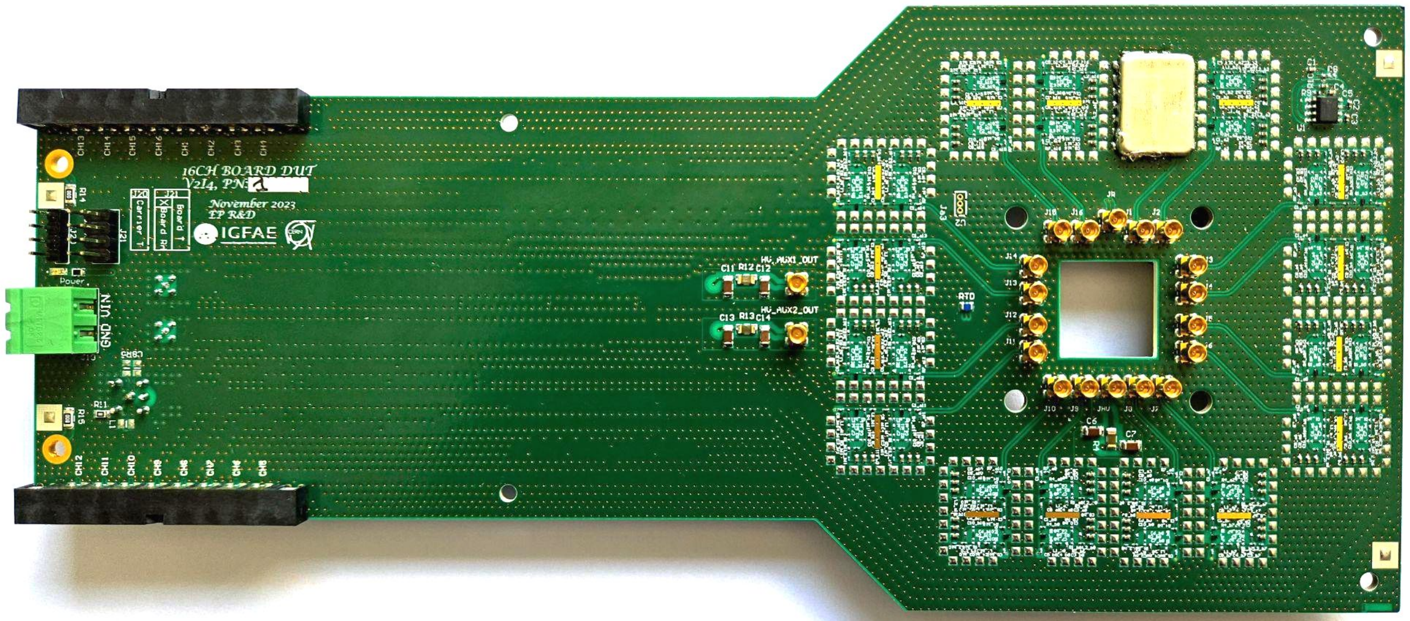
- Picopix outputs ToT of highest charge pixel in a cluster + 3x3 hitmap centred on this pixel → full charge information not available for cluster position calculation, configurable weights used
- In high data-rate environment, can reduce packet size by calculating cluster position on-chip
- How do these modes affect spatial resolution?

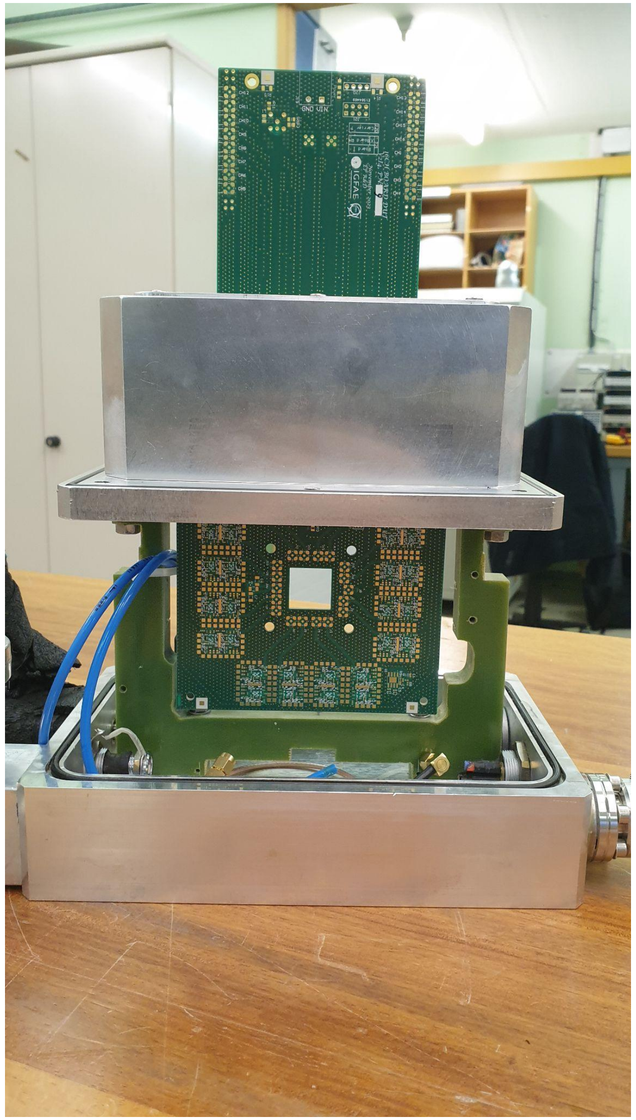
Effect on spatial resolution of calculating cluster position in 3D sensor using full charge information (left) or using configurable weighting (right).



16 ch board

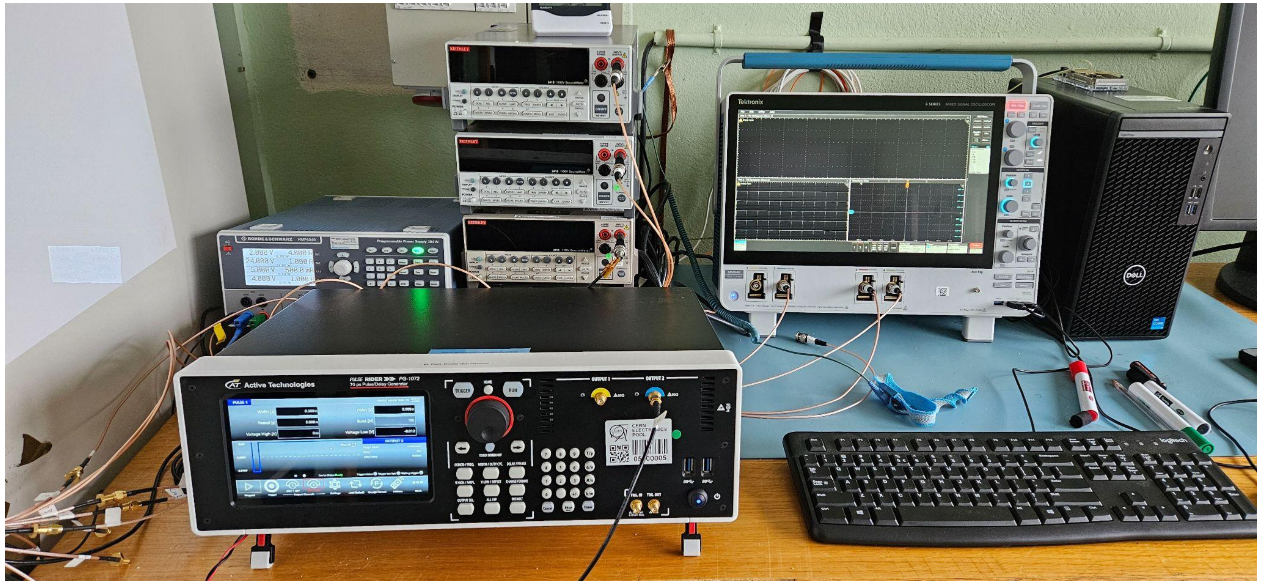
- **Improved 16 channel board design:**
  - Design based on Transimpedance Amplifier (TIA) with gain ~ 70
  - Improved signal insulation from the previous version
  - Added auxiliary high voltage lines for SiEM characterization
  - Compatibility with several carrier board designs
  - Compatibility with Timepix4 DUT mechanics for test beam characterization

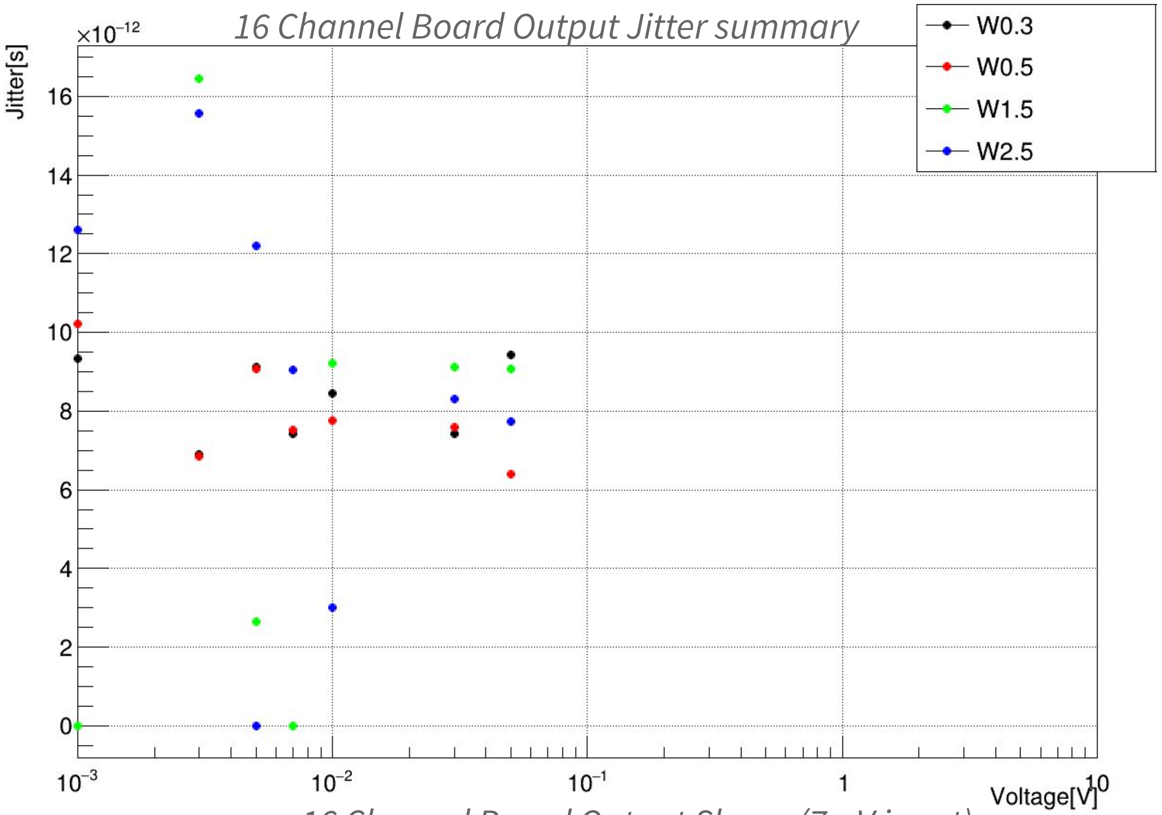


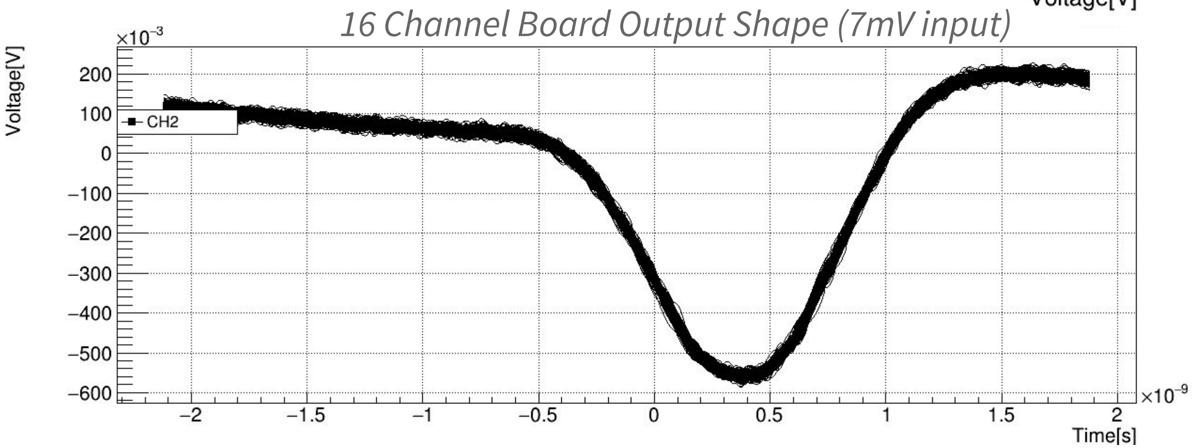


16ch board pulser tests

- **Preliminary tests with fast pulser:**
    - Investigated several input voltages and pulse shapes
    - Jitter ~ 10 ps for most of the cases
    - Gain ~ 70
    - T_{fall} & T_{rise} ~ 500 ps
    - Further test using laser/source

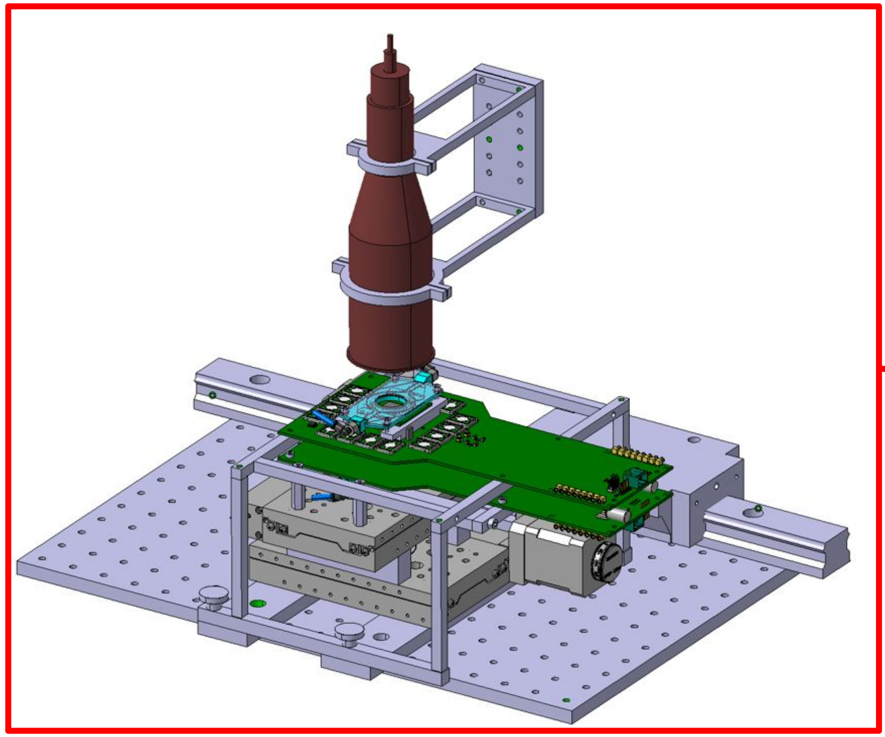


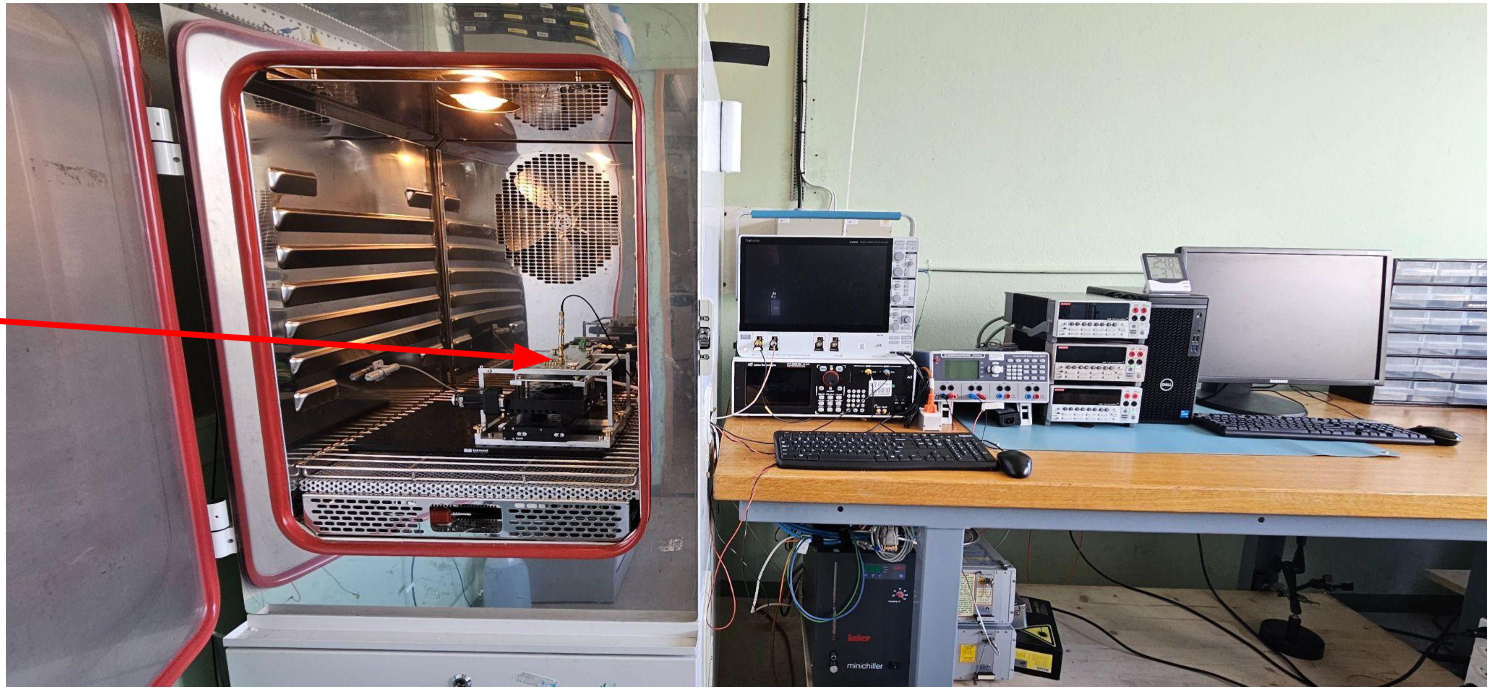




Laser setup commissioning

- Beta source set-up from 1st phase merged with a laser set-up + new mechanics + 16ch board integration + improved environmental controls
- Laser (660 nm & 1064 nm) system procured from Particulars (Slovenia) with modifications to be made for timing measurements, to be integrated once received
- Lab reorganisation (20/R-006, 014, & 016) performed: dedicated sensor testing area, area with dedicated individual stations (microscope, soldering, etc.), and large open lab workspaces





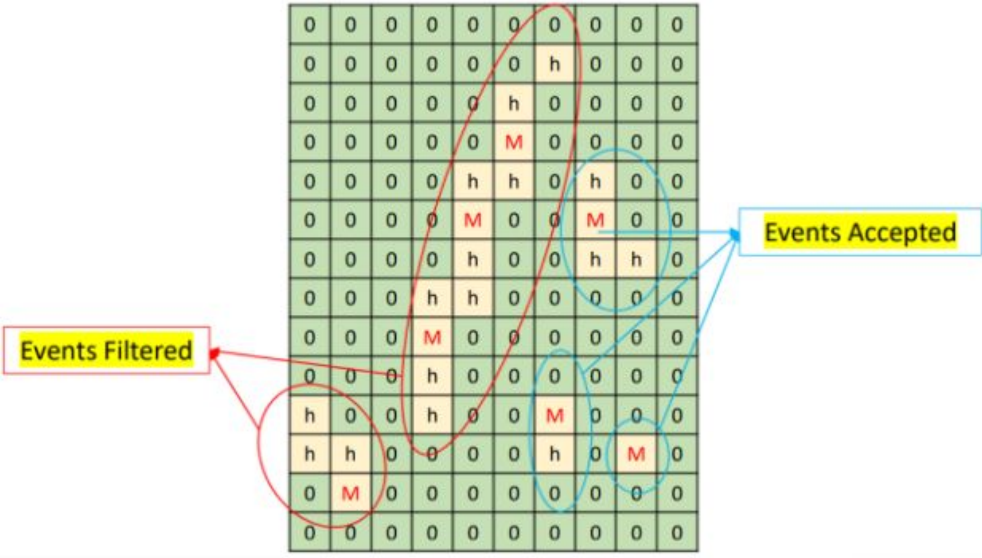
Picopix project

Project driven by EP-ESE with contributions from EP R&D WP1.1, WP5, WP6, Nikhef, Santiago

- **LHCb 4D-tracking for VELO U2 used as a specifications**
- 28 nm CMOS technology → first from EP-ESE at this node
- **Target resolution of < 20 ps rms track time**
  ⇒ Single plane resolution of < 50 ps rms

- **Target $\sigma^2_{\text{analogFE}}$ < 25 ps rms**

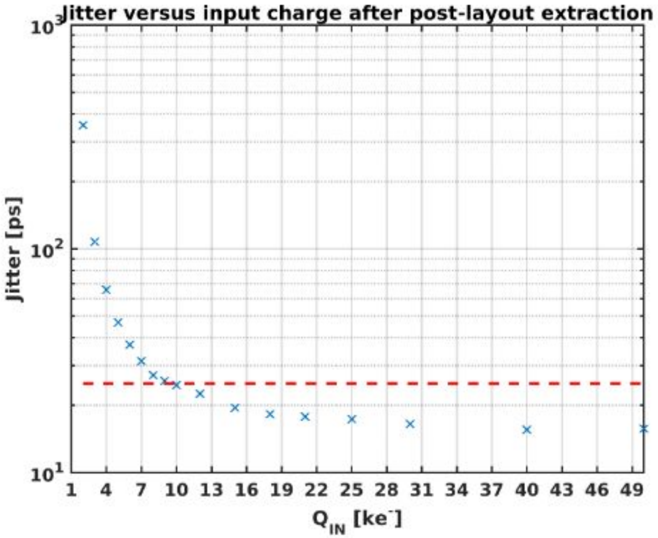
- **Pixel size < 55 µm:**
  - Challenging power budget and data rate
  - In-matrix clusterization ⇒ reduces in matrix trafic by vetoing cluster not compatible with tracks in acceptance (3x3)
  - ToT output for only highest ToT pixel in the cluster
  - Different readout modes being investigated for high data rate regions
  - Expected to achieve 2.6 -3.8 G events/s/chip



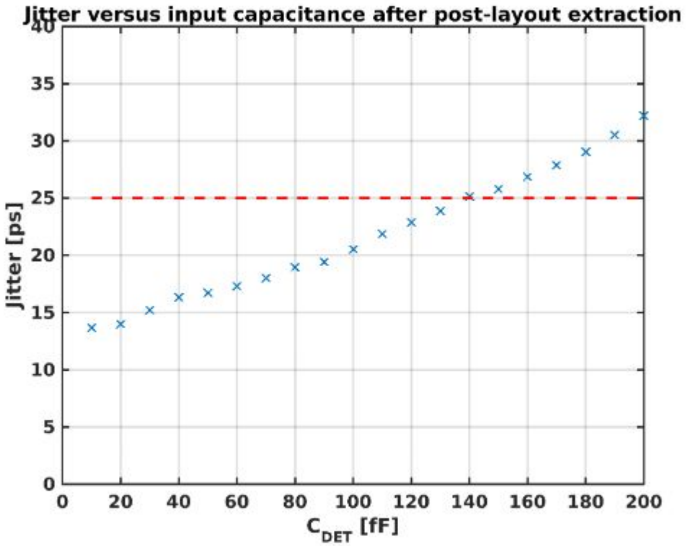
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	h	0	0	0
0	0	0	0	0	h	0	0	0	0
0	0	0	0	0	M	0	0	0	0
0	0	0	0	h	h	0	h	0	0
0	0	0	0	M	0	0	M	0	0
0	0	0	0	h	0	0	h	h	0
0	0	0	h	h	0	0	0	0	0
0	0	0	M	0	0	0	0	0	0
0	0	0	h	0	0	0	0	0	0
h	0	0	h	0	0	M	0	0	0
h	h	0	0	0	0	h	0	M	0
0	M	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Analog island design

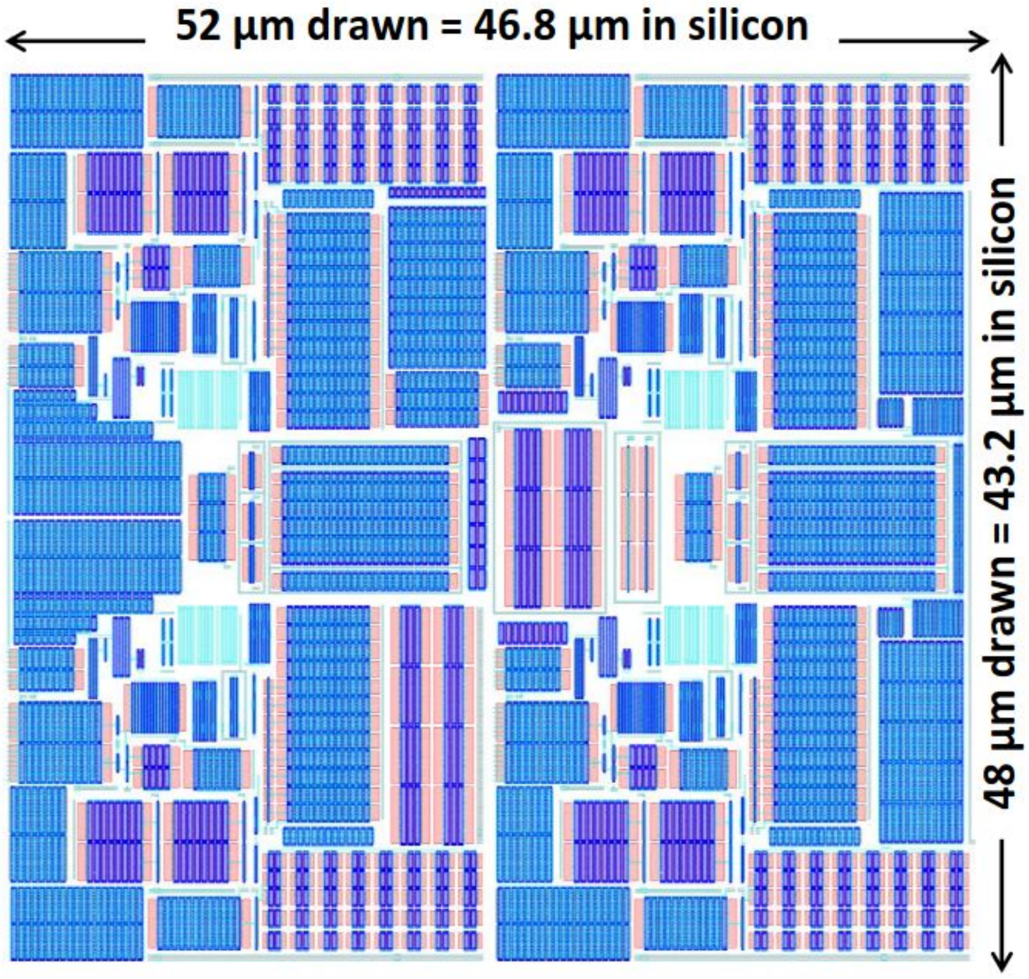
- **Analog FE designed done by V. Sriskaran (FELL EP R&D WP1.1) with EP-ESE**
  - 2x2 pixels analog island
  - 52 x 48 µm² area drawn: equivalent to 25% area in a 45 µm pitch or 17 % area in a 55 µm pitch.
  - Layout following the radiation recommendation rules.
- **Design reviewed in February; EP R&D seminar April**



Parameters= {C_{DET}= 110 fF, I_{KRUM}=100ns}



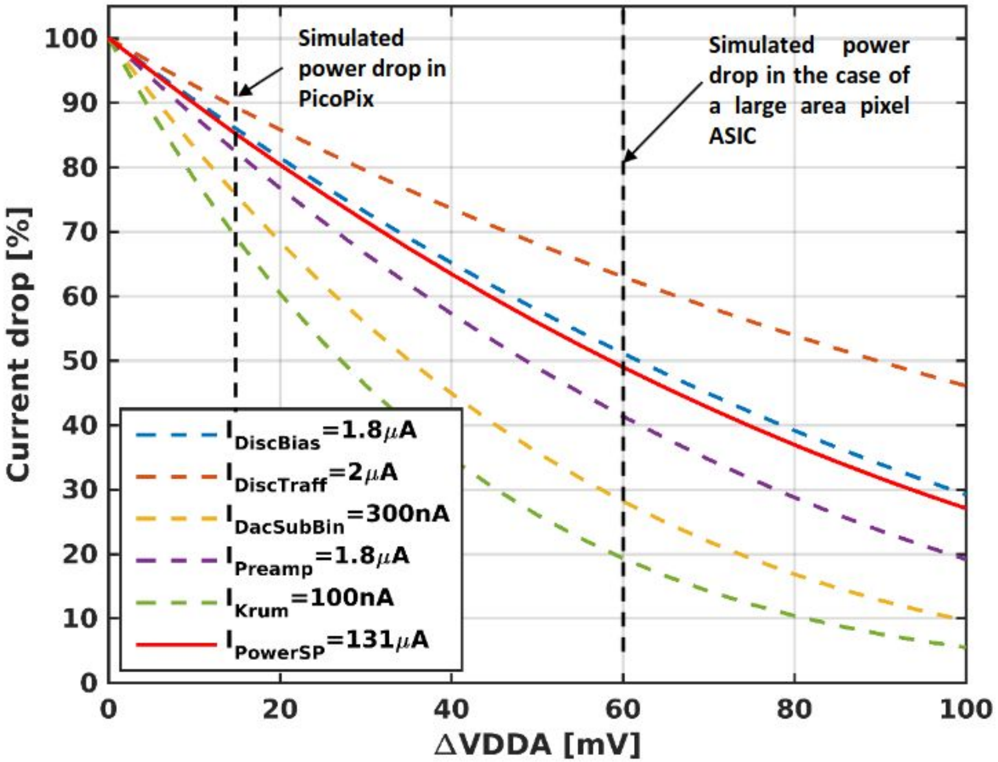
Parameters= {Q_{IN}= 2fC, I_{KRUM}=100ns}



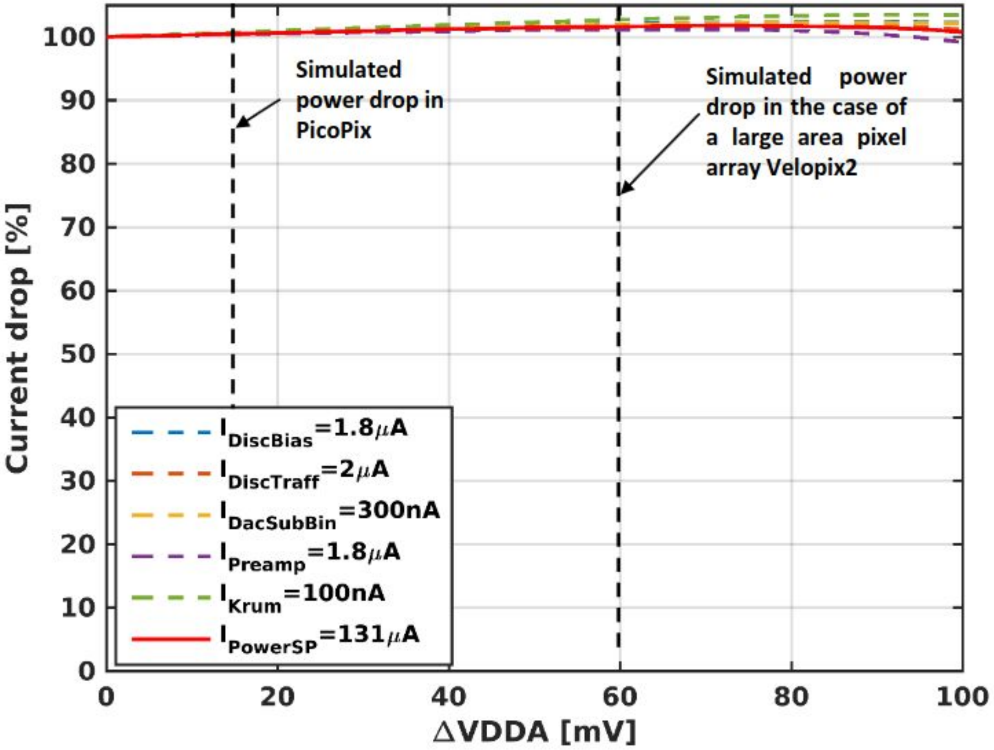
Layout Superpixel SP0

On-pixel power drop compensation

- Original design showed power distribution is key to keep the timing performance along the matrix
- Possible alternative is use of TSV ⇒ depending on project can be expensive and challenging
- Implemented a on-pixel power drop compensation mechanism with success in simulations



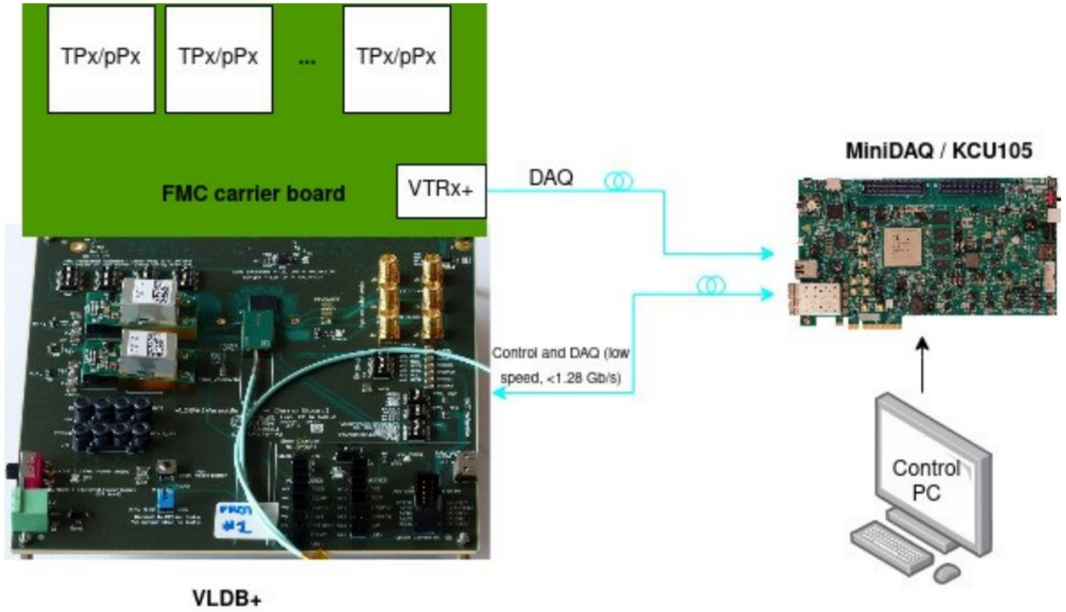
Pixel biasing without on-pixel power-drop compensation



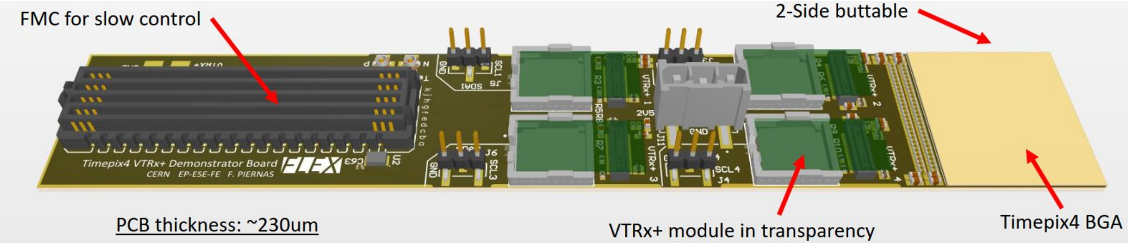
Pixel biasing with on-pixel power-drop compensation

Picopix readout

- **System integration for Picopix based on VTRx+ and lpGBT**
    - lpGBT: main control ASIC option for upcoming detector upgrades
    - Timepix4 has similar ECS protocol as being designed for Picopix → integration of Timepix4 with VLDB+ board allows the clock distribution and control through lpGBT be tested
    - Carrier board design for Timepix4 ongoing
    - 12.5 GBps output line will be investigated using VTRx+. Design of DAQ is on going in the EP-ESE department → both will be merged together in the future



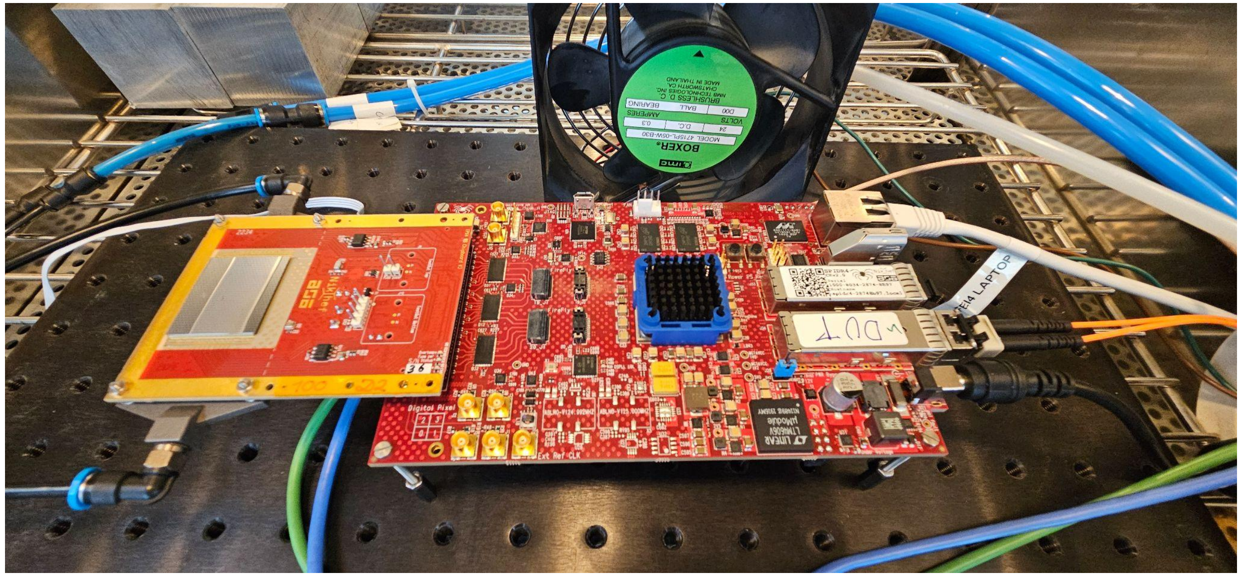
Carrier board, EP-ESE project by F. Piernas

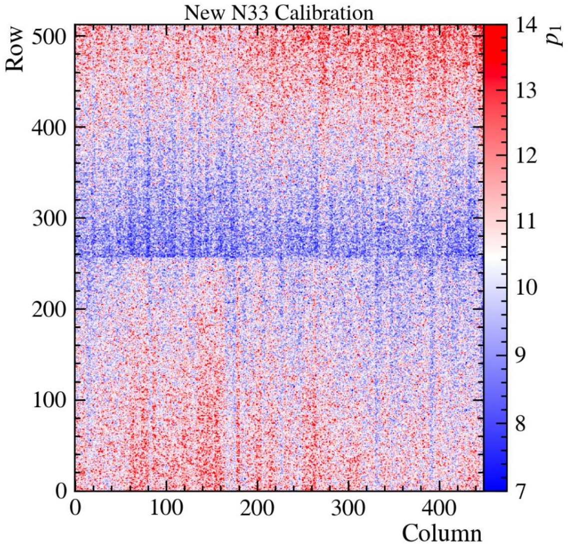


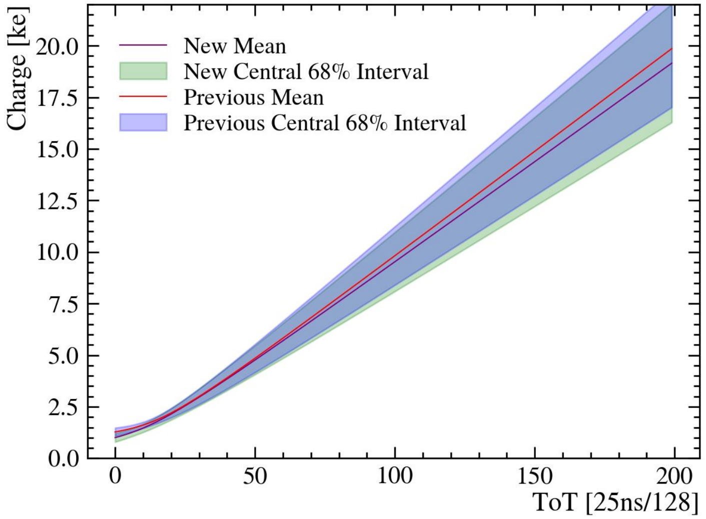
Timepix4 set-up

Improved Timepix4 setup in the lab for charge calibration:

- New run control machine installed
- Better temperature and humidity control
- Timepix4 cooled down with a chiller to replicate test beam temperature conditions
- Improved charge calibration routine from previous 14 hours → 2 hours
- Verified new calibration routine comparing with previous one

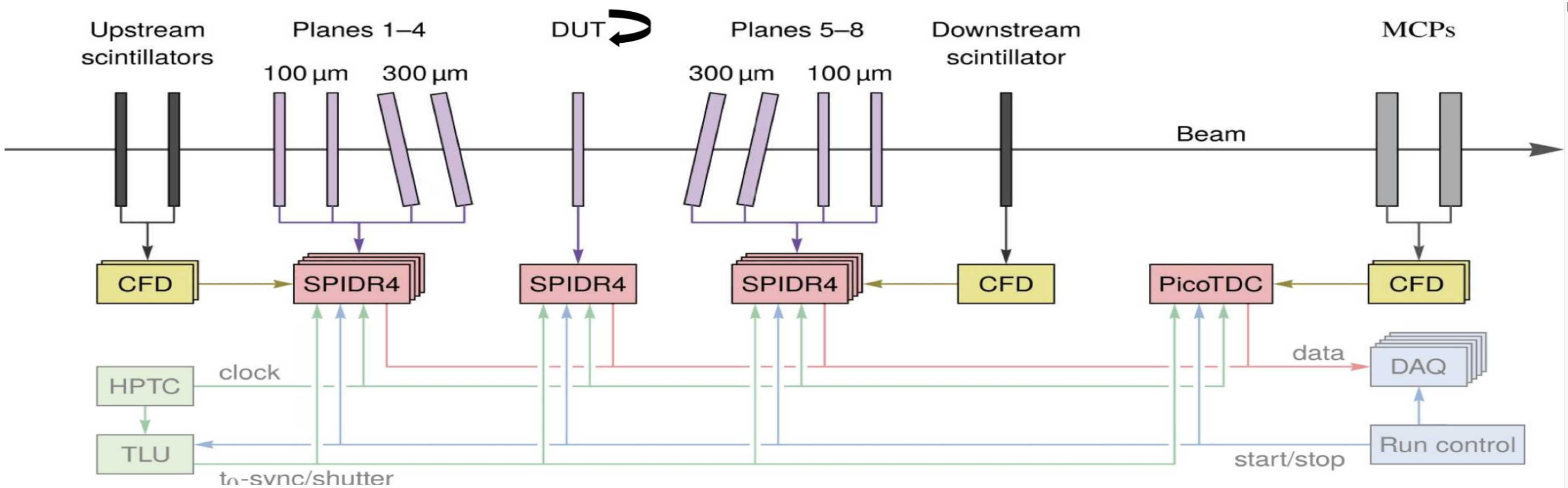


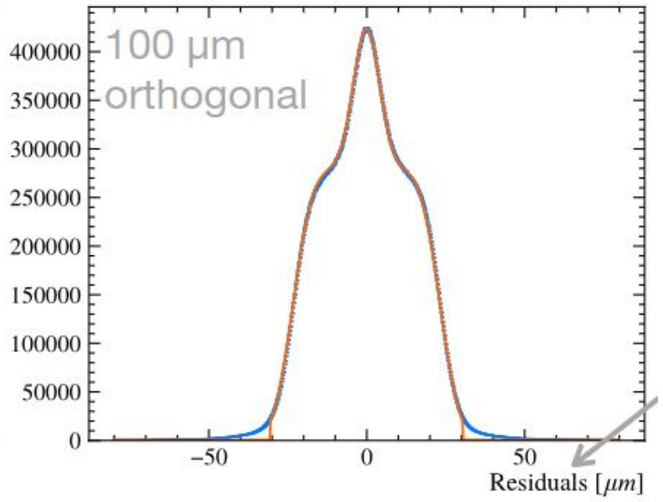


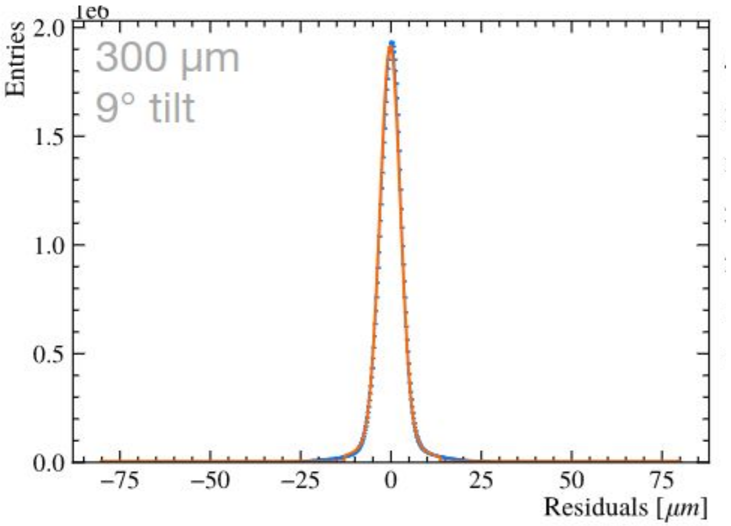


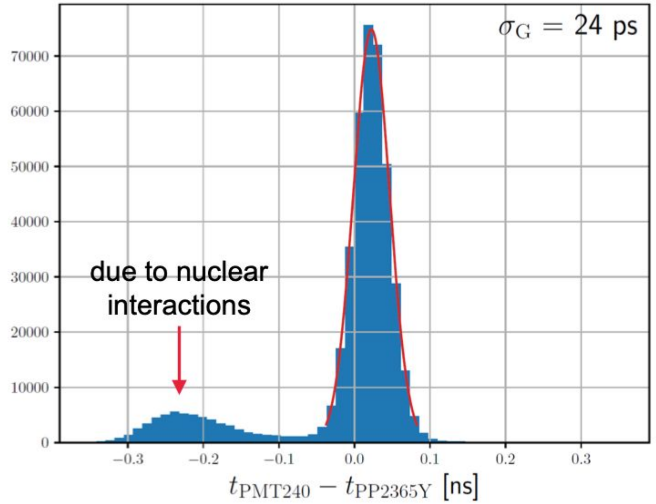
Timepix4 telescope

Collaboration including:
CERN, Nikhef, IGFAE, TU Dortmund, University of Manchester, University of Oxford, University of Birmingham,University of Glasgow









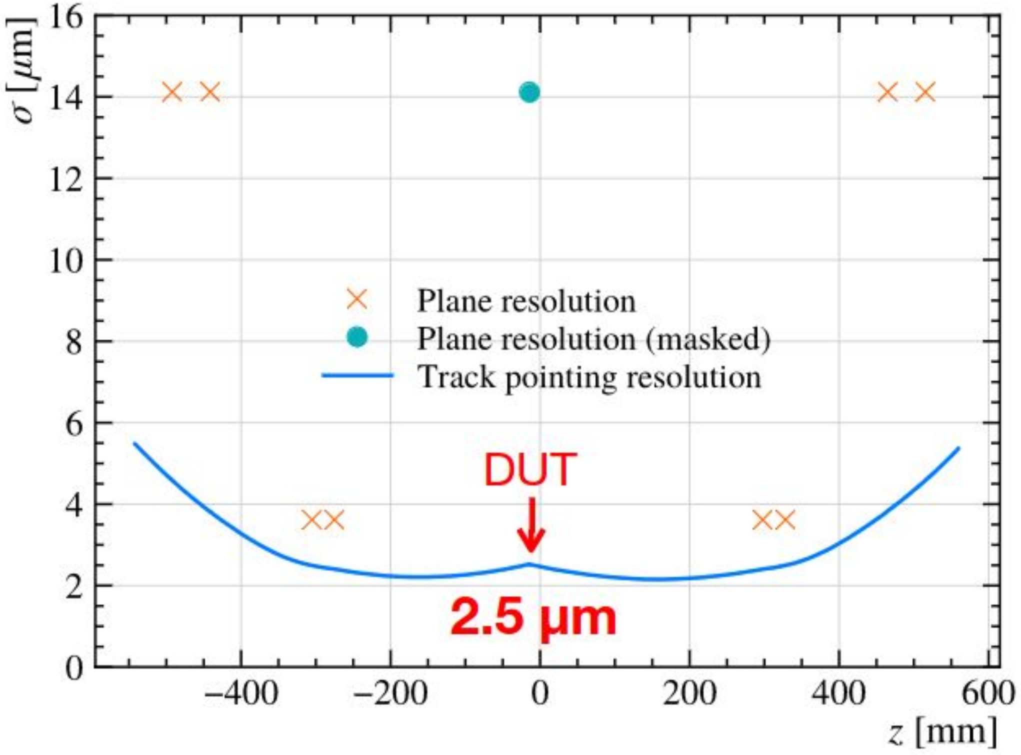
Outermost planes are vertical and have poorer spatial resolution but better timing resolution

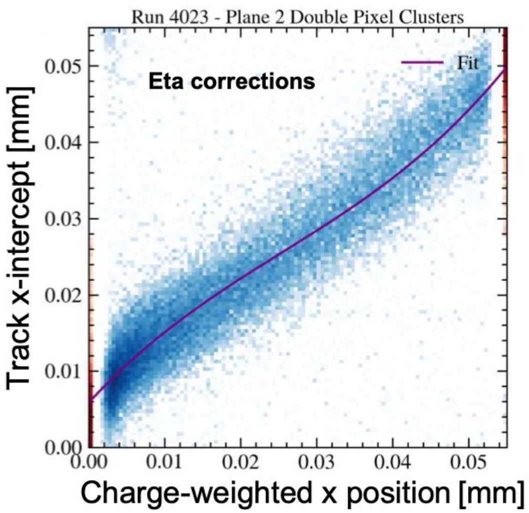
Innermost tilted planes provide best spatial resolution

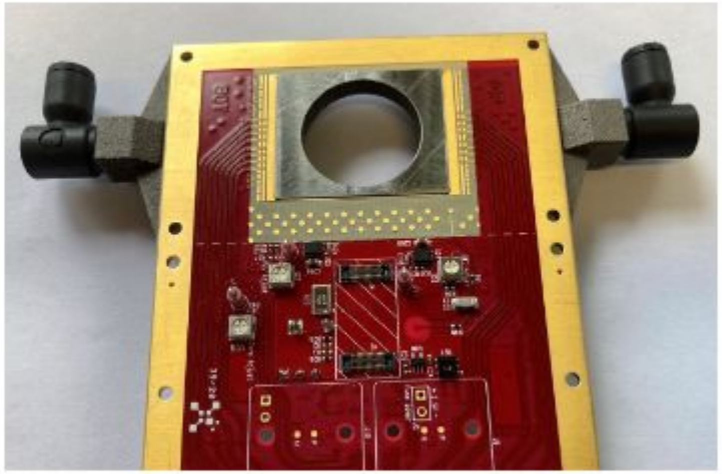
Timing provided by MCP reference planes with combined resolution of 12 ps, or by Timepix4 planes for high rate time stamping

Timepix4 telescope

- **Four innermost planes rotated 9 degrees around x and y to enhance charge sharing between pixels**
- Per pixel calibration applied from test pulses
- **Single plane resolution: 3.7 µm**
  - Achieved **2.5 µm** pointing resolution at the DUT
  - PCB adds 1.8% X0; milling out PCB will improve resolution to **2.0 µm**
  - Investigating eta corrections for non linear charge sharing

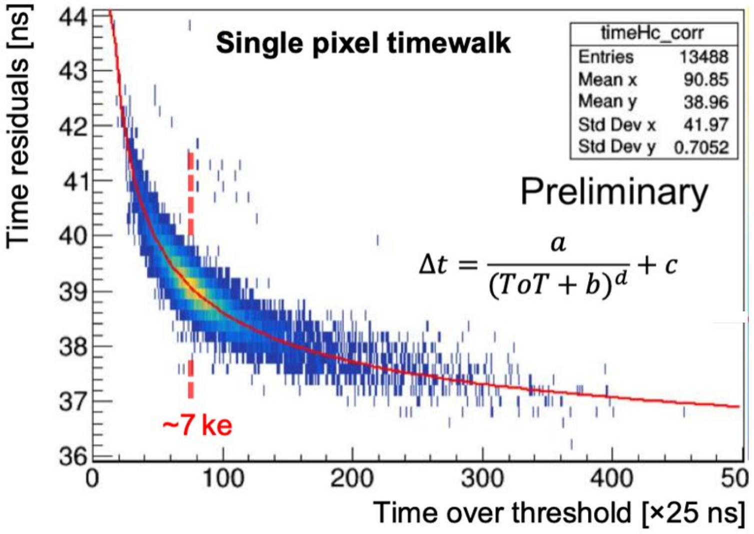


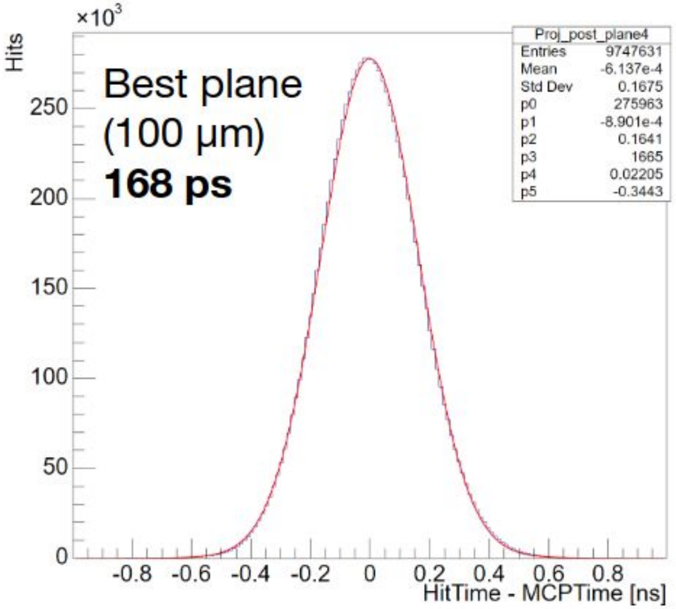


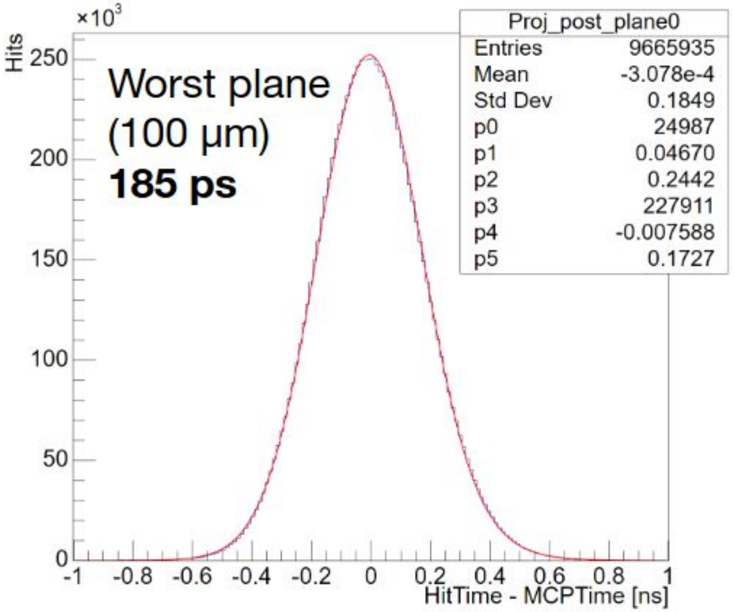


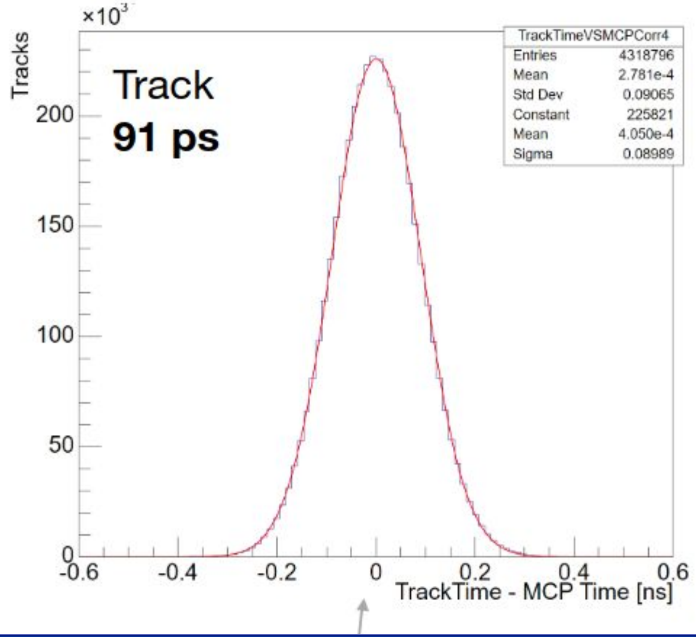
TPX4 telescope timing capabilities

- **Timing reference provided by MCPs (combined σ_t = 12 ps)**
- **ToA measurement from timepix planes**
    - Corrected for per superpixel VCO
    - Corrected for timewalk
- **Aim is to investigate performance for 4D tracking applications**
    - 100 µm planar sensor have limited HV reach ⇒ best σ_t = 168 ps
    - Global track time resolution based on 4x100 µm sensor σ_t = 91 ps
    - Shows the scaling of time resolution from individual planes to 4D tracks do scale as $\sigma_+/\sqrt{N}$



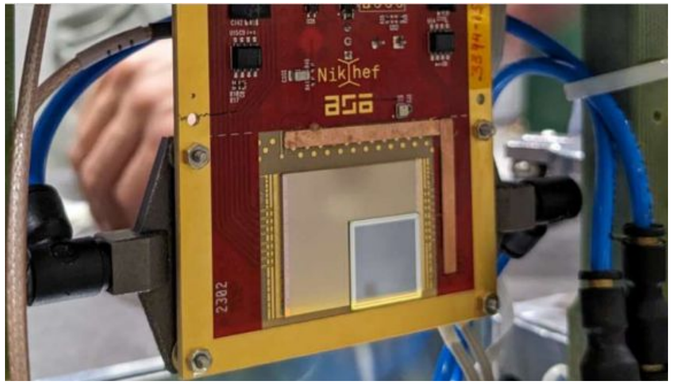




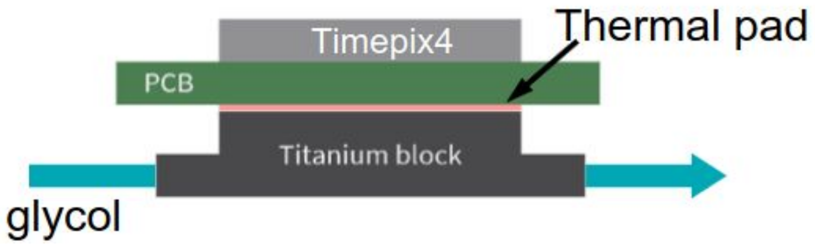


Timepix4 telescope

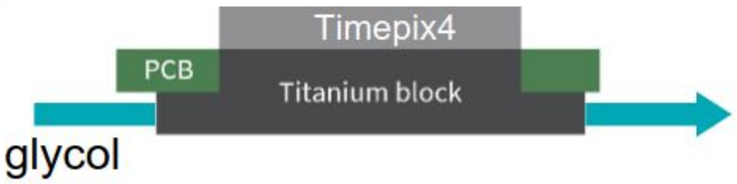
- **May and June 2023 testbeam campaigns:**
  - Targeting TPX4 telescope commissioning (bias, threshold, I_{preamp})
  - since June also study DUTs (planar 50, 100 and 200 µm)
- **August 2023 testbeam campaign:**
  - Inverted LGADs as DUT (bias, threshold, angle scan)
- **May 2024 testbeam campaign:**
  - Trench Insulated LGADs, ILGADs and 3D as DUT (bias, threshold, angle scan, I_{preamp})
- **Improvements:**
  - Fast sensors to bring the 4D tracking capabilities to the target performance
  - Material budget reduction to improve track resolution on DUT by milling the PCBs
  - This will also allow direct thermal contact with Timepix4
  - Ability to readout non-TPX4 based DUT, starting with 16ch board readout by oscilloscope or PicoTDC



Current thermal interface



Future thermal interface



Conclusion

Many aspects of WP1.1 have progressed and evolved over the last year:

- Ongoing investigations into SiEM and 3D sensor technologies for radiation hard fast timing detectors, both with simulations and production
- Improvements of 16 channel board and laboratory set-ups for sensor characterisation
- Evolution of Picopix project, with the analog front-end design and readout development being performed within WP1.1
- Current status of Timepix4 telescope has been presented, with outlook on improvements to be performed in the near future

CERN