EP R&D WP1.2

Monolithic CMOS Sensors

EP R&D Day

22 May 2024

Francois Vasey, on behalf of WP1.2 team

Acknowledgement: the results presented here were achieved thanks to a massive contribution from Colleagues outside EP R&D, in particular from the ALICE Collaboration.

WP1.2 Overview

Monolithic CMOS sensors for future tracking applications

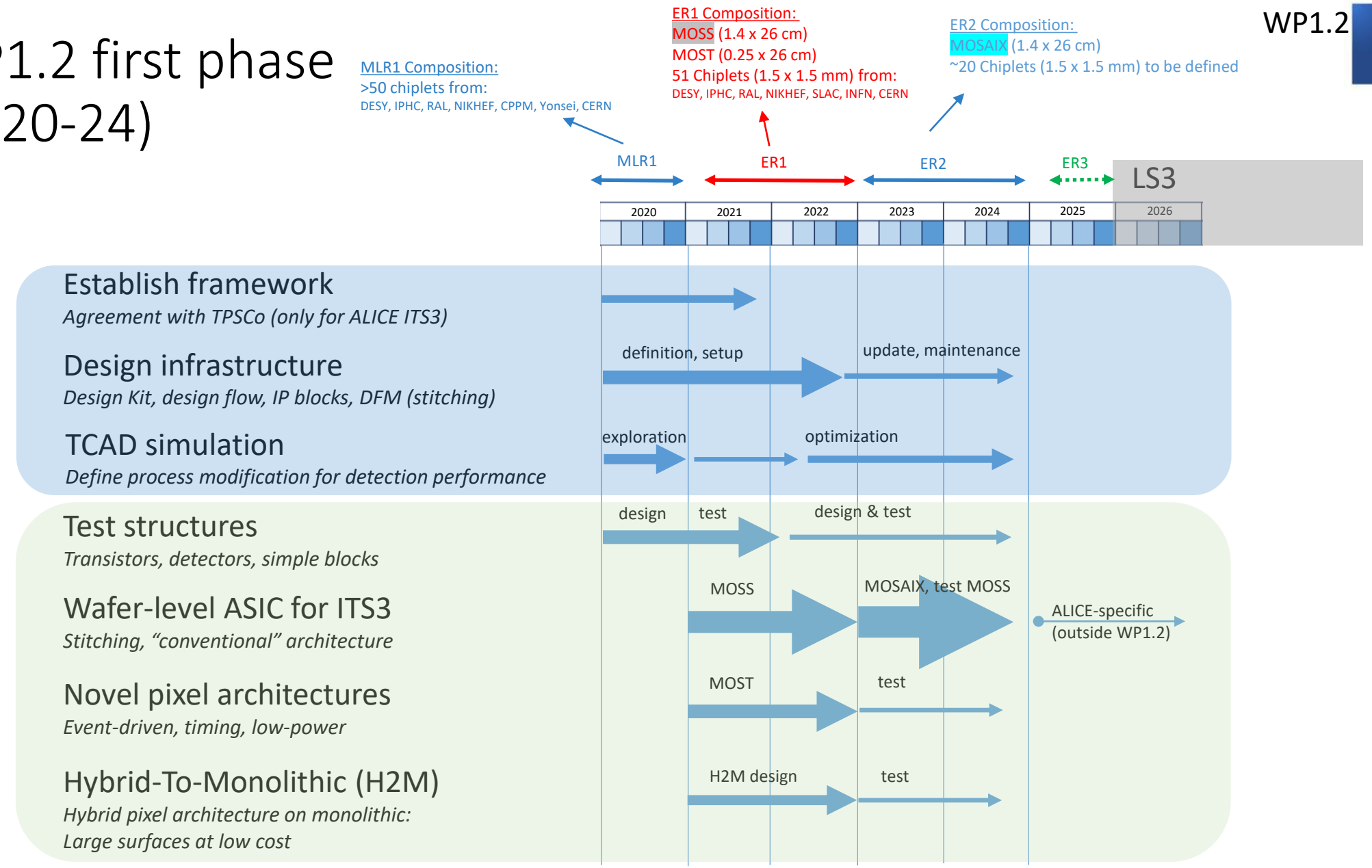
Wafer-scale stitched sensor (ALICE ITS3)

TPSCo 65nm Design framework (contribution to DRD7)

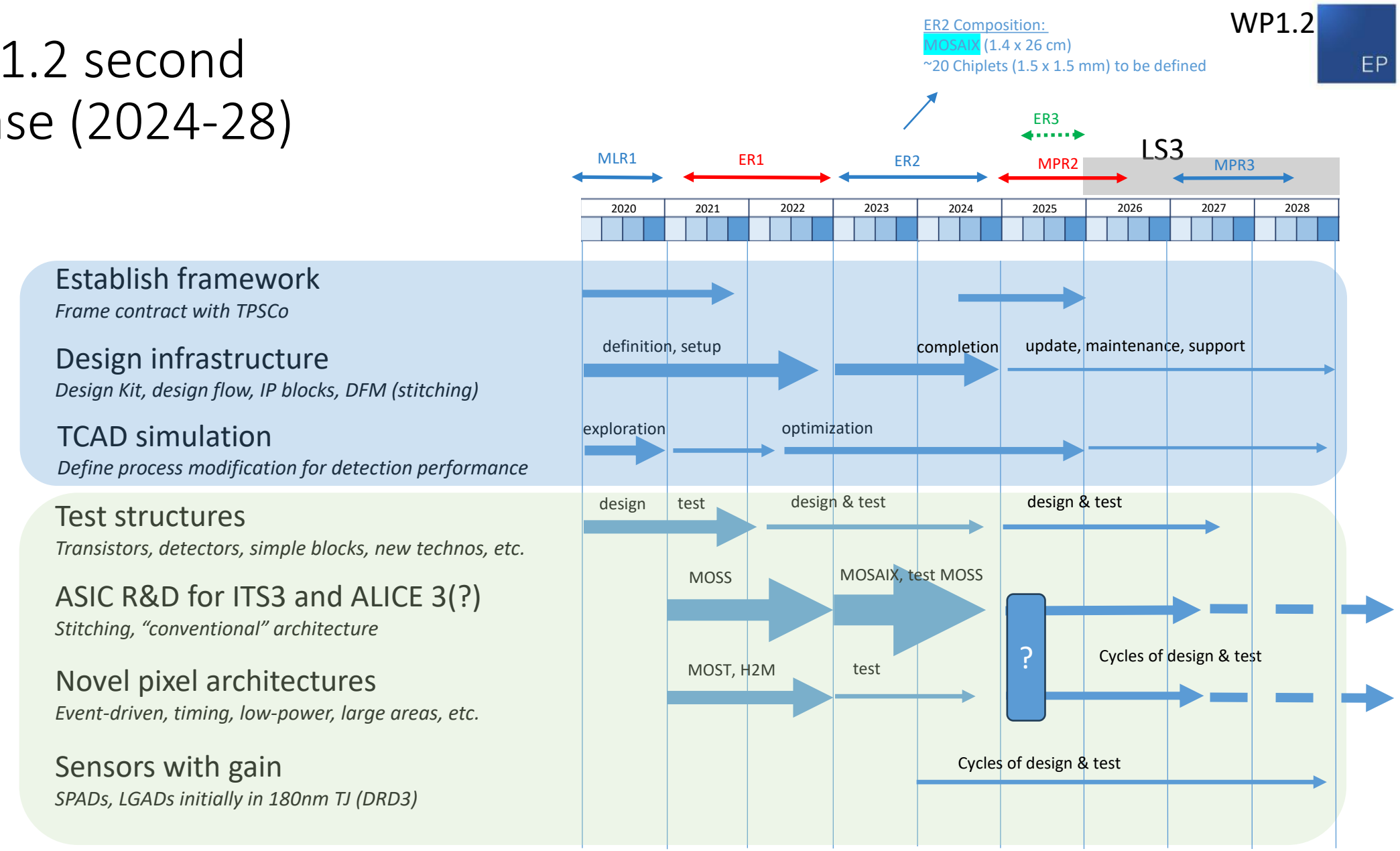
Novel concepts CMOS sensors

- *Radiation tolerance*
- *Large area*
- *Fast timing*
- *Low power*

WP1.2 first phase (2020-24)

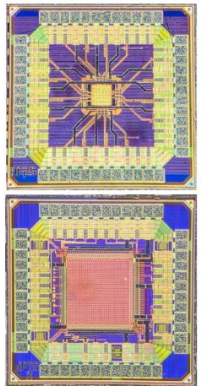


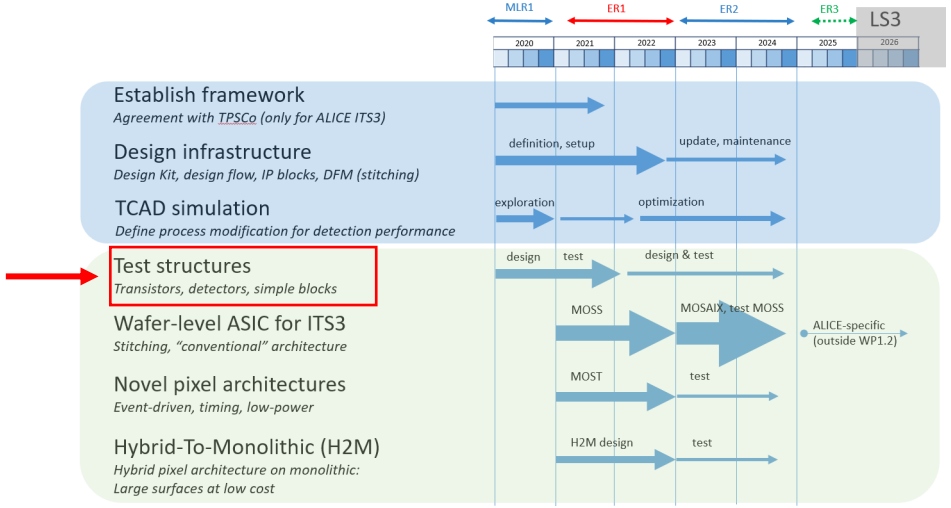
WP1.2 second phase (2024-28)



Recap: MLR1 and ER1 test results

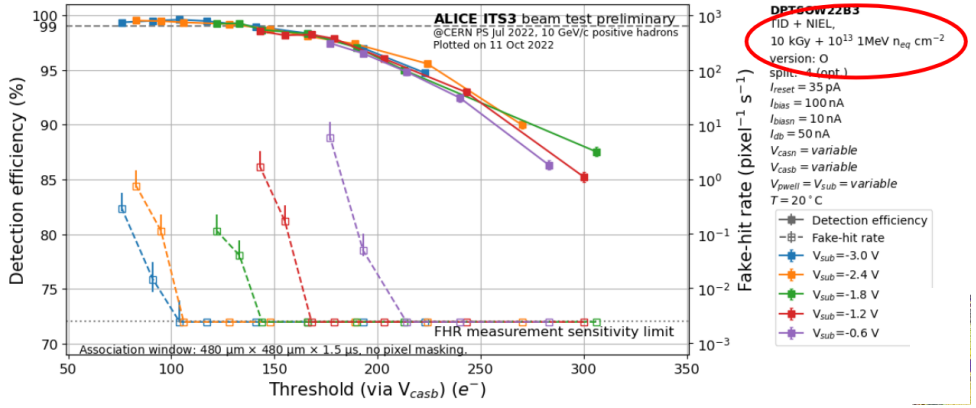
a) CHIPLETS

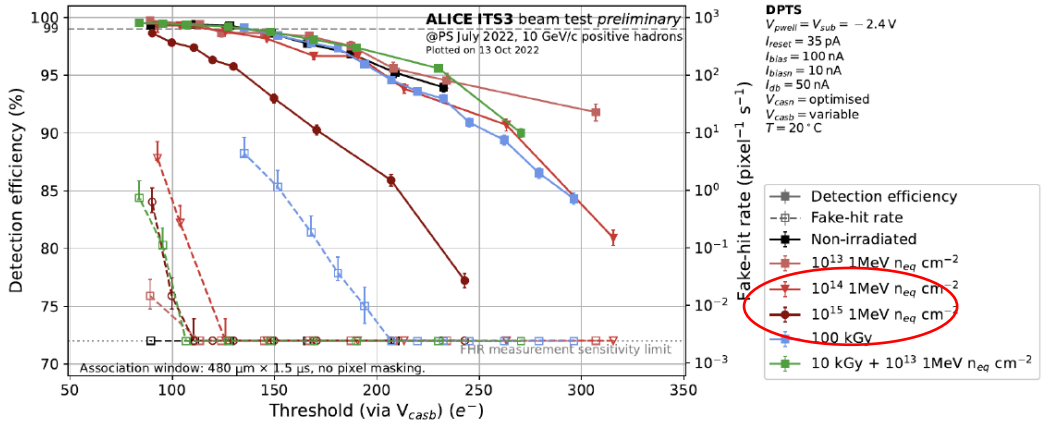


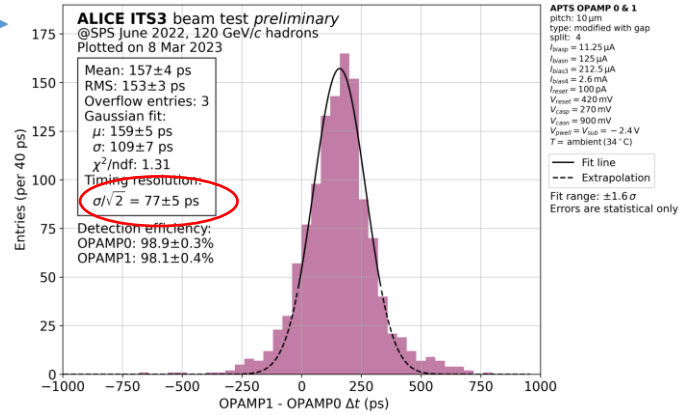


TPSCo-65 ISC technology features

- Fully efficient chain of optimized sensor, analog front end, digital readout in 15 x 15 µm2 pixel (DPTS)
- Circuit radiation tolerance TID in line with other 65 nm technologies (ringoscillators up to 25 % frequency degradation after ~800 Mrad)
- ~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature
- <100ps timing precision
- Multiple unexplored features
  - Stacked photodiodes
  - Gain
  - Wafer stacking
  - Etc.



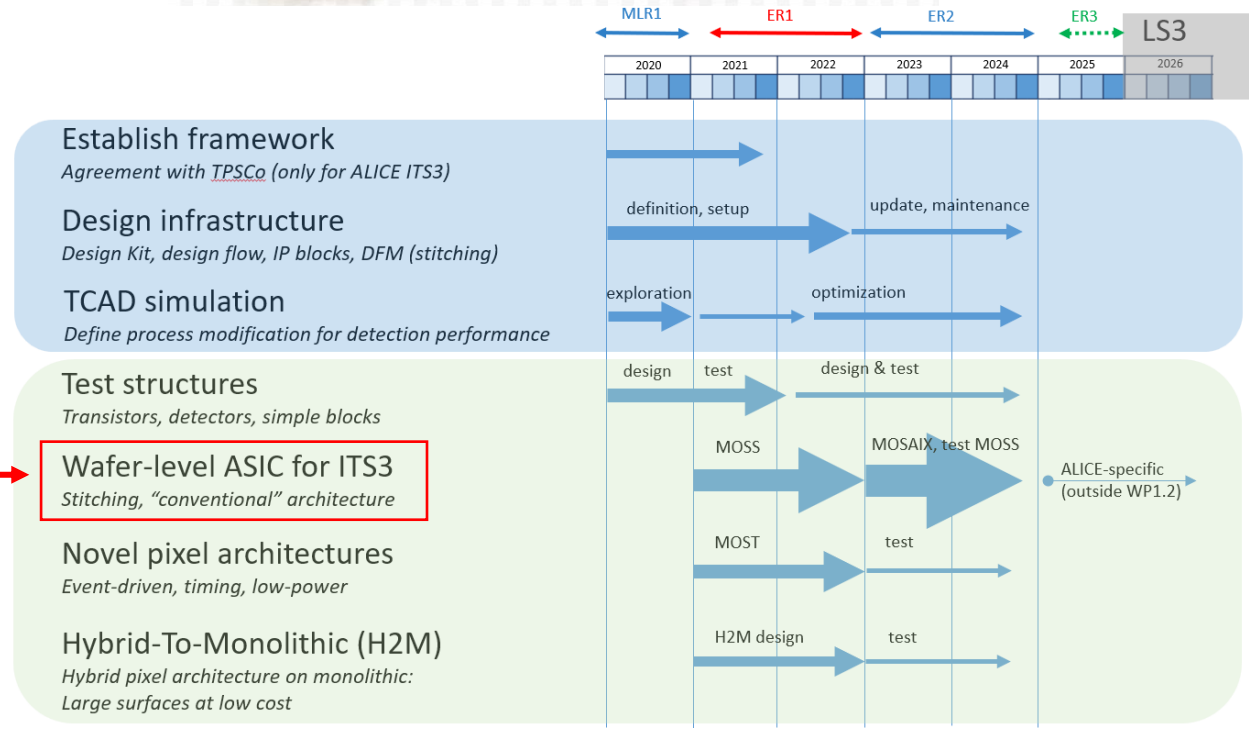




ER1 test results

a) CHIPLETS

b) MOSS TESTING OVERVIEW



MOSS Monolithic Stitched Sensor Prototype

WP1.2

EP R&D

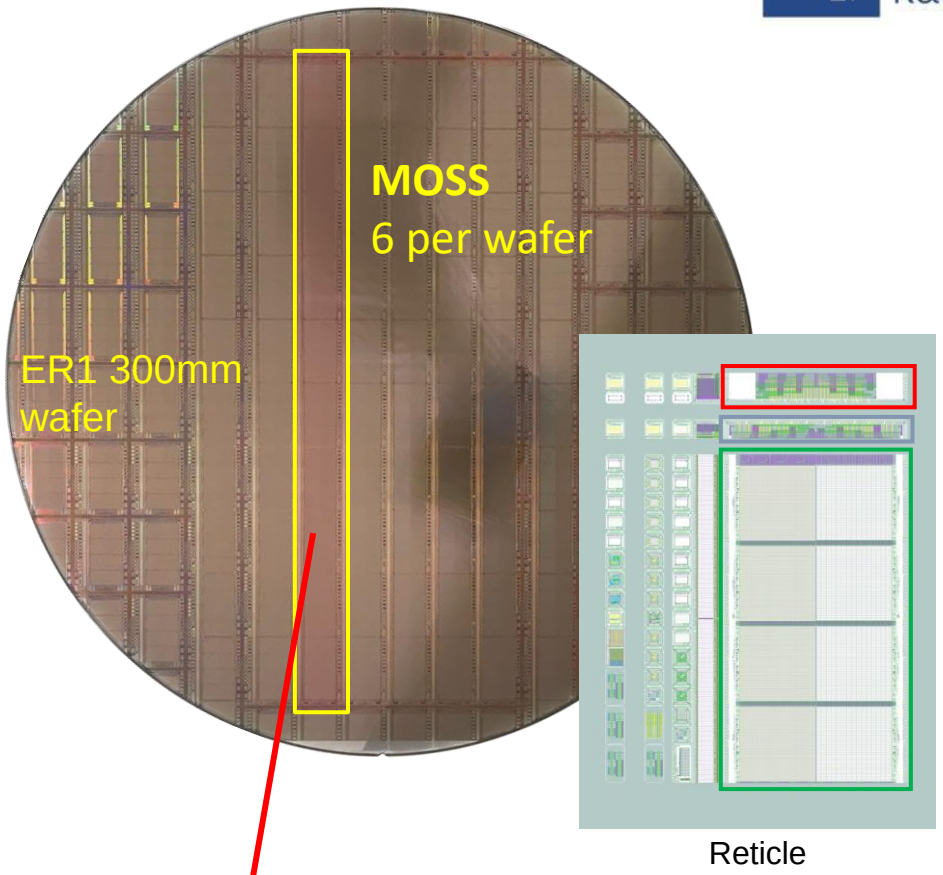
Goals

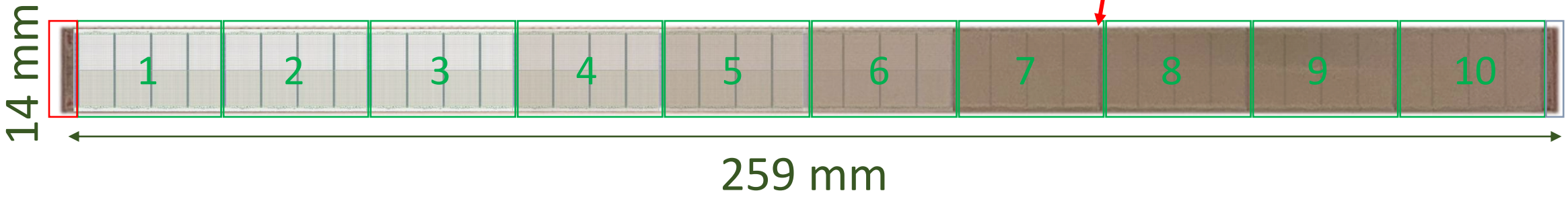
- Learn techniques to make wafer scale sensors
- Study yield, constraints, powering, spread of parameters

Repeated units abutting on short edges

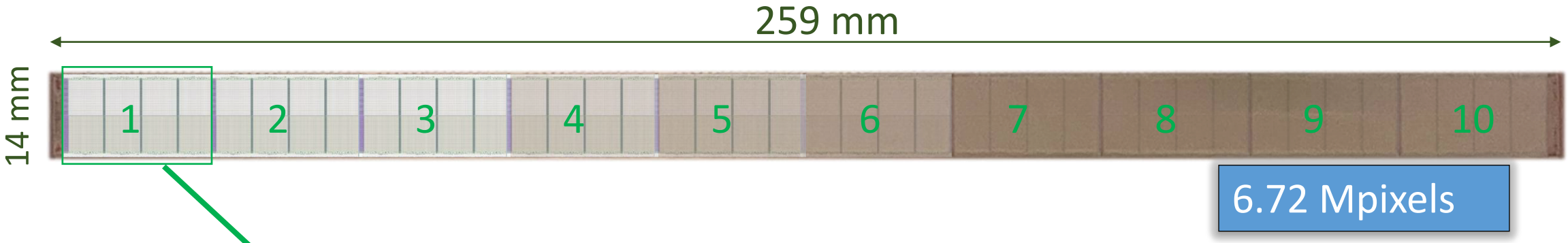
- 10 Repeated Sensor Units, 1 Endcap Left, 1 Endcap Right
- Metal traces cross stitching boundaries for power distribution and long range on-chip control and data transfer
- Module integration on wafer scale die for the first time
- 1/20 power segmentation

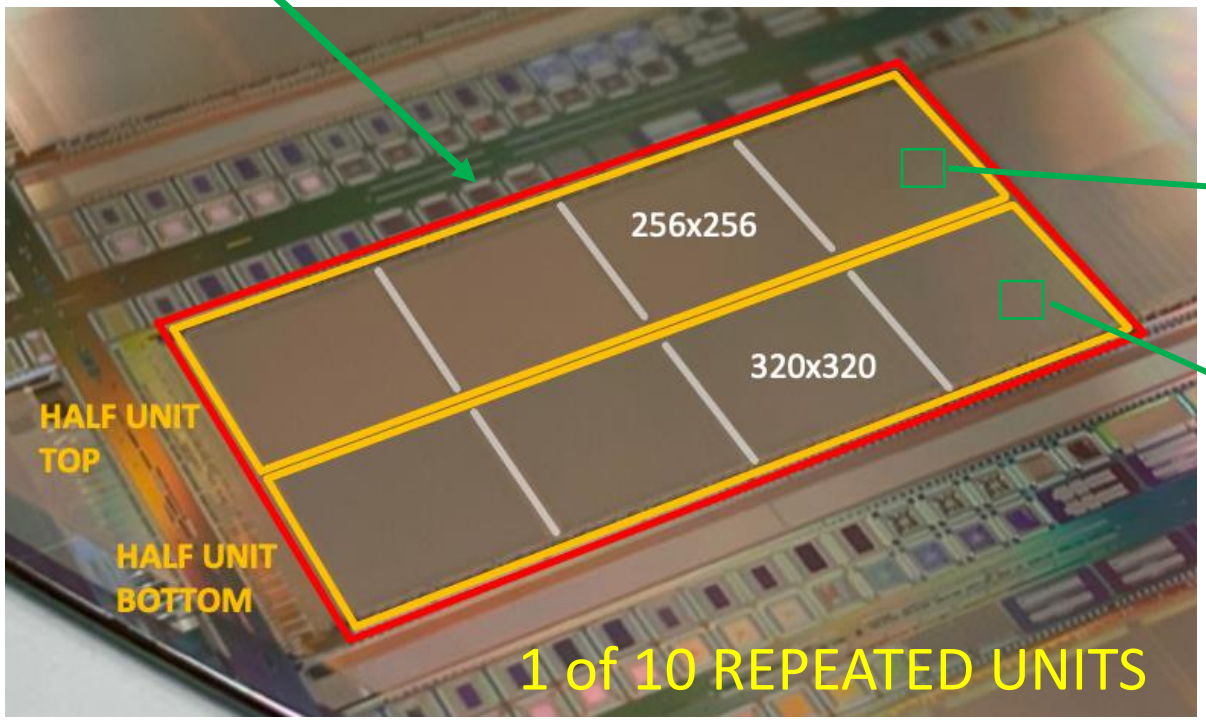
Submitted Nov 2022, Received May 2023



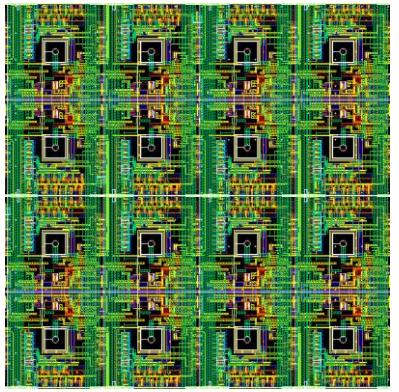


MOSS Layout

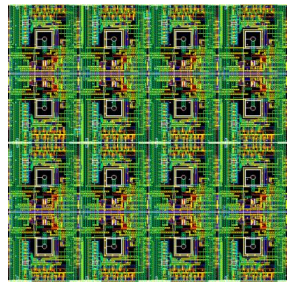




Large Pixel Pitch
22.5 µm



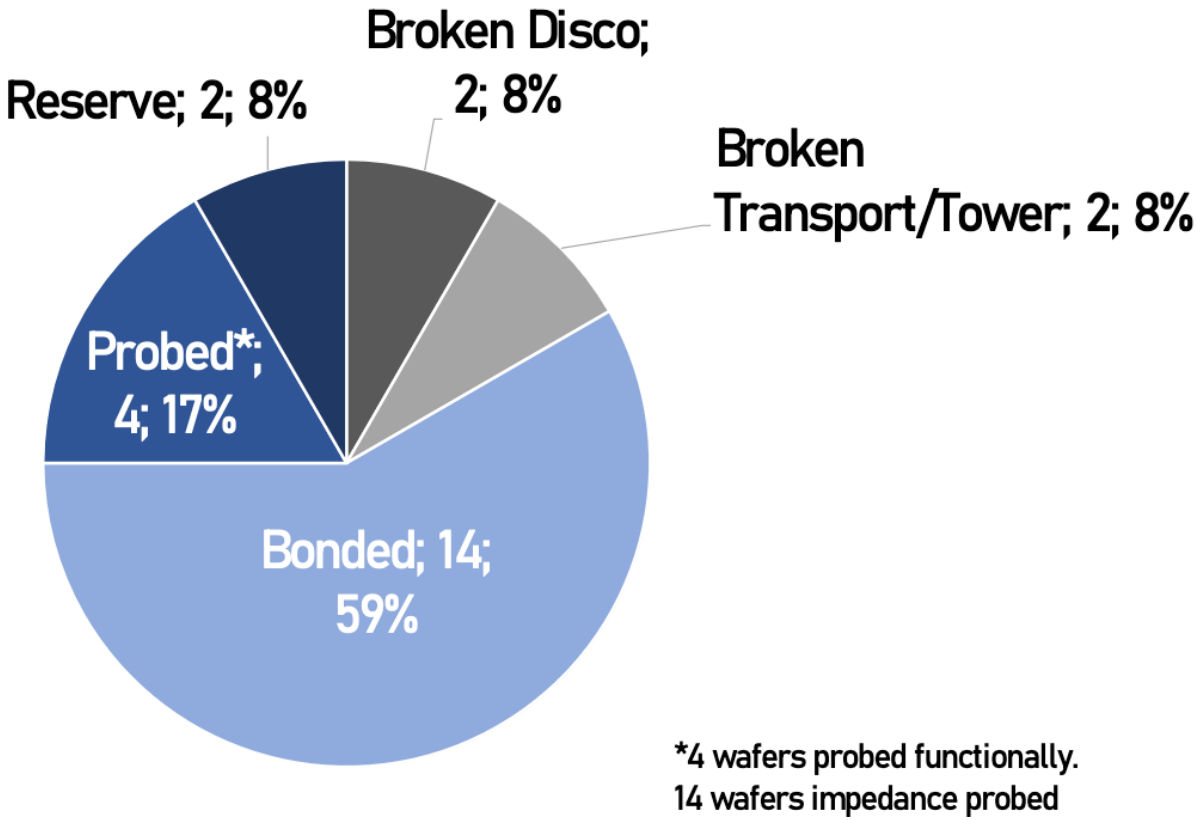
Fine Pixel Pitch
18 µm

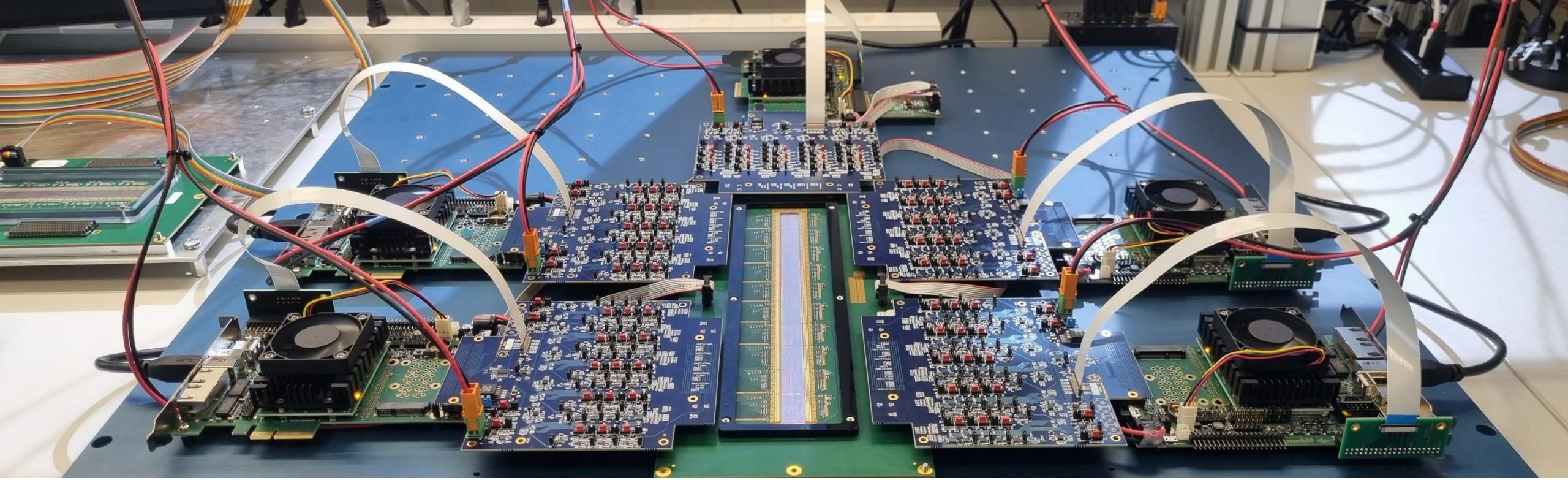


Investigate effects of layout density

ER1 Wafers and MOSS Under Test

- 24 Wafers manufactured
  - 4 broken
- Tests before thinning and dicing
  - Impedance tests (14 wafers)
  - Functional tests (4 wafers)
- Tests after thinning, dicing and bonding on carriers
  - 82 full size MOSS under testing, 2 broken
  - Many additional Single-Stitch MOSS
- A massive effort from ALICE community





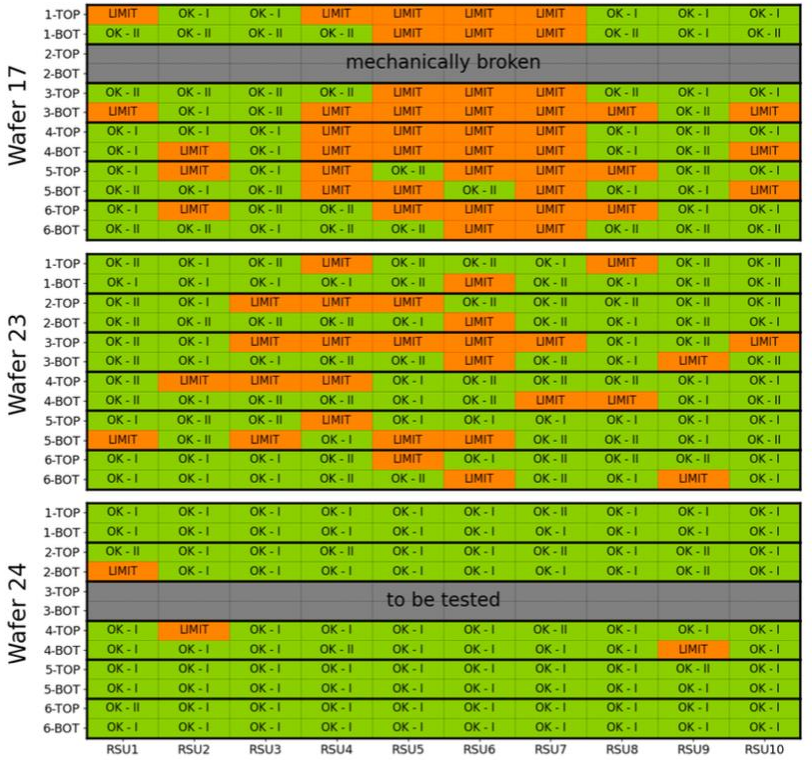
MOSS Functional Tests

- MOSS design fully functional
  - Design concepts and methodology validated
  - Block level yield and local defect rate under study
    - Faults probability seems negligible with respect to power shorts
  - No evidence of yield difference between the two layout densities
- Facts learned and proposed improvements to be used in the ER2 engineering prototype (MOSAIX)

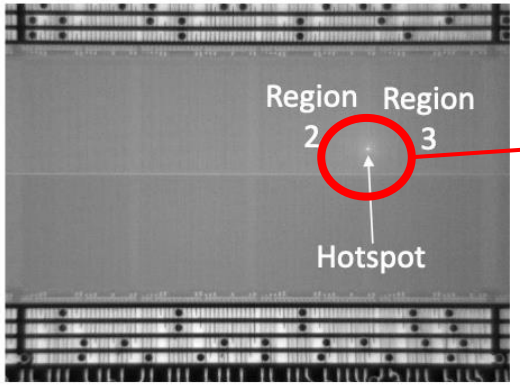
MOSS Testing – Powering Yield

- Dominant failure mode: short circuits between power nets
- Long and intense investigations. Finding: unexpected inter-metal vertical shorts
  - Related to manufacturing.
  - Wafer to wafer variations.
  - Followed-up with foundry. Expected to disappear or reduce with new metal stack and mitigation by layout
- Results before and after thinning and dicing consistent
  - -> No yield reduction due to wafer post processing

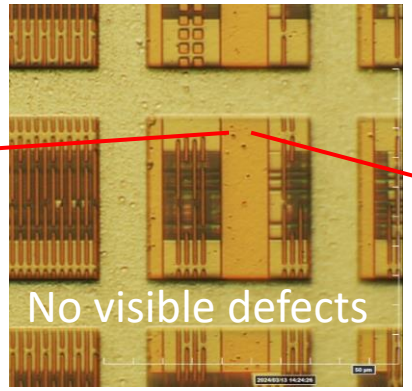
CERN-LHCC-2024-003 / ALICE-TDR-021
Powering tests from chips of the first three wafers tested.
The chips were thinned, diced, glued and bonded before testing.



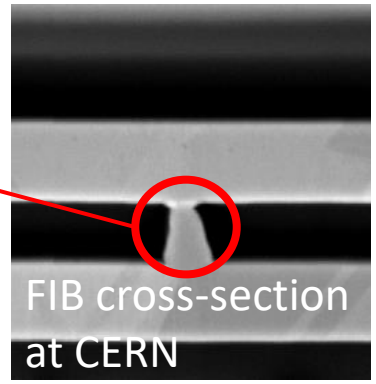
Thermal Imaging reveals shorts



Optical Microscope

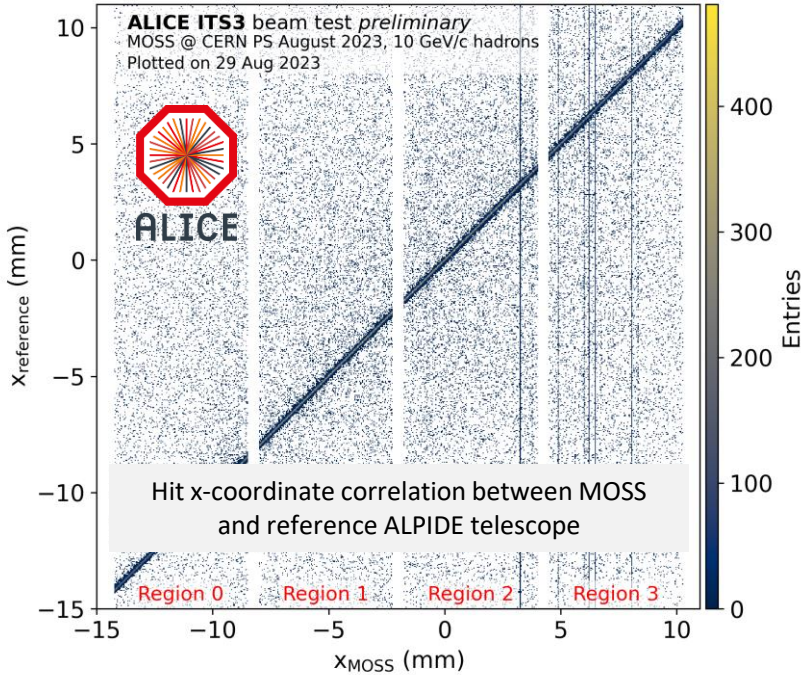


SEM image of metal-to-metal short

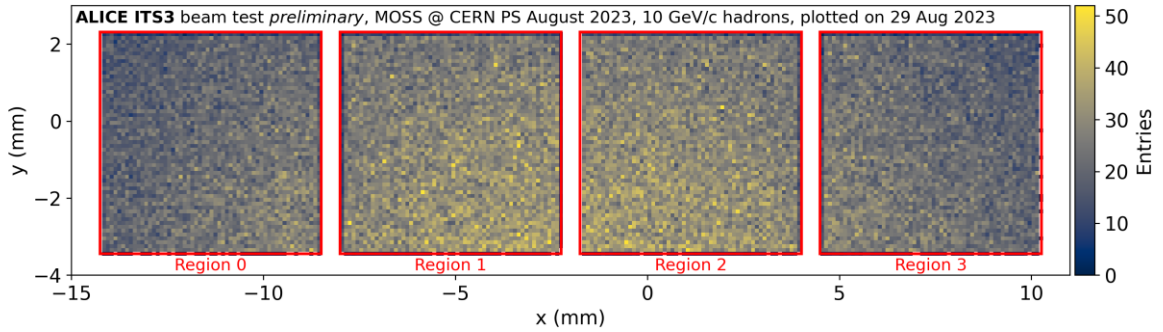


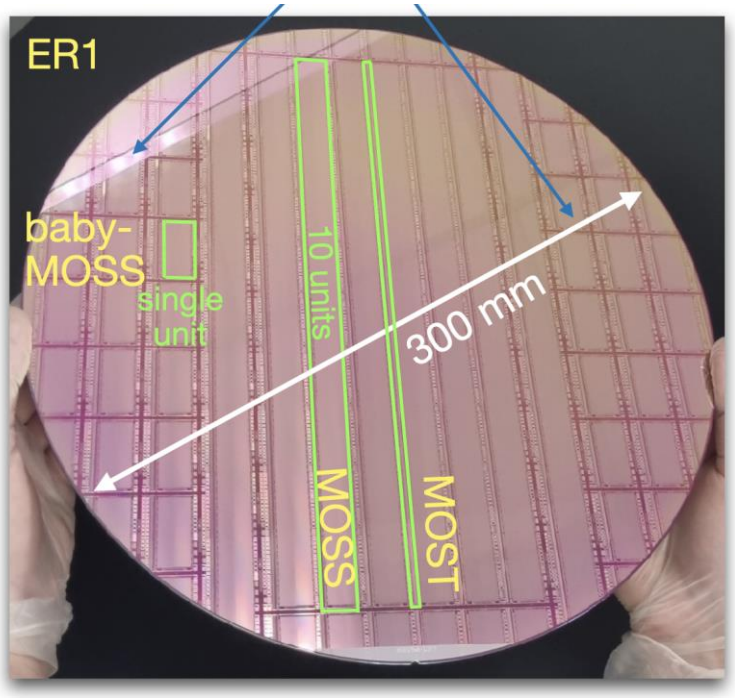
MOSS Characterization with Beams

- Sensor performance characterization ongoing
  - Based on laboratory measurements and multiple beam tests with Full MOSS and Single-Stitch MOSS
  - Studying detection efficiency, FHR, position resolution and tuning operating settings
  - Compare 6 variants of pixels × 2 process splits × Non-irradiated and NIEL Irradiated samples
- Cross sections of SEU and SEL events
  - Beam tests with Single Stitch MOSS
  - SEUs as expected
  - Indications of sensitivity to SEL, will investigate to localize and mitigate



Hit Map (1 HRSU, 4 regions)



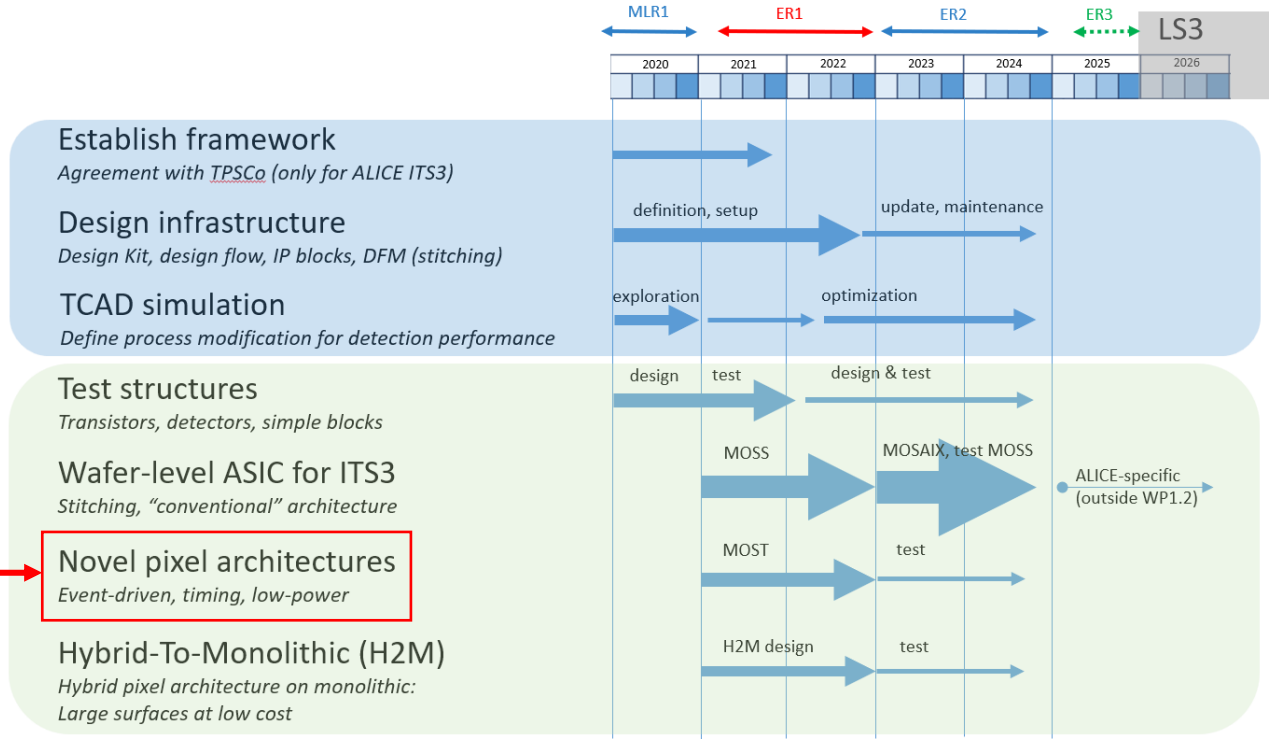


ER1 test results

a) CHIPLETS

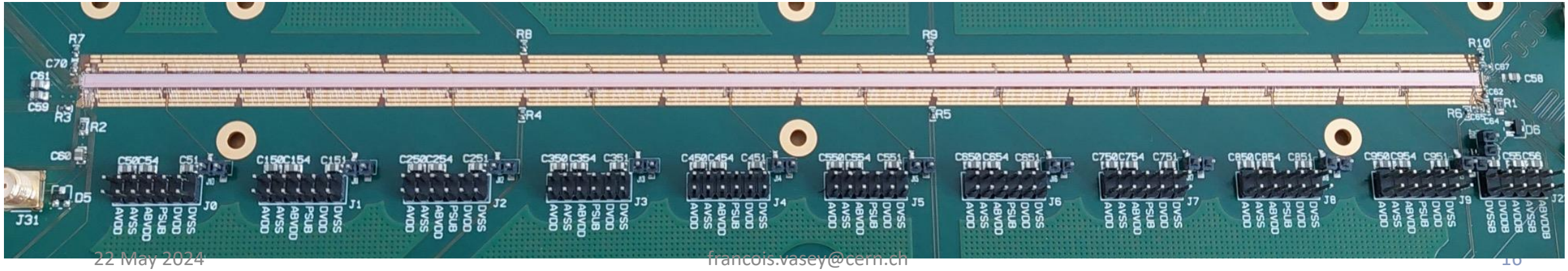
b) MOSS TESTING OVERVIEW

c) MOST TESTING OVERVIEW



MOST chip

- 2nd stitched chip on the ER1 run: 2.5 mm x 259 mm
- 10 repeated sensor units:
  - 18 µm pitch, very densely designed pixel matrix
  - Conservatively designed global power distribution + high granularity power switches to switch off faulty parts
  - Asynchronous, hit-driven readout, low power consumption + timing information.
- Measurements at CERN and at NIKHEF within the ALICE experiment.



MOST powering up measurements

WP1.2 EP R&D

- First measurements with early setup, new proximity board setup now coming online
- 9 MOST bonded
- All impedances have been measured and all chips were power-ramped.
  - 3 x DVDD trip with 50 mA compliance
  - 1 x AVDD trip with 50 mA compliance
  - 1 x DVDD trip on first ramp, ramps after that OK
  - 4+1 good ramps

    4 x respond to slow control
- More chips are being prepared for testing (carriers + glueing + wire bonding).

MOST Sequential power release

WP1.2

EP R&D

- Nothing anomalous observed so far
- No chip found which cannot be fully powered once passing the initial ramp

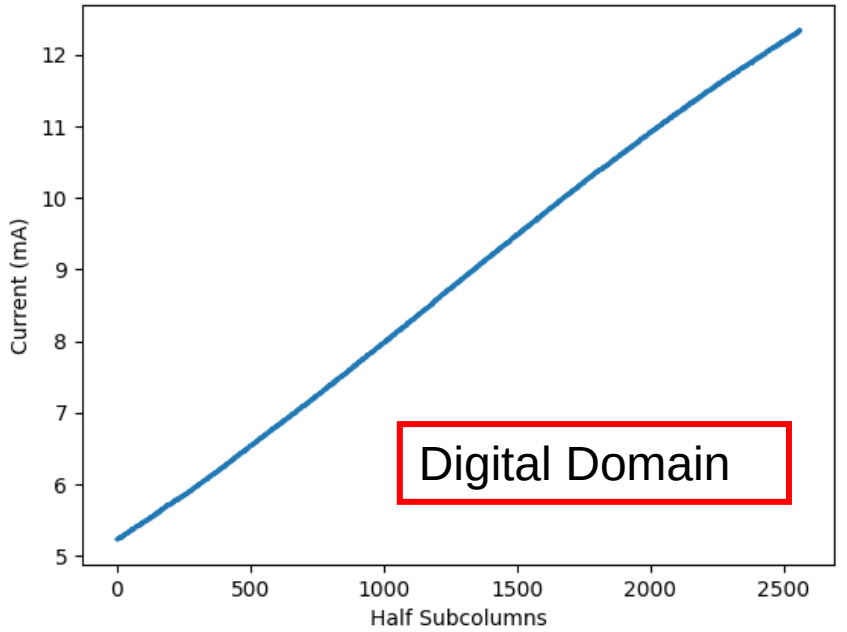
  -> in line with vertical shorts observed

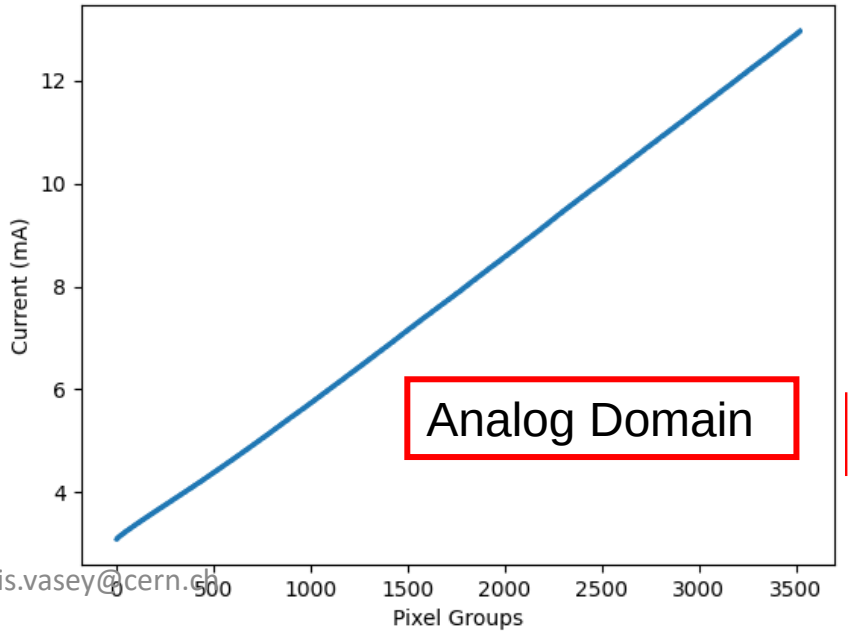
- 1 digital switch per 352 pixels

  2560 total
- 1 analog switch per 256 pixels

  3520 total

- Pixels next to powered down pixels behave normally from an electrical point of view (only tested so far on split without low dose deep implant in the pixel matrix).

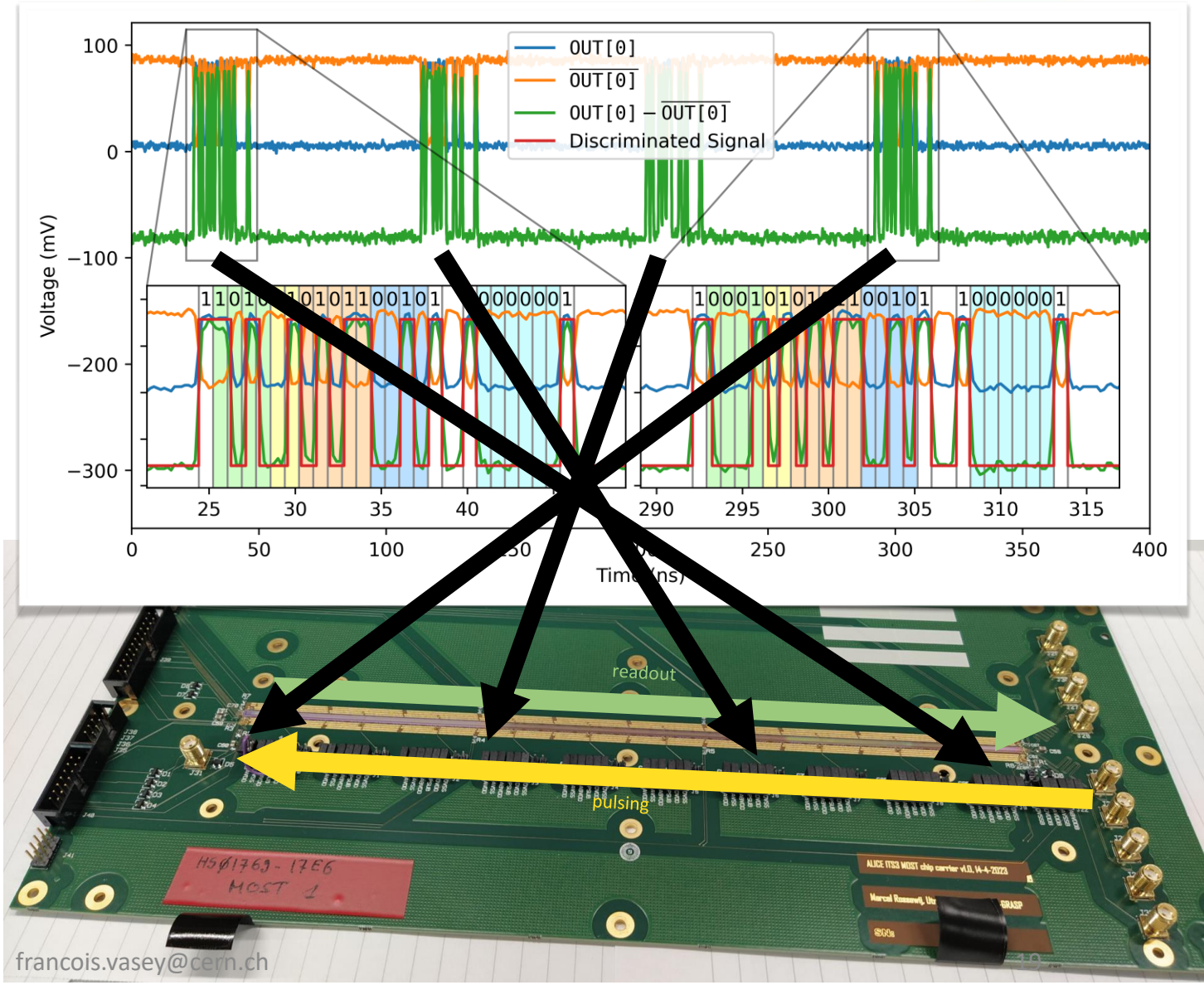




MOST Pulsing & readout

WP1.2 EP R&D

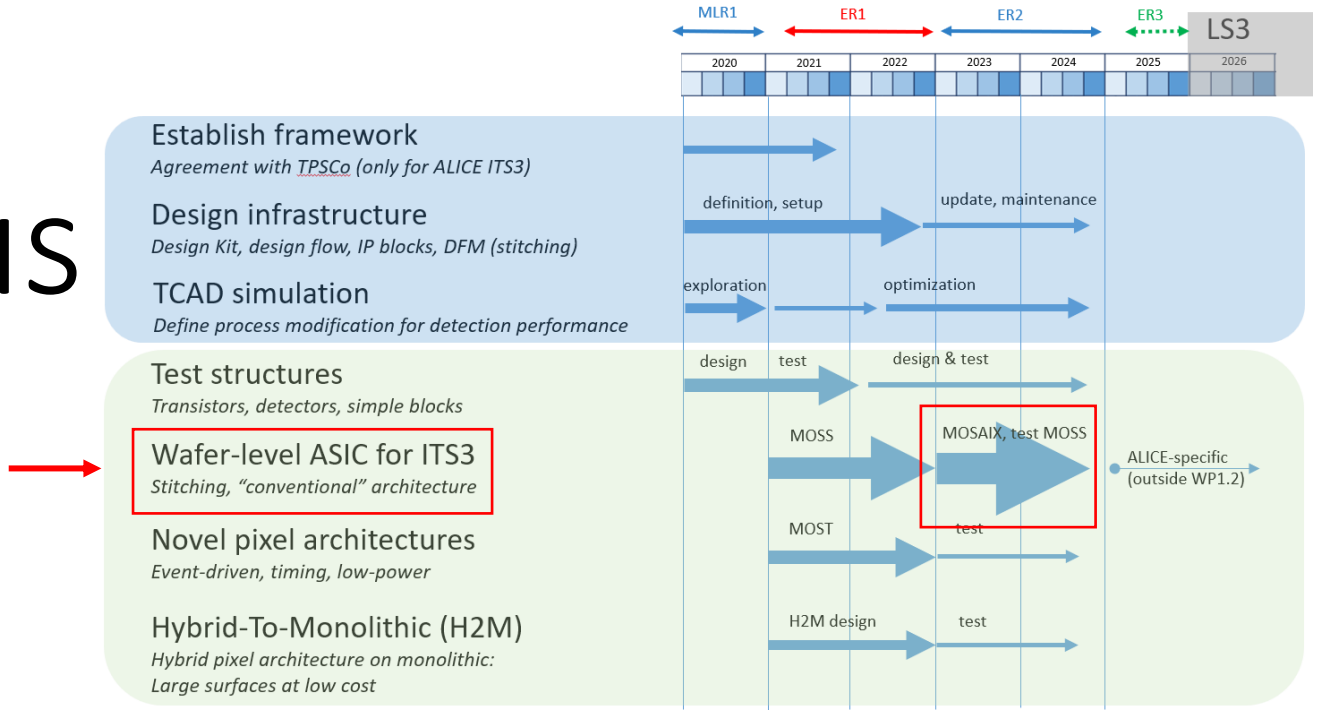
- All 256 readout lines work across the full length of the chip/across all stitches
- About 300 ns delay between pixels pulsed at the left and at the right of the chip (right is near input and output)
- Chip is functional, including front ends, pixel address is sometimes only transmitted partially due to a marginality in the design.



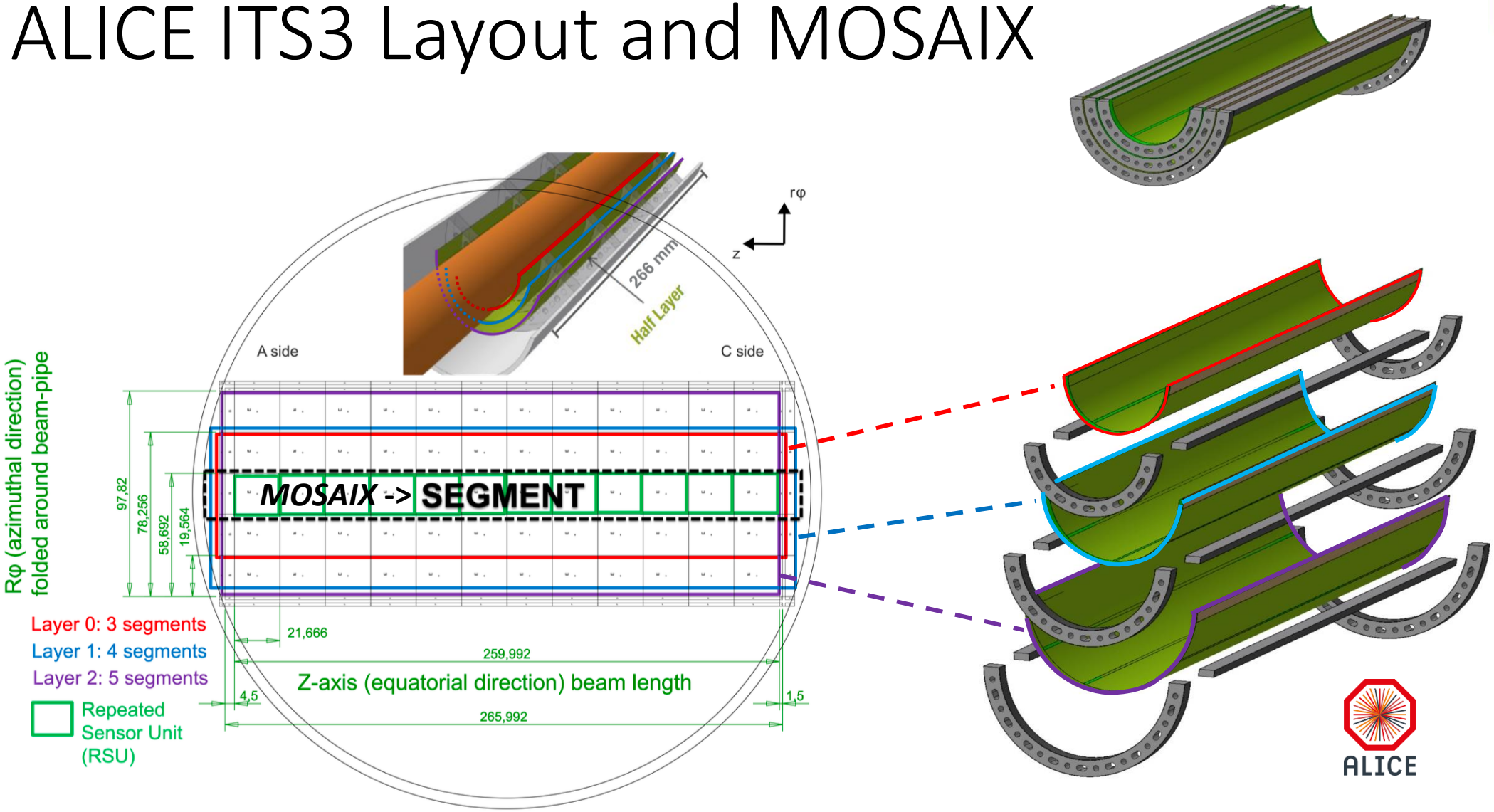
francois.vasey@cern.ch

ER2 design status

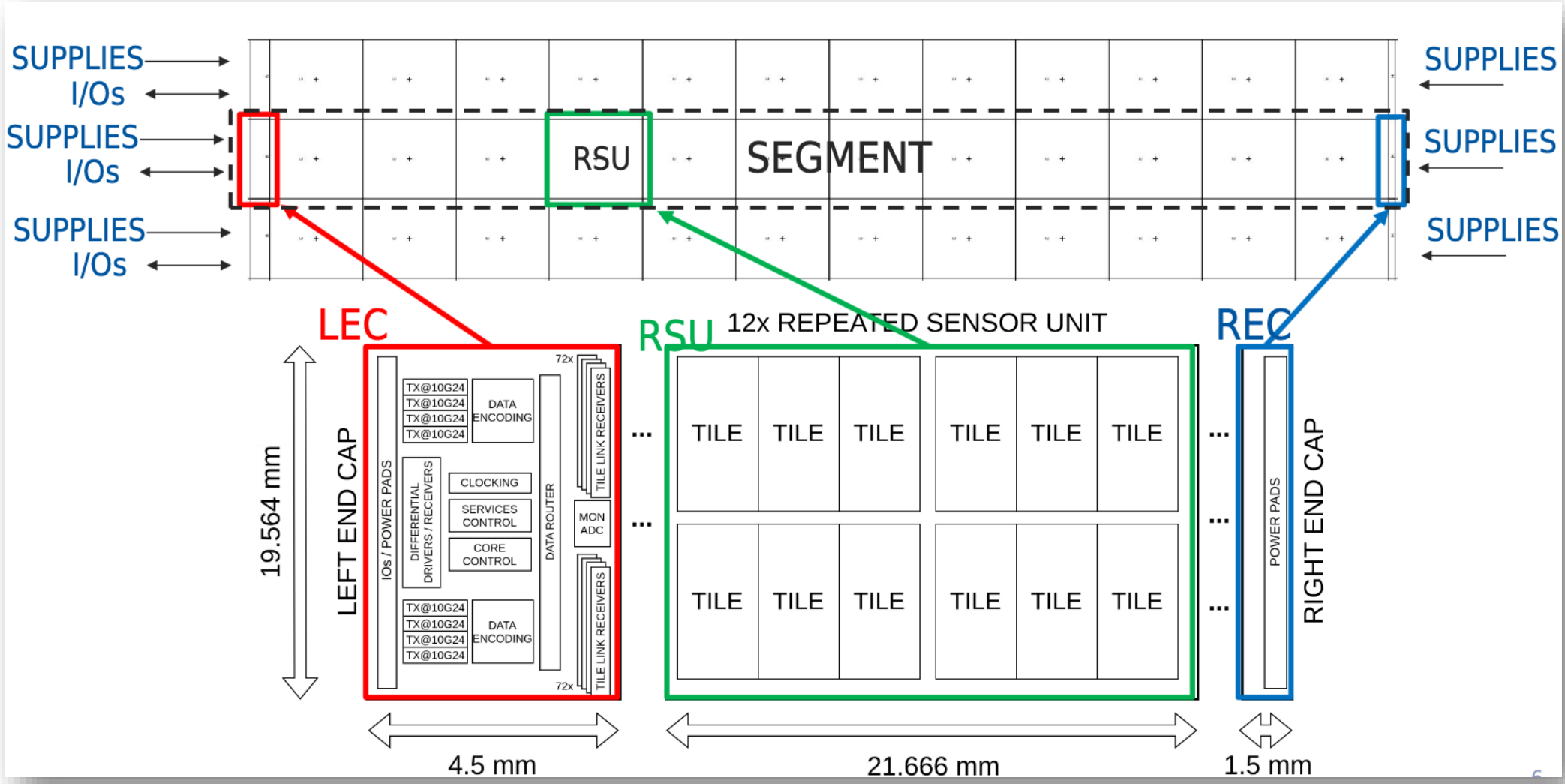
a) MOSAIX STATUS



ALICE ITS3 Layout and MOSAIX



MOSAIX Architecture



MOSAIX Summary

- MOSAIX Design
  - Prototype and study phases completed
  - Architectural and Detailed specifications completed
    - Done three Shared Brain Sessions **Technical Reviews**
    - Done ALICE MOSAIX engineering **Specification Design Review**
  - Detailed design of blocks progressing in parallel, completion of a large set expected by **end of June**
  - Some components on critical path or expected late (end of July)

- Ahead:
  - Migration to new metal stack. Depend on release of PDK and DDK by the foundry (June)
  - Complete design entry
  - Full chip verification and sign-off phase

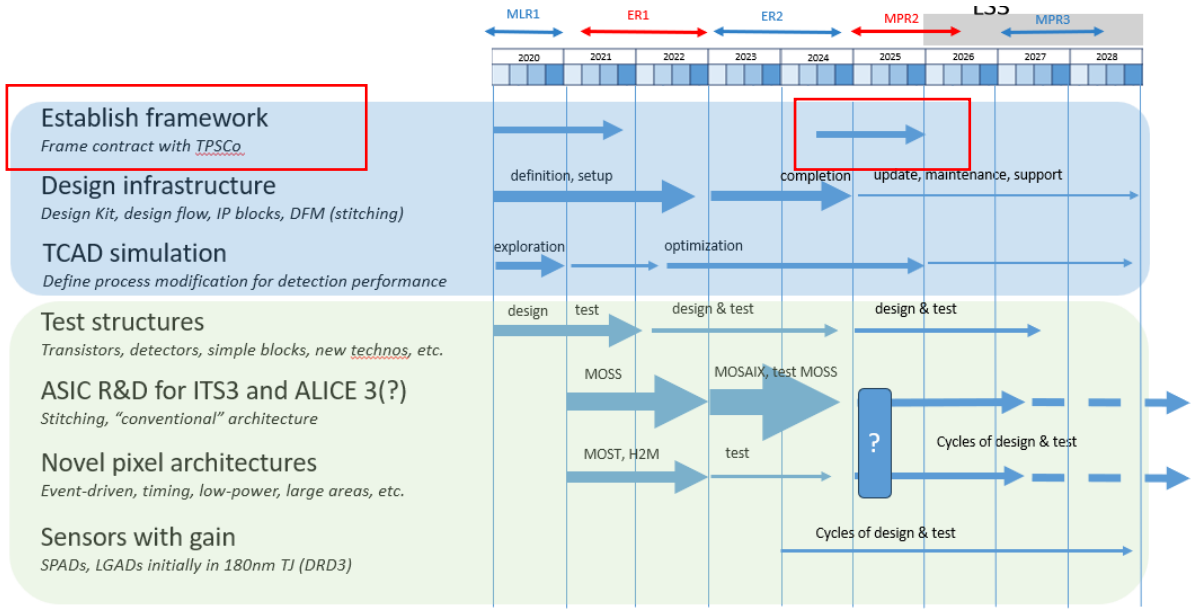
- MOSAIX design to be completed by July 2024, then sign-off and reticle integration
  - A collective effort: CERN, BNL, INFN, IPHC, MIT, Nikheff, RAL, …

- Targeting ER2 submission by end of October 2024

ER2 design status

a) MOSAIX STATUS

b) DESIGN FRAMEWORK



TPSCo65 Design framework

- TPSCo. offers a mixed-signal design kit:
  - PDK (Physical Design Kit) for analog designs
  - DDK (Digital Design Kit) for digital designs
  - IP blocks (std cells, I/O pads, SRAM/ROM compilers, eFuses)

- CERN has a collection of tested in-house macrocells, custom std cells, custom DRC/LVS decks & RTL2GDS workflow
  - These tools are to be made available to the community for MPR2
  - Digital flow based on CERN ASIC support flow
  - Early access is already possible

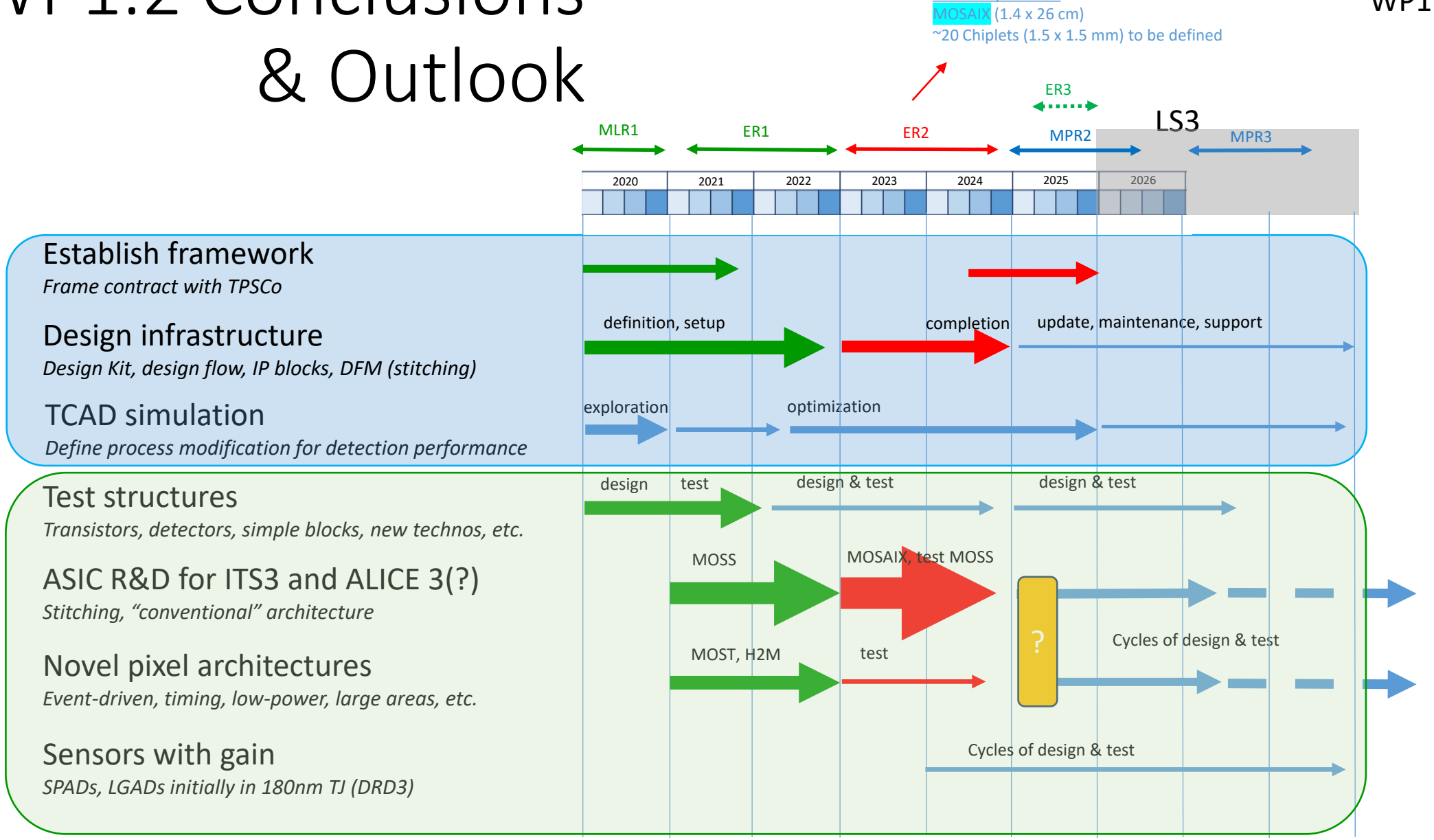
- Modified process enables optimized sensor performance

CERN RTL2GDS workflow

- The workflow consists of:
  - Template scripts for digital on top implementation (flowkit from Cadence is used)
  - Bookkeeping of tech and design files (tmake tool, https://cern.ch/tmake)
  - Possibility to triplicate the design using the TMRG tool (https://cern.ch/tmrg)
  - Versioning of Open-Access library via ClioSoft SOS
  - Set of signoff checks to perform
    - Guidance on custom DRC/LVS decks for yield and latchup immunity improvements
    - Power analysis signoff
    - SEE simulations for radiation hard designs
  - Documentation
- The goal is to empower the user with a workflow capable of rapid digital design prototyping, guiding the user from start to finish.
- Support to be deployed through CERN-ASIC-Support framework, as contribution to DRD7.6 Work Package

WP1.2 Conclusions & Outlook

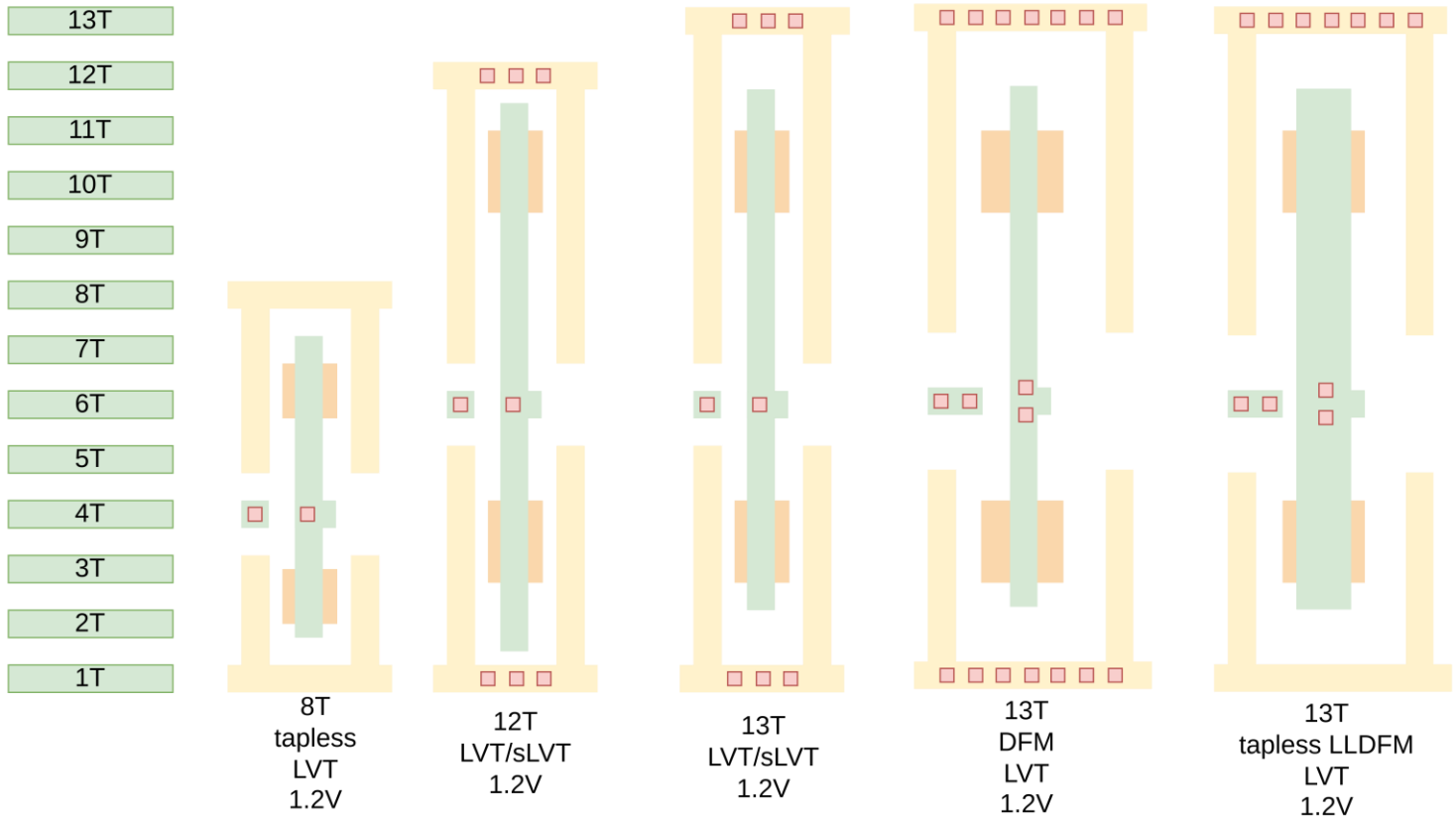
WP1.2 Conclusions & Outlook



Backup slides

TPSCo65 Design framework

- A wide variety of digital standard cells are available:
- 8 track, high density [custom]
  - low-VT, 1.2 V
  - tapless, allows reverse bias
  - targets in-pixel logic
- 12 track & 13 track
  - low-VT and super-low-VT, 1.2 V
- 13 track, DFM [custom]
  - DFM, low-VT, 1.2 V
  - targeted to comply DFM rules
- 13 track, DFM [custom]
  - DFM, low-leakage, low-VT, 1.2 V
  - tapless, allows reverse bias
- 22 track (not shown)
  - HV, 3.3V compatible
  - targets 1.8-3.3V power domains



RSU Architecture

WP1.2

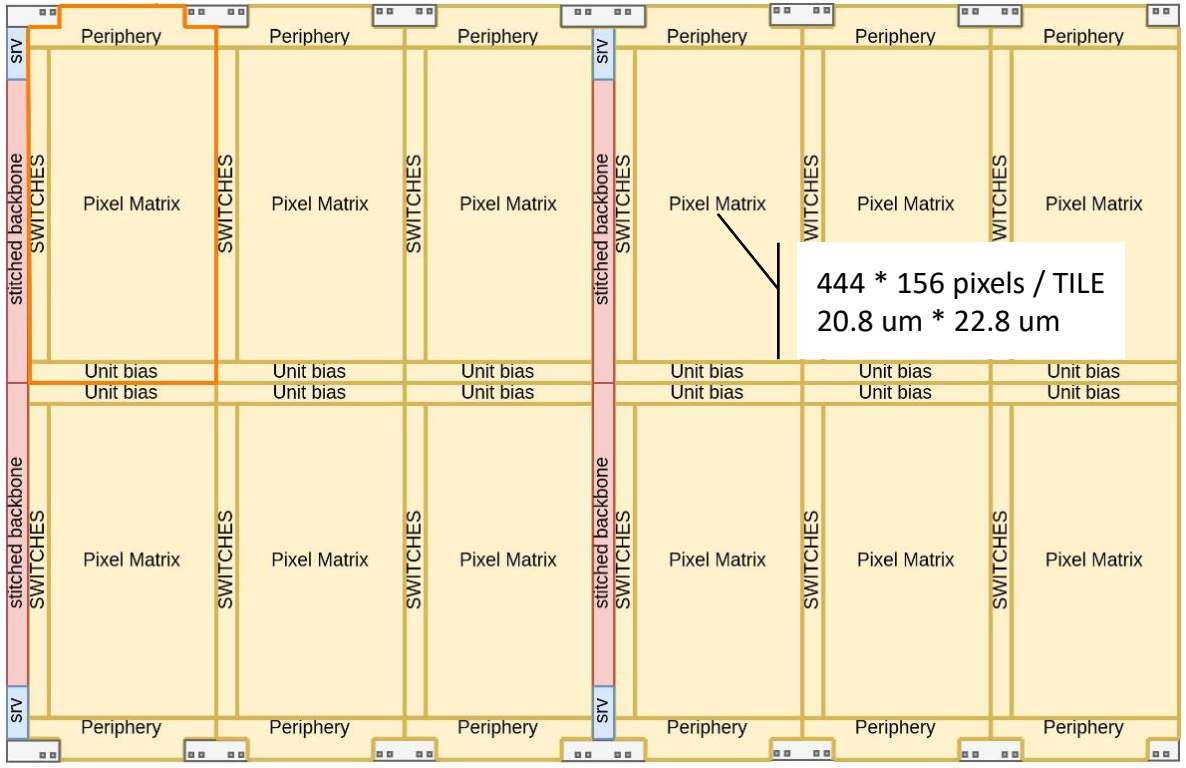
12 RSU per segment

12 TILEs per RSU

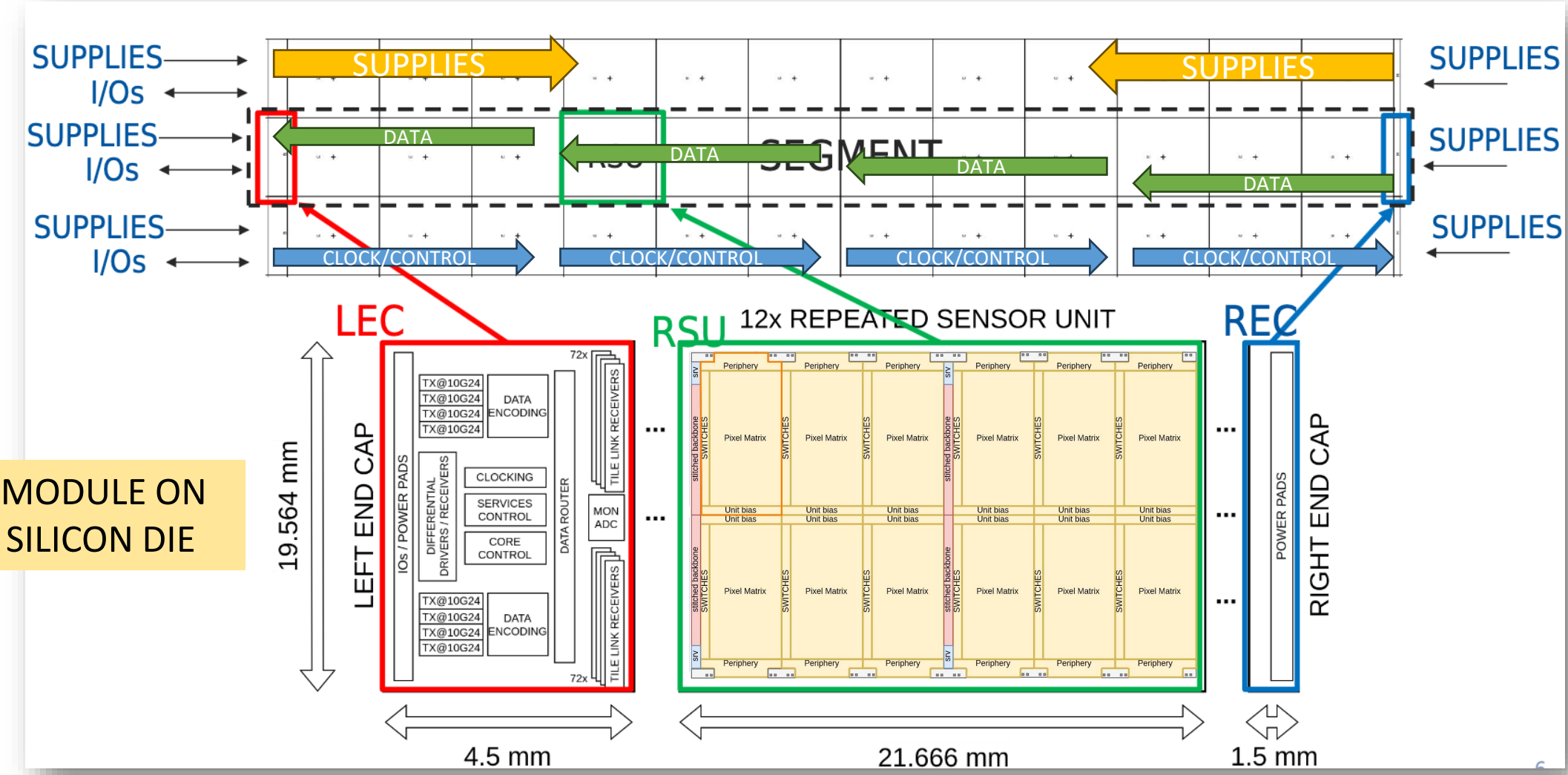
TILEs can be switched on, biased and read out independently

One TILE is 1/864=0.116% of L0 acceptance

TILE



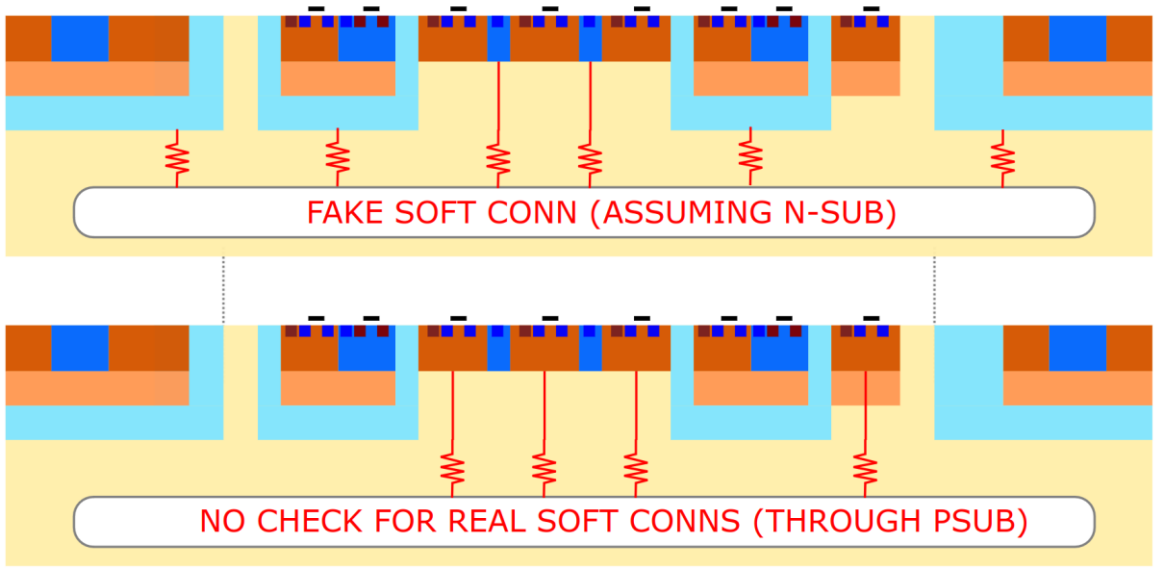
MOSAIX Architecture

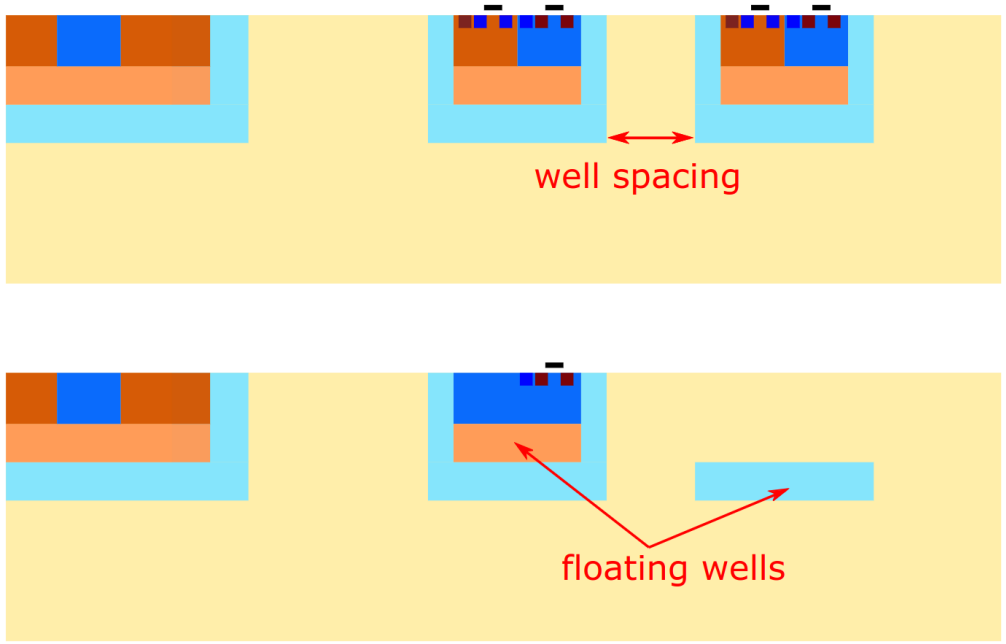


FULL MODULE ON ONE SILICON DIE

TPSCo65 Design framework

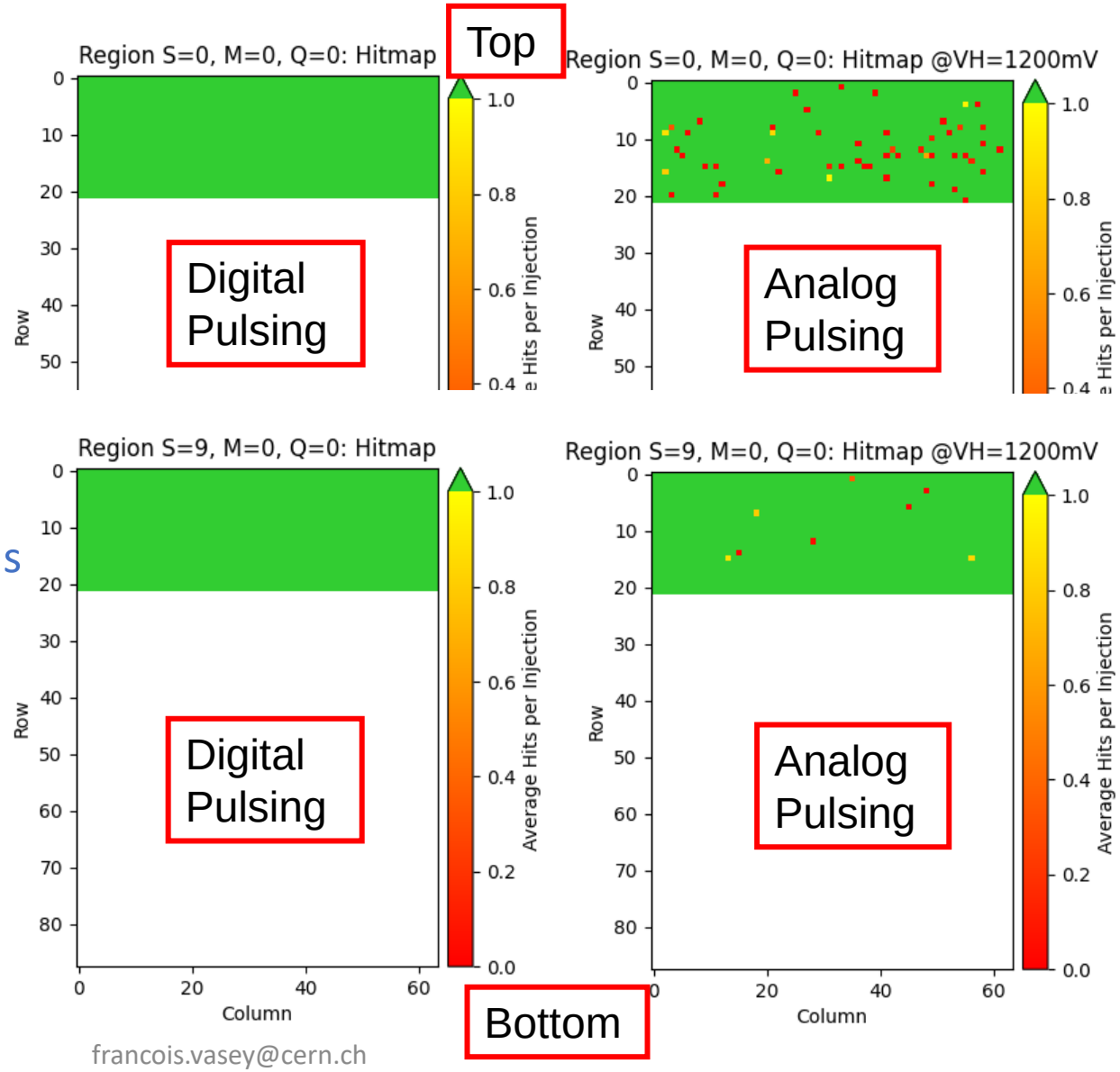
- Custom LVS & DRC rule decks available and integrated into Calibre





MOST Pulsing

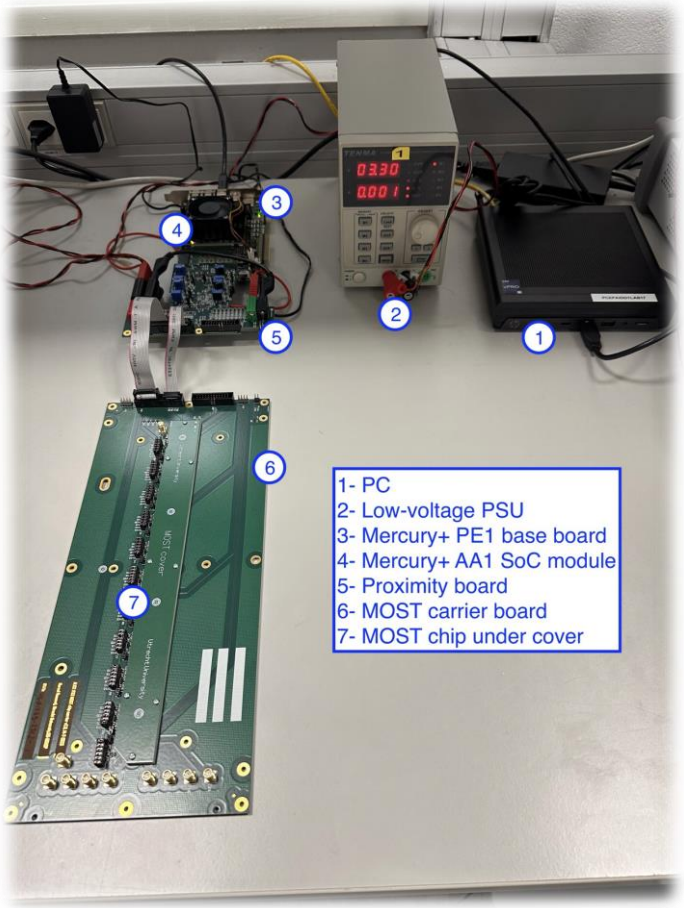
- Pulsing
  - Analog: charge injection
  - Digital: bypassing frontend
- Initially some pixels did not respond to charge injection, see right, now fixed, was biasing issue
- For all tested chips, all 256 global transmission lines (M4) are functional.

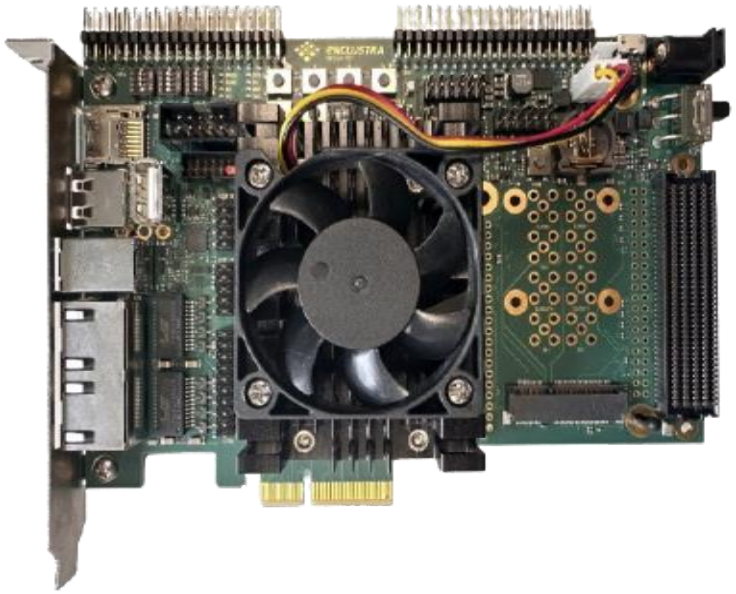


Measurements Nicolas Tiltmann

francois.vasey@cern.ch

MOSS and MOST test setup development





Base board

- Mercury+ PE1 base board
- Mercury+ AA1 SoC Module
- USB connection to PC
- FMC connection to Proximity board • Needs FX3 + MOST firmwares

Proximity board

- 1 x DAC63004 for VDD supplies
- 2 x AD5668 for bias supplies
- 1 x AD7091R for current monitoring
- VDD regulators + Digital buffers
- FMC connection to base board

- Firmware/software development Younes Otarid (several elements from ALICE)
- Carrier and proximity board design (Marcel Rossewij Nikhef)