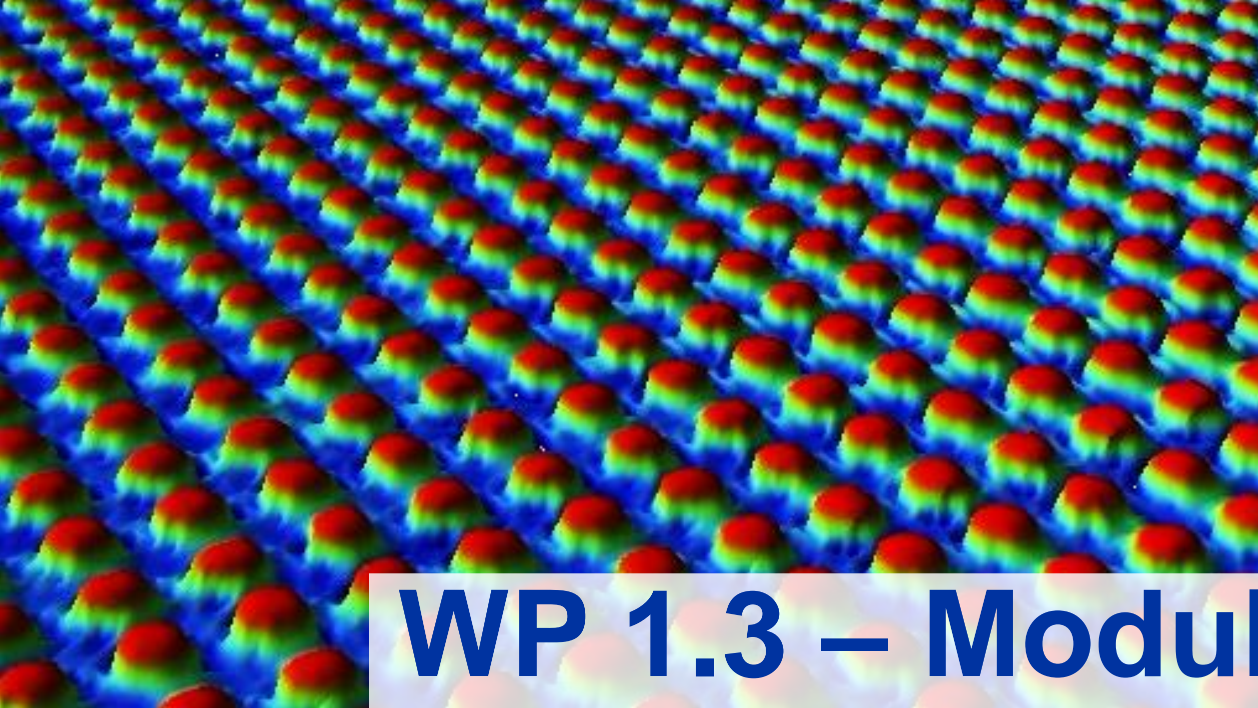
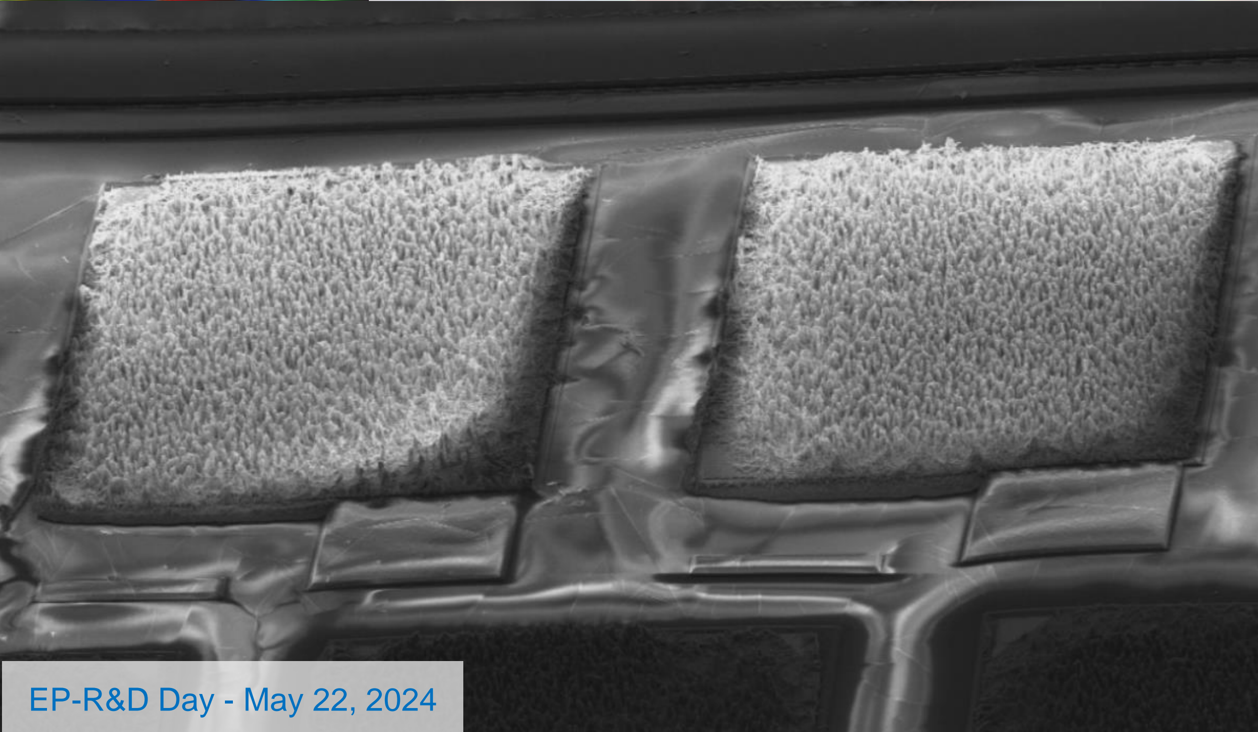
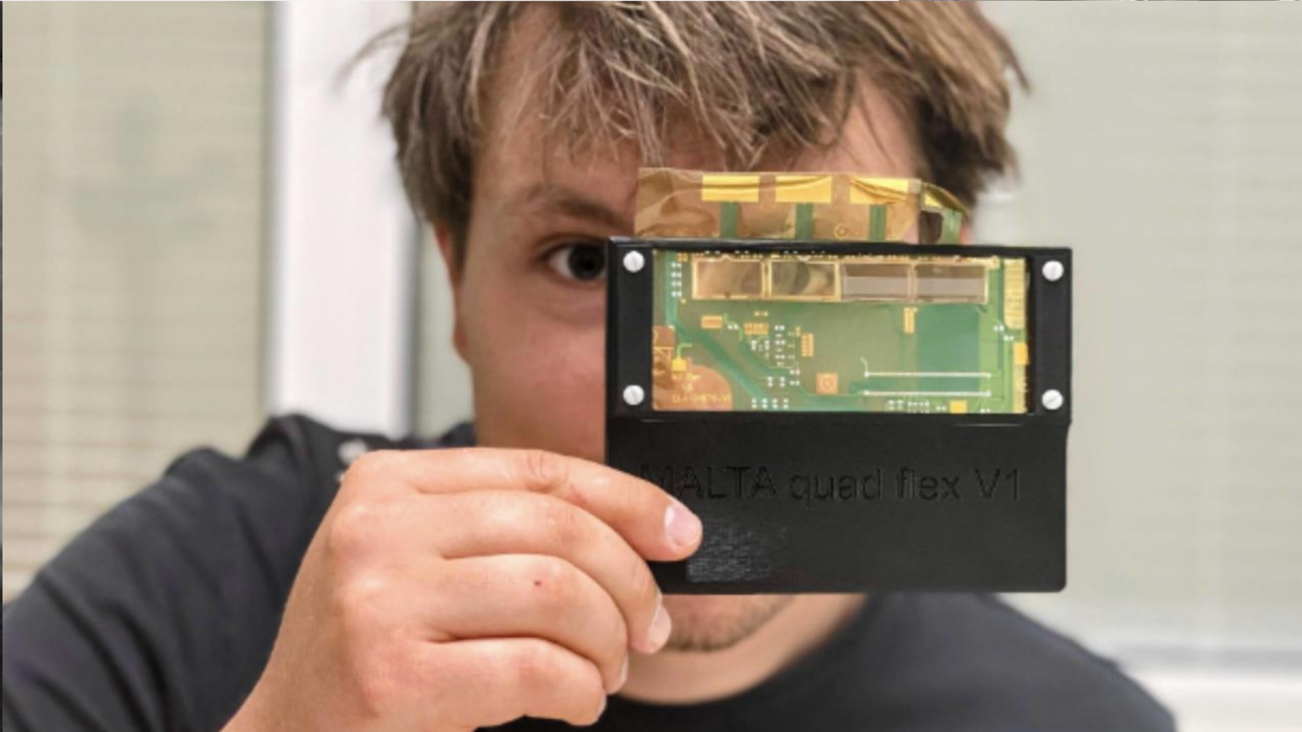


WP 1.3 – Module Development

Introduction
D. Dannheim, P. Riedler

Plating
Ahmet Lale, Haripriya Bangaru

Hybridisation
Peter Švihra

Module interconnection, flex developments
Julian Weick, Abhishek Sharma

Plans and Conclusions
D. Dannheim, P. Riedler

WP 1.3 Team

- Diverse team with contributions from **CERN staff, users, students and fellows**
- 2 FTE fellows + 2 FTE students from WP 1.3 funds

Current WP 1.3 core team

Current contributors:

Haripriya Bangaru (TECH), Ruddy Costanzi (STAF), Dominik Dannheim (STAF), Ahmet Lale (FELL), Florentina Manolescu (STAF), Robert Munzer (USER), Rui de Oliveira (STAF), Marcin Poblocki (STAF), Petra Riedler (STAF), Abhishek Sharma (STAF), Peter Švihra (FELL), Milou van Rijnbach (FELL), Mateus Vicente (USER), Julian Weick (FELL), Xiao Yang (FELL)

Former team members 2020-2023:

Justus Braach, Florian Dachs, Janis Schmidt, Alexander Volker, Morag Williams

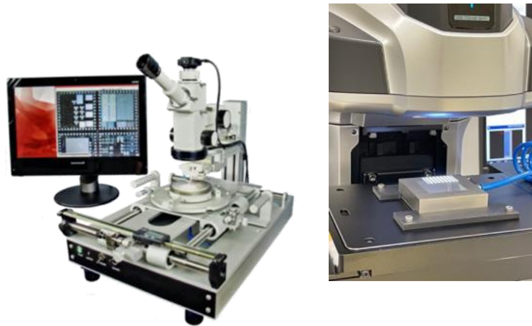
WP 1.3 Scope and Collaborations

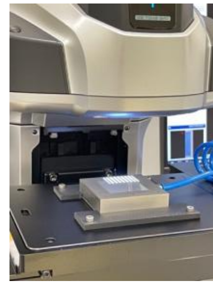
Study and development of **new modules** for hybrid and CMOS pixel detectors:

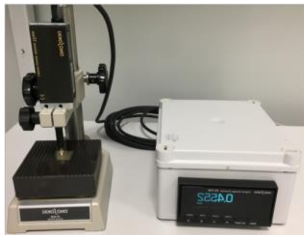
- Build flexible **in-house hybridization and module concepts** using existing prototype chips and sensors
- Working closely with **other silicon WPs**, **institutes** and **collaborations** to develop concepts
  e.g. University of Geneva, LPNHE Paris, CEA Saclay, ESRF, University of Oslo, INFN Cagliari, CTU Prague, AIDAinnova
- Links with **industrial partners**, to develop, tune and test technologies / products & processes
  e.g. DISCO, Dexerials, Conpart, FBK, Hybrid SA, IZM , Optim, PacTech, Hitech, Nanowired, SCS/Comelec
- Collaborating with **CERN services**, to develop procedures and processes, analyze material
  e.g. Micropattern lab EP-DT-EF, Bondlab, QARTlab, BE-CEM-EPR or EN-MME

WP 1.3 Infrastructure & Investments

- Cost sharing with projects/experiments optimizing **synergies** and common needs
- Dedicated area in the DSF cleanroom for **common equipment**
- Tools are supported for general use→ build up knowledge, experience & **training** opportunities across projects (e.g. ALICE, ATLAS, CMS, LHCb, 100muPET)
- Regular use of silicon processing infrastructure available at **CMi EPFL** and **Campus Biotech** Geneva







Instruments available in the DSF:

Instrument	Model	Year	Contributions
3D Metrology Scanner	Keyence VR-5200	2020	WP 1.3, ATLAS
Plasma Cleaner	Henniker HPT 500	2020	WP 1.3, DT
Wafer Thickness Measurement	Ono-Sokki	2021	WP 1.3
Micro Diamond Scriber	MR200	2021	WP 1.3, DT
Die Ejector Chuck	SemiCorp	2022	WP 1.3
X-ray Imaging System	Nikon XT V 160	2022/23	WP 1.3, DT, ATLAS, CMS, ALICE, LHCb

Planned shared investments for phase II:

- Inspection system for micro/nano structures
- Multi-module test system
- Clean area (tent with laminar flow) for DSF
- New flip-chip machine with improved performance

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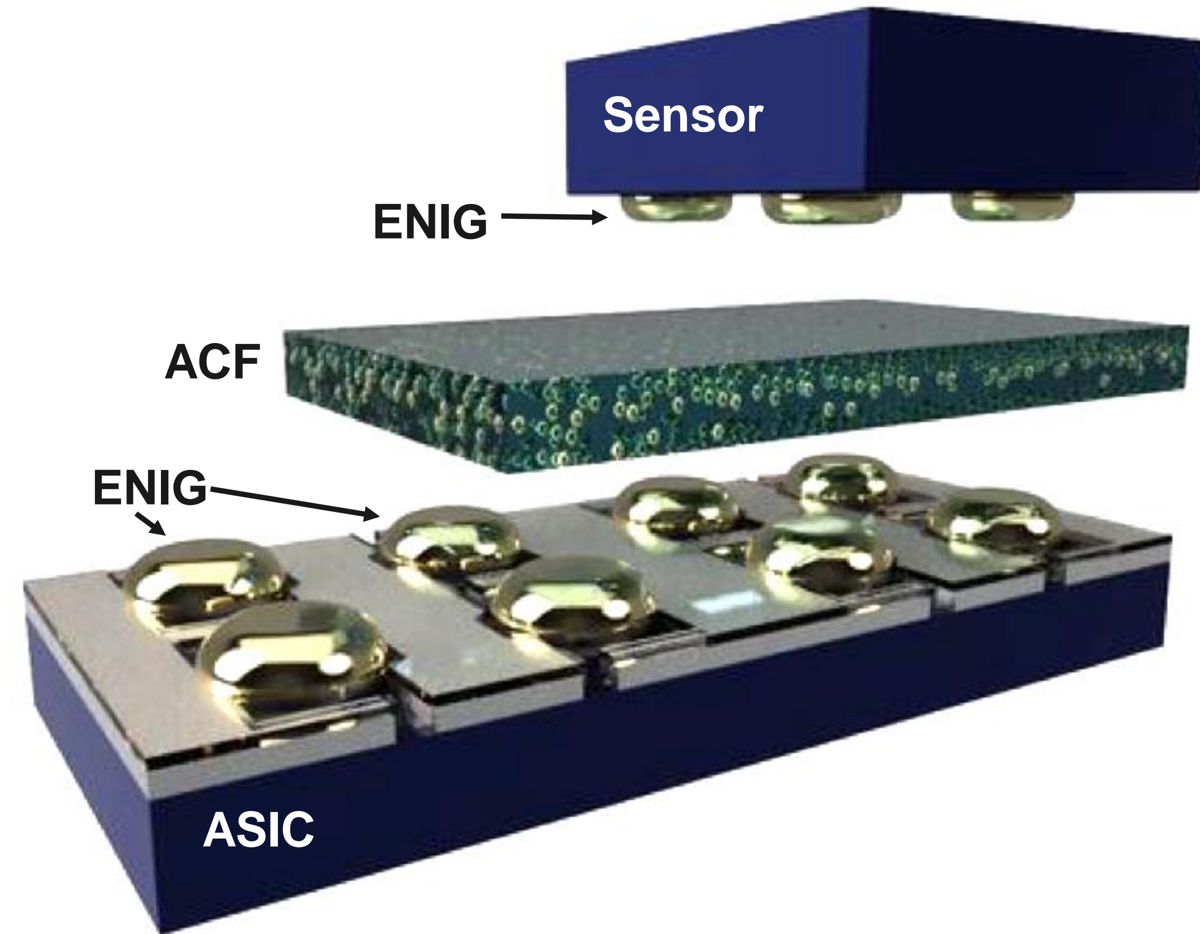
Introduction

Development of an in-house module hybridization technique in two main steps:

1. Creation of bumps on the pads of Sensor and ASIC with ENIG plating
2. Flip-chip assembly with an anisotropic conductive layer between the chips

Advantages: In-house, maskless, adaptable to the application, scalable, cost-efficient

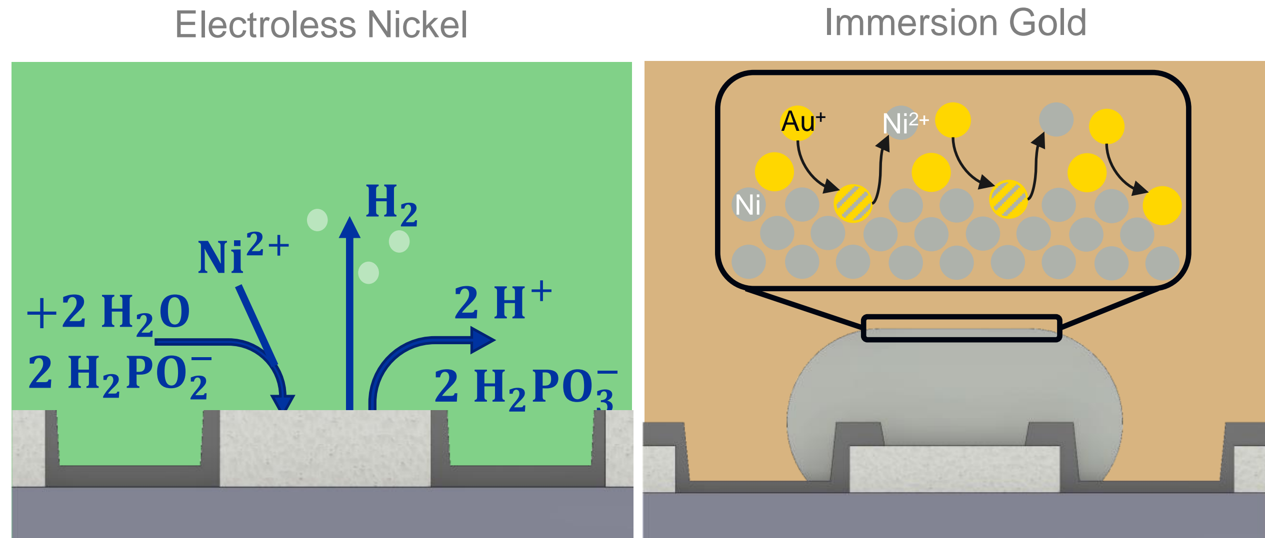
- **ENIG:** Electroless Nickel Immersion Gold
- **ACF: A**nisotropic **C**onductive **F**ilm
- **ACP: A**nisotropic **C**onductive **P**aste
- **NCP**: **N**on **C**onductive **P**aste

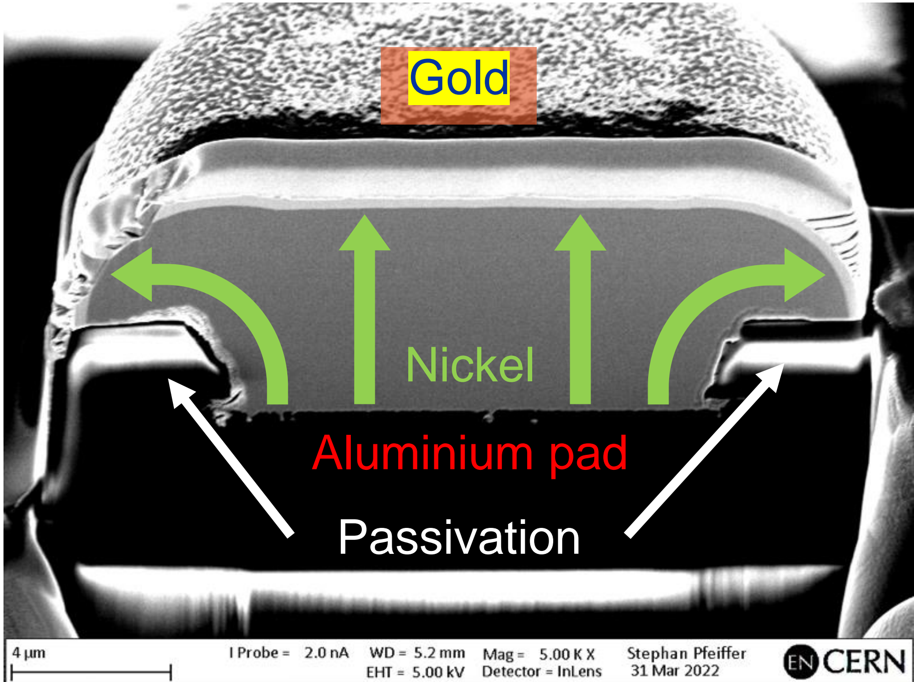


Introduction

3 main steps for ENIG plating:

1. Pre-treatment and zincation of the aluminium pad
2. Electroless Nickel deposition (creation of the bump)
   - Self-catalytic reaction on pad surface
3. Immersion Gold
   - Corrosion protection, bondable surface, very thin layer (< 1 μm)





FIB cross-section of an ENIG bump on an aluminium pad

Introduction

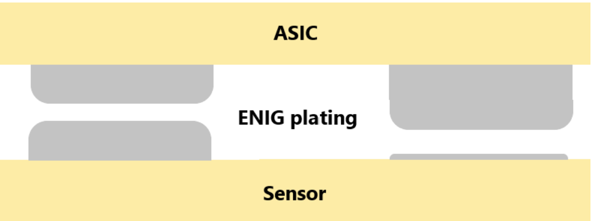
Challenges :

- Improve the uniformity of nickel bump height across the chips (especially at the edge of the chip)
- Avoid pad skipping and area skipping phenomena (non-plated pads and areas on a chip)
- Avoid over-plating phenomenon (plating on areas that should not be plated)
- Enhance deposition reproducibility from one chip to another
- Achieve ENIG plating on high connection density chips (ex: CLICpix2, 12µm pads; 25µm pitch)

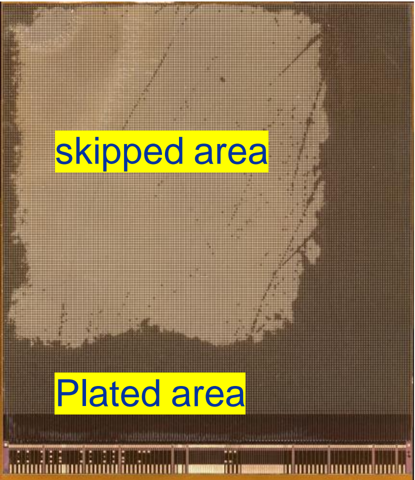
Improvements :

- Setup and process
  - For pre-treatment and zincation
  - For nickel deposition
- Characterisations
- Project management methods (systematic studies)

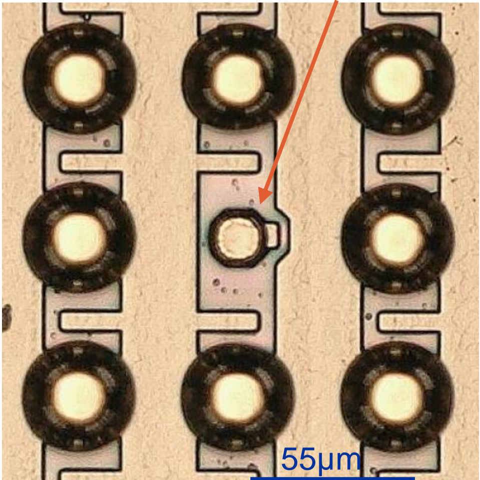
Illustration of non uniform plating



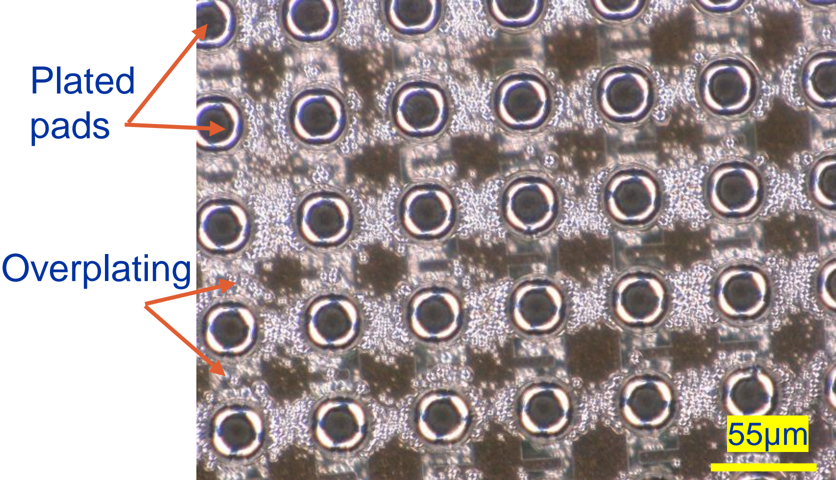
Plated chip with skipped area



Example of skipped pad

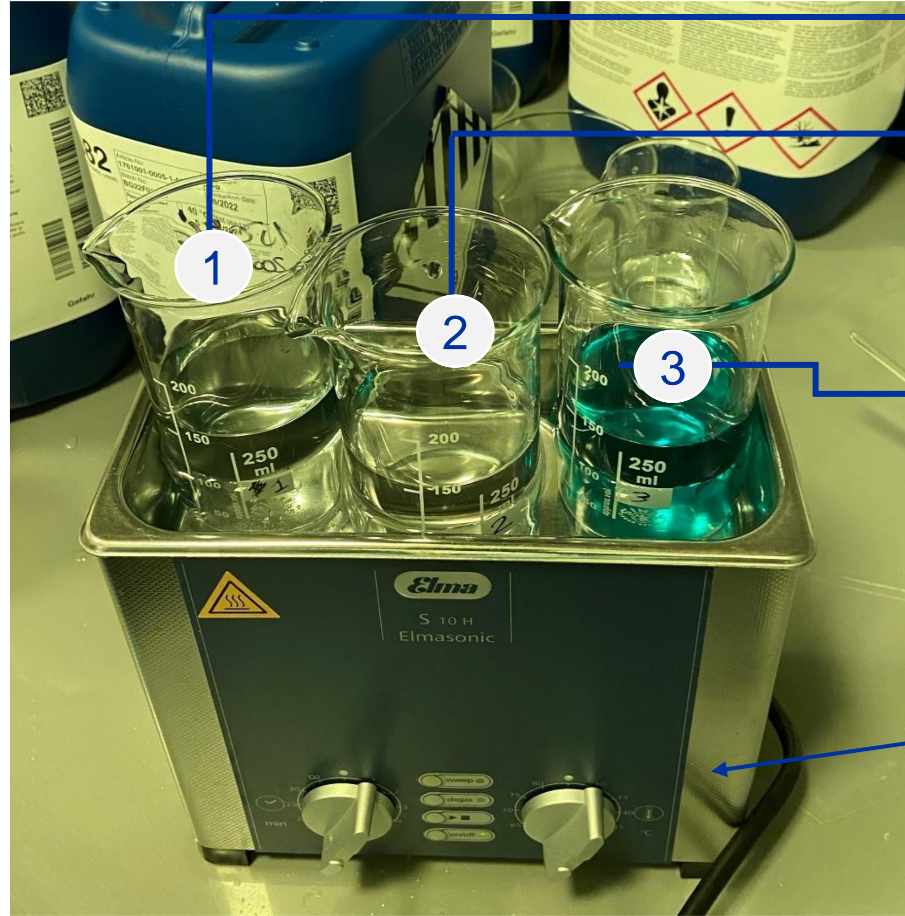


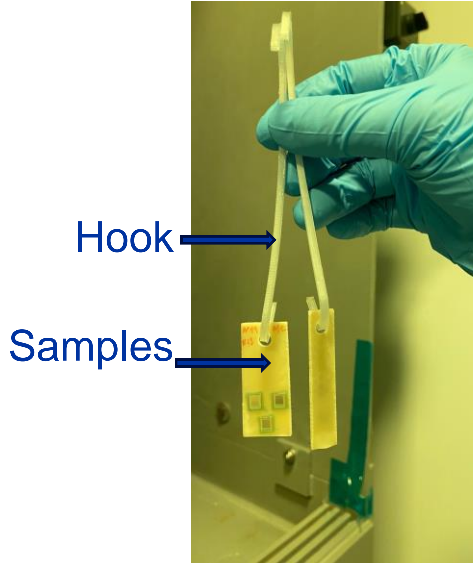
Example of overplating

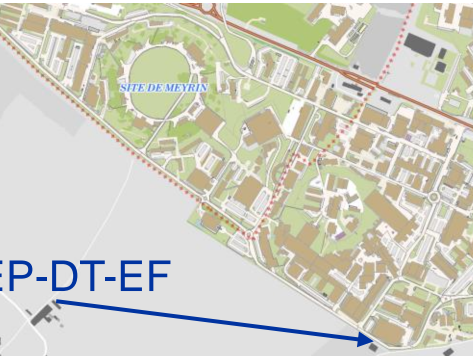


Setup and process improvements

Improvements for pre-treatment: ultrasounds + manual movements (previously static)







Setup and process improvements

Setup for nickel deposition

Hook

Sample

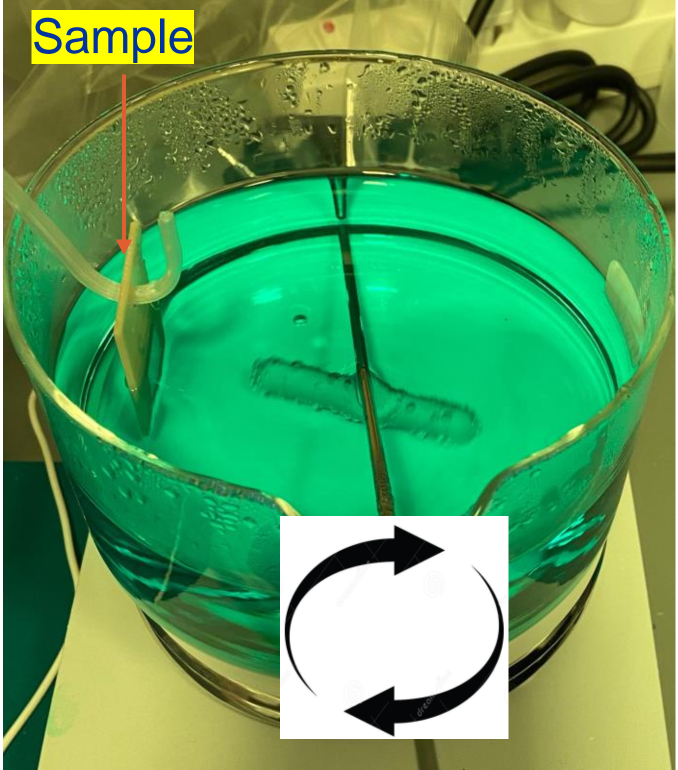
Stirring magnet

Hot plate

Temperature probe

Setup and process improvements

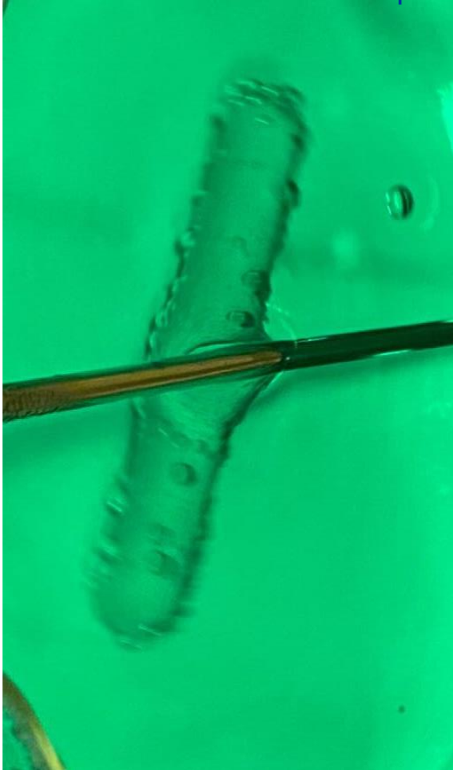
Stirring optimisation



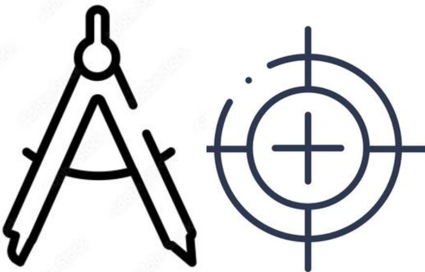
Swing movements

Bubbles removal

From the surface of the chip



Frequent calibration



- pH metre
- Temperature probe
- Micropipette

Avoiding cross-contaminations

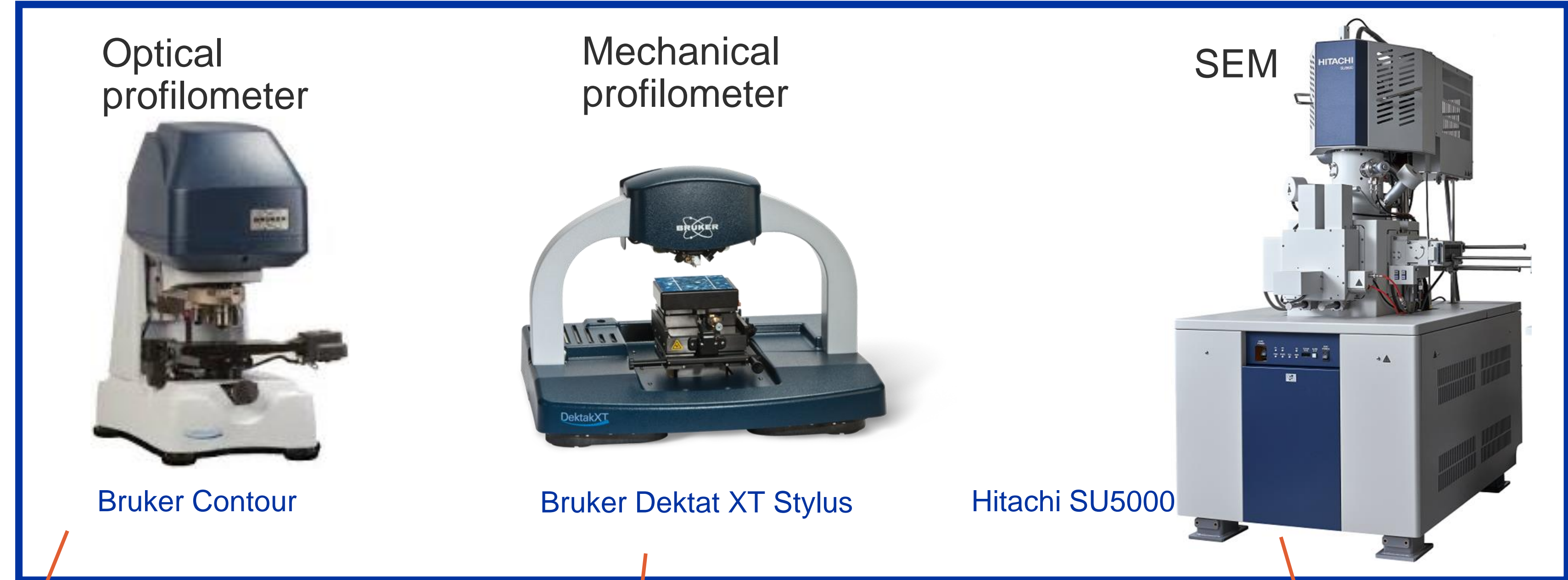
Thorough cleaning and use the same beaker for the same solution…

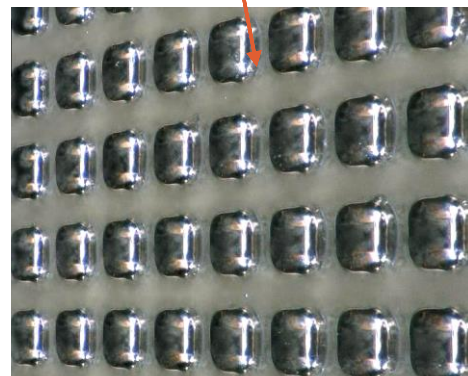
Nickel deposition

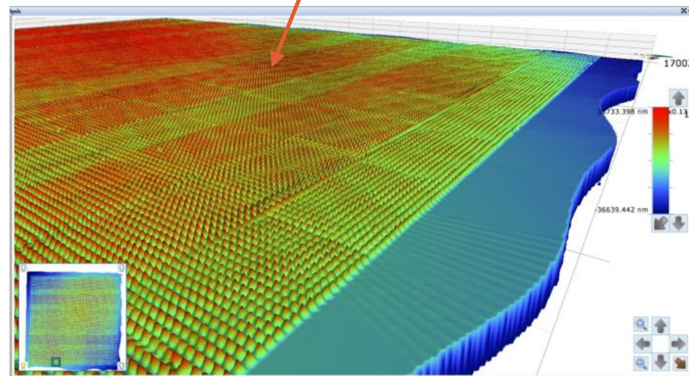
Characterisation improvements

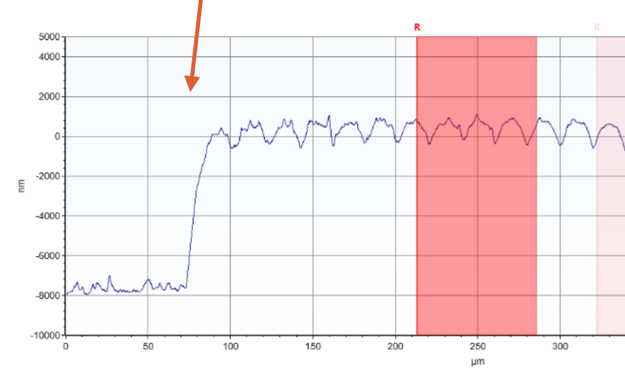
Keyence optical microscope
(CERN EP-ESE, B14)

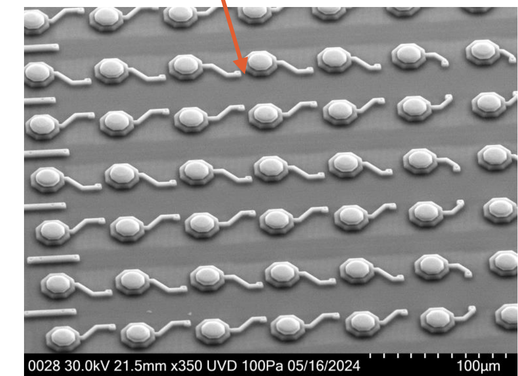
NEW (at Campus Biotech)





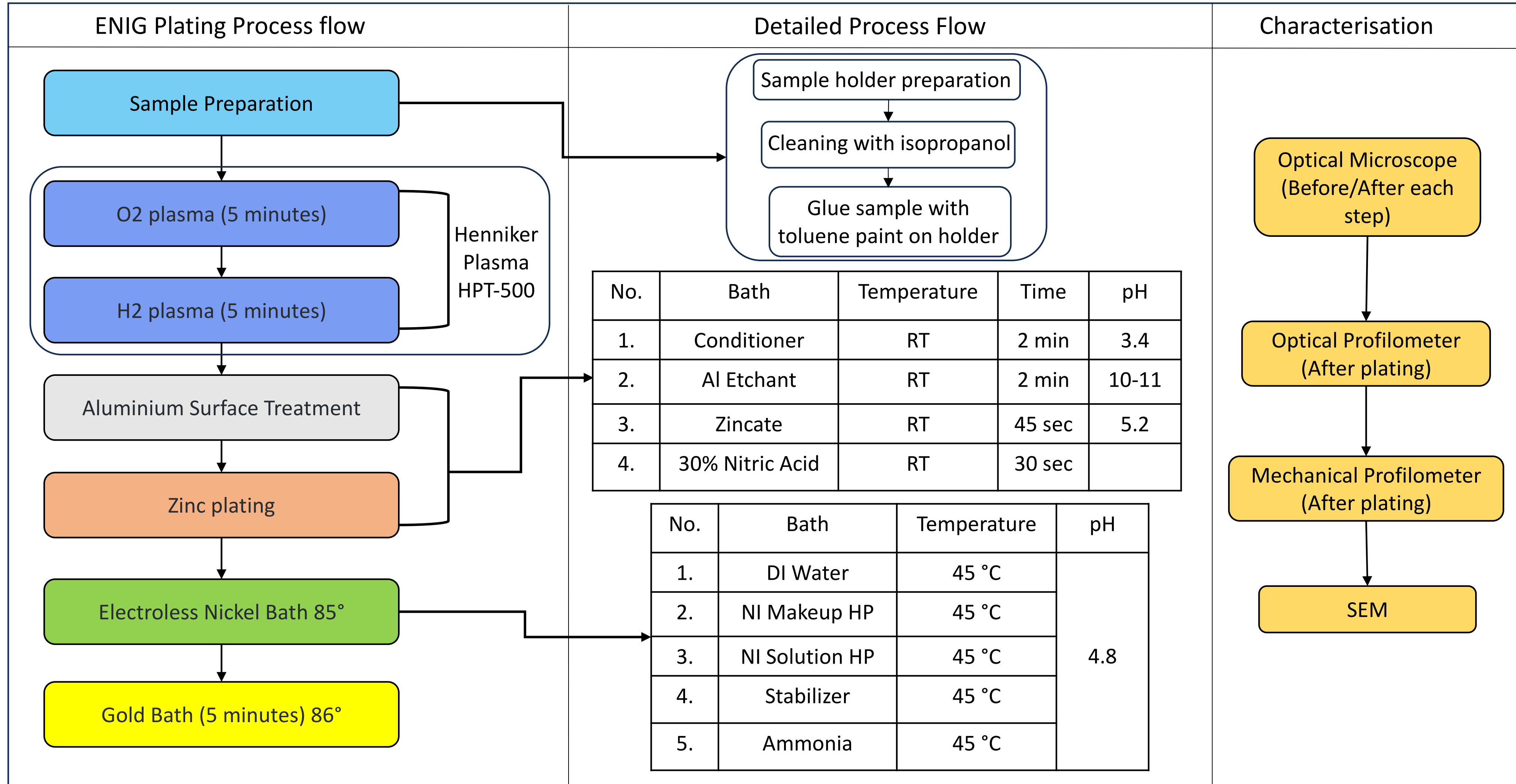






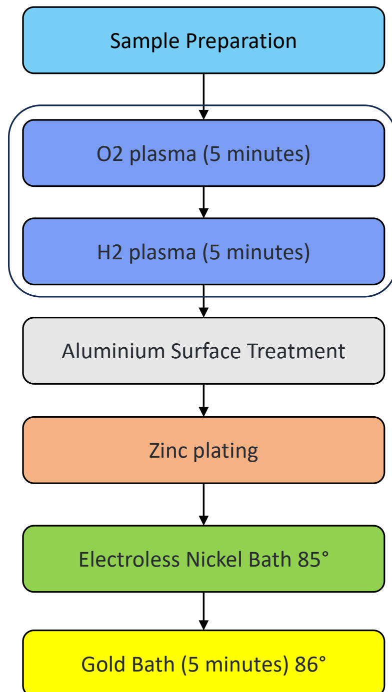
Process flow documentation

Systematic studies:
- Process flow
- Experimental design
- Detailed reports
- …



Experimental design development

Systematic studies:
- Process flow
- Experimental design
- Detailed reports…



3 months

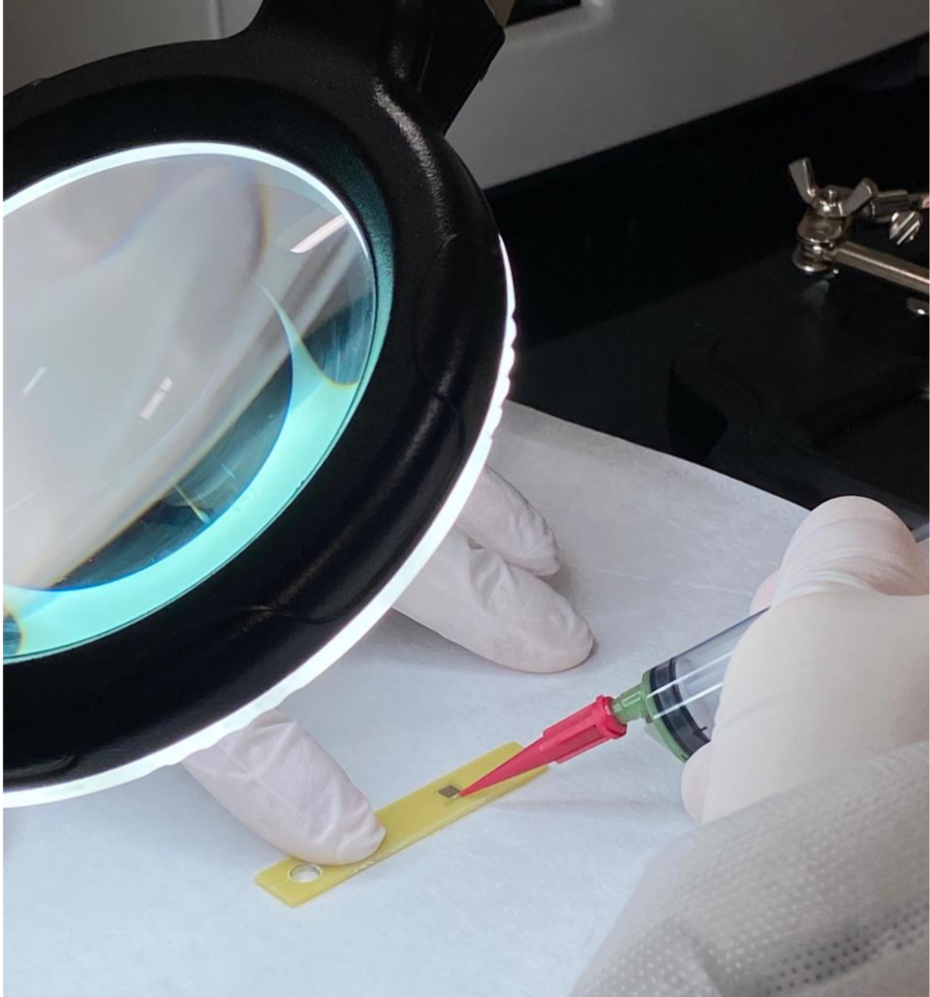
	ULTRASOUND FOR SURFACE TREATMENT	ULTRASOUND FOR ZINC PLATING	STIRRING FOR NICKEL PLATING	STABILISER CONCENTRATION	NICKEL BATH pH
Test 1	YES	YES	50	0.2 ml/l	4.8
Test 2	YES	NO	50	0.2 ml/l	4.8
Test 3	YES	YES	0	0.2 ml/l	4.8
Test 4	YES	NO	0	0.2 ml/l	4.8
Test 5	YES	YES	30	0.2 ml/l	4.8
Test 6	YES	NO	30	0.2 ml/l	4.8
Test 7	NO	NO	50	0.2 ml/l	4.8
Test 8	NO	NO	0	0.2 ml/l	4.8
Test 9	NO	NO	30	0.2 ml/l	4.8
•					
•					
•					

← Best results to date (Test 5)

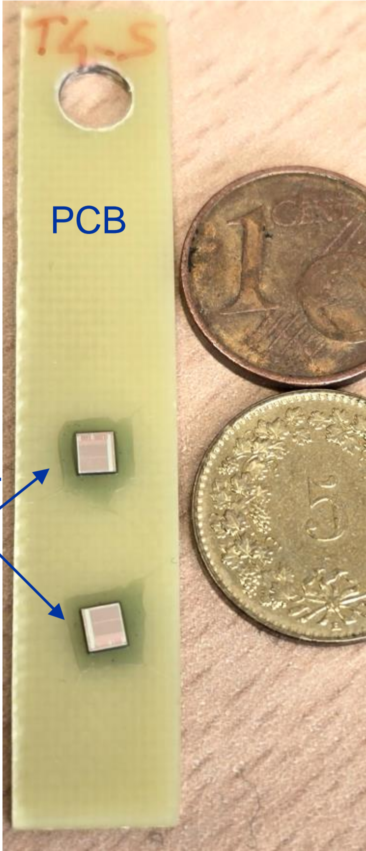
Samples preparation

Samples preparation steps:

- Cut PCB (FR4) pieces
- Drill PCB
- Clean PCB
- Glue the Chip on the PCB



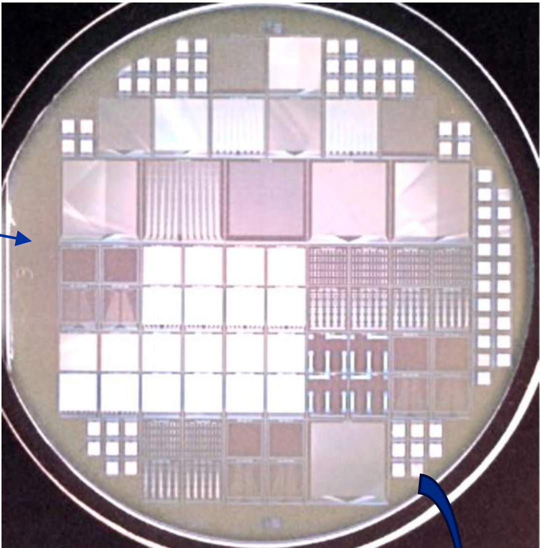
At DSF, B186

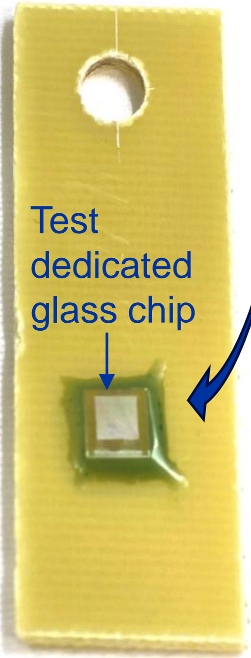


PCB

TIMESPOT chips

Test dedicated glass wafer





Test dedicated glass chip

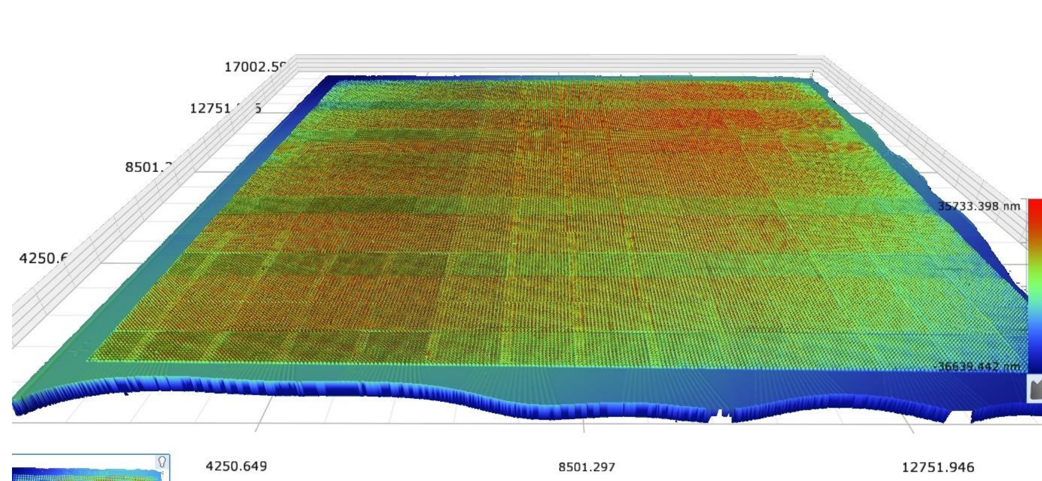
Results

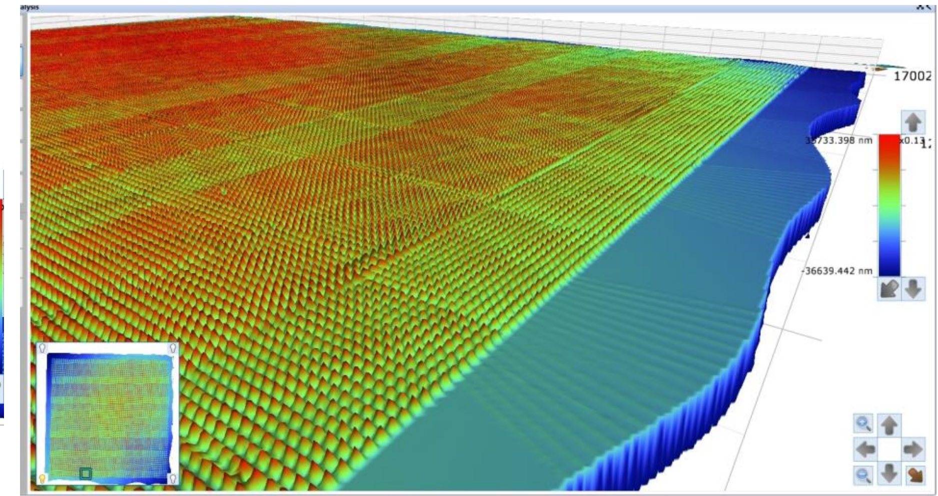
Timepix 3 test structures

Good ENIG results on 22µm pads and 55µm pitch:

- No overplating
- No skipped pad or area
- Good pad homogeneity
- 99% of pads correctly plated
- Pads height: 10 µm (+-0.5µm) 55min deposition

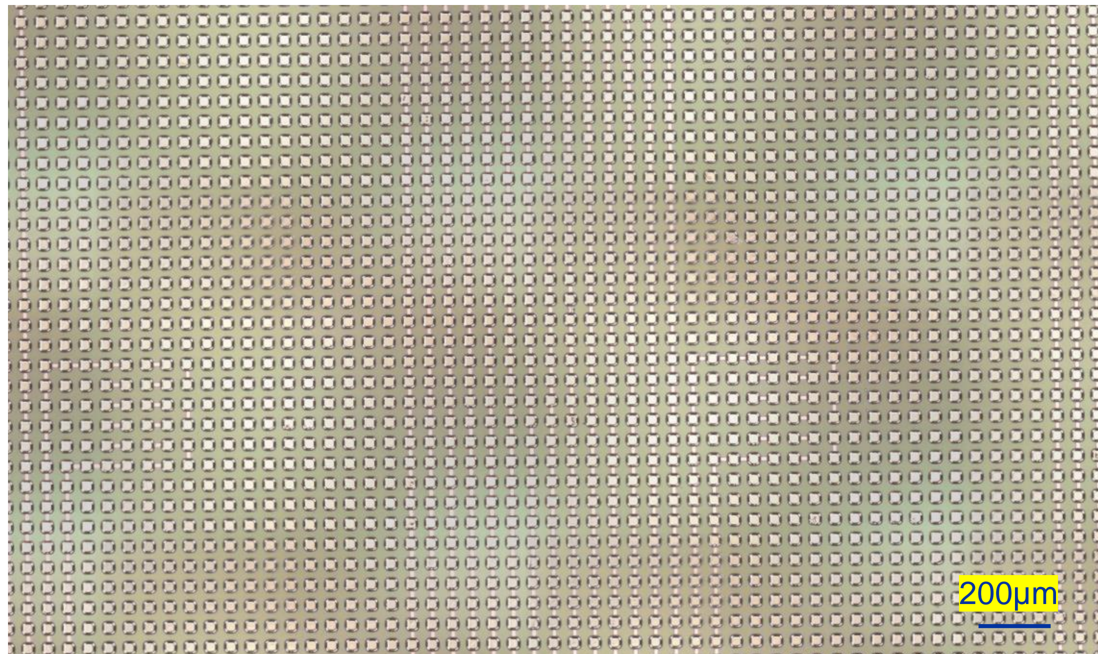
Optical profilometry after ENIG plating



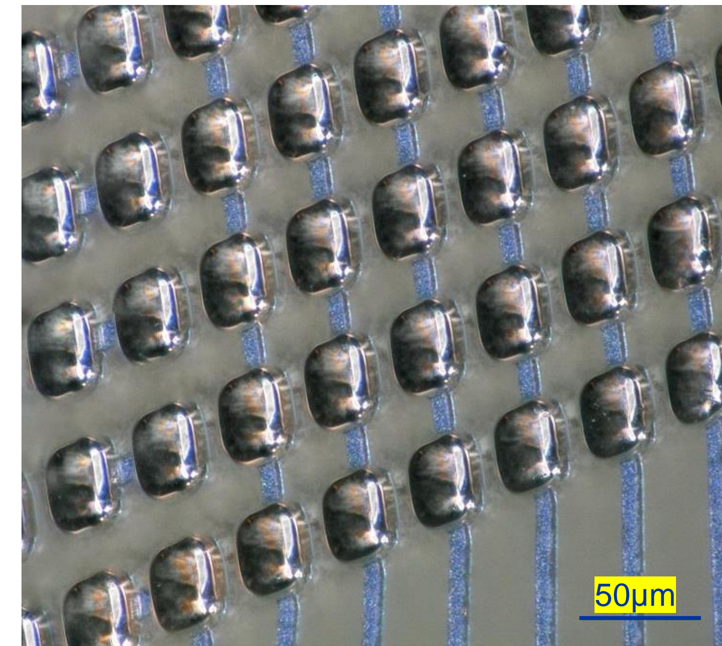


Timepix 3 test structure (14x14mm)

Optical microscopy after ENIG plating



Optical microscope, 45° tilt



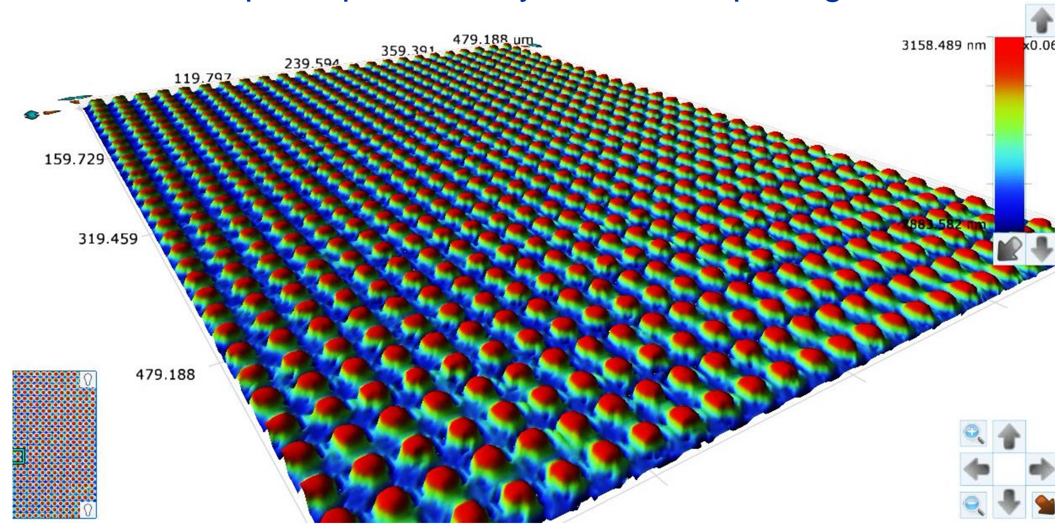
Results

"CLICpix2" test structures, 20µm pitch, 10x8µm rectangular pad size (High connection density)

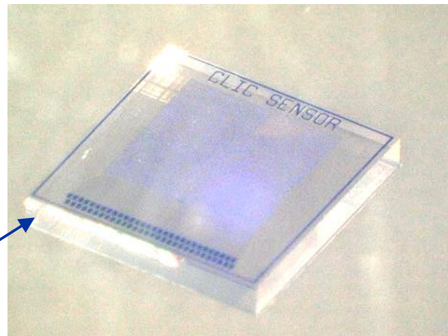
Excellent ENIG results:

- Good results, in line with our objectives
- >99% of pads correctly plated (16384 pads)
- Pads height: 4.5 µm (25min deposition)

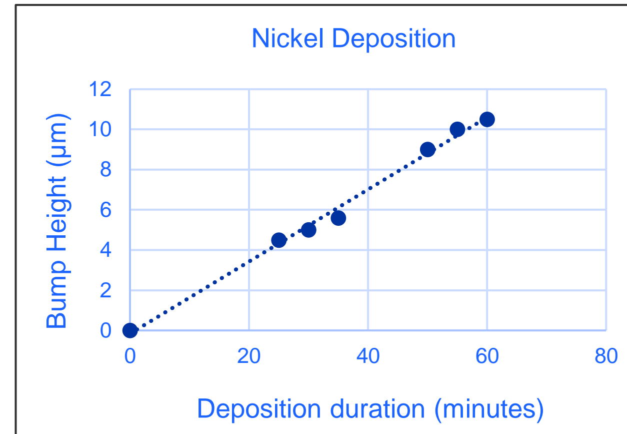
Optical profilometry after ENIG plating



Optical microscope, 45° tilt



CLICpix2 test structure (3.2x3.2mm)



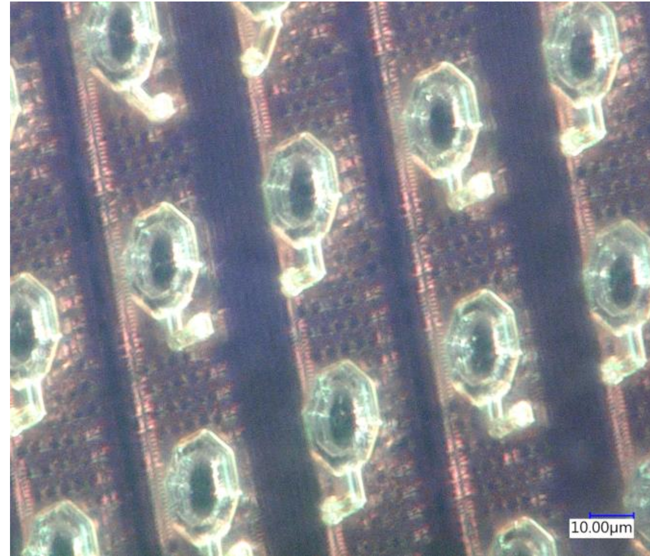
Results

TimeSpot ASIC
Functional chip
55µm pitch, 19µm pads

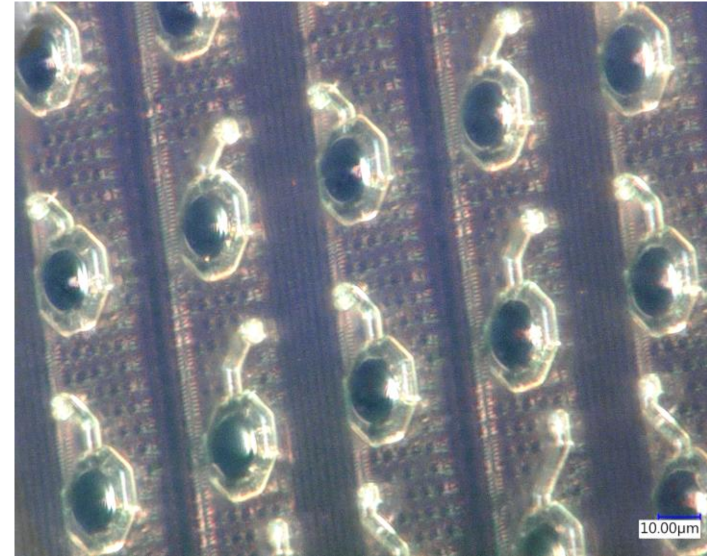
Excellent ENIG results:

- 99.93% of pads correctly plated (1184 pads, 1 not correct due to particle masking)
- Pads height: 10 µm (1h deposition)

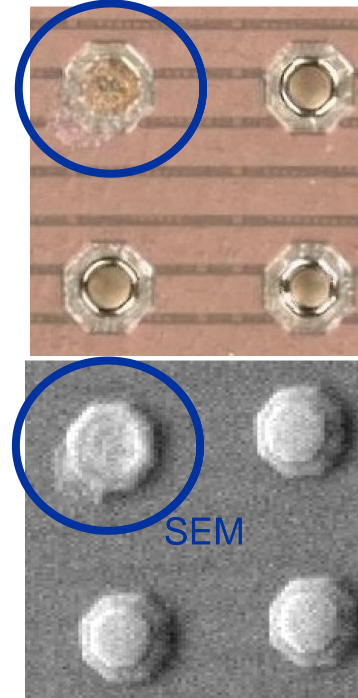
Before plating, optical microscope



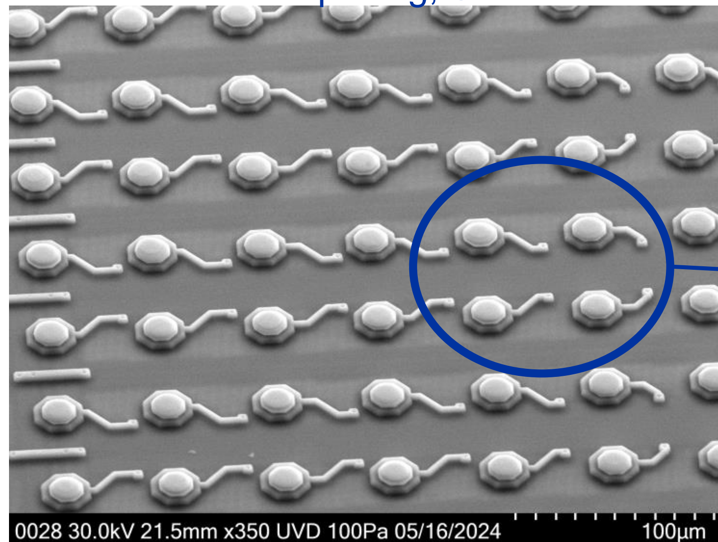
After 1h plating, optical microscope

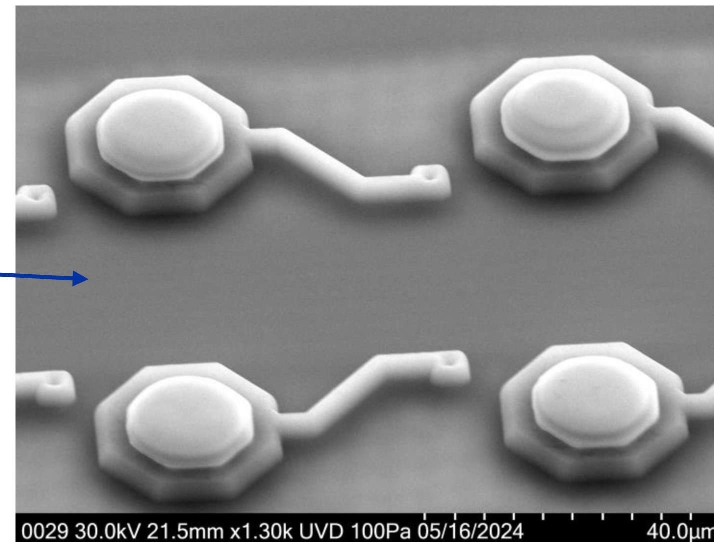


1 pad non plated due to particle



After plating, SEM





Conclusion for ENIG plating

- **Improvements of all the key points of ENIG plating:**
  - Reproducibility
  - Skipping (pads and areas)
  - Over-plating
  - Uniformity (even at the edge of the chips)

- **Adaptation of the ENIG process to high pad density (20µm pitch) and smaller pads (10µm)**

- **Successfull plating of TimeSpot ASIC**

Next steps:

- Confirmation of these results on high number of chips
- Study of the stability of the process over time (process drift)
- Apply this ENIG plating process to a large number of ASIC and sensors and adjust plating parameters for each application (TimeSpot, CLICpix2, Timepix3/4, ALTIROC…)
- Scalability of the process (single wafer processing)

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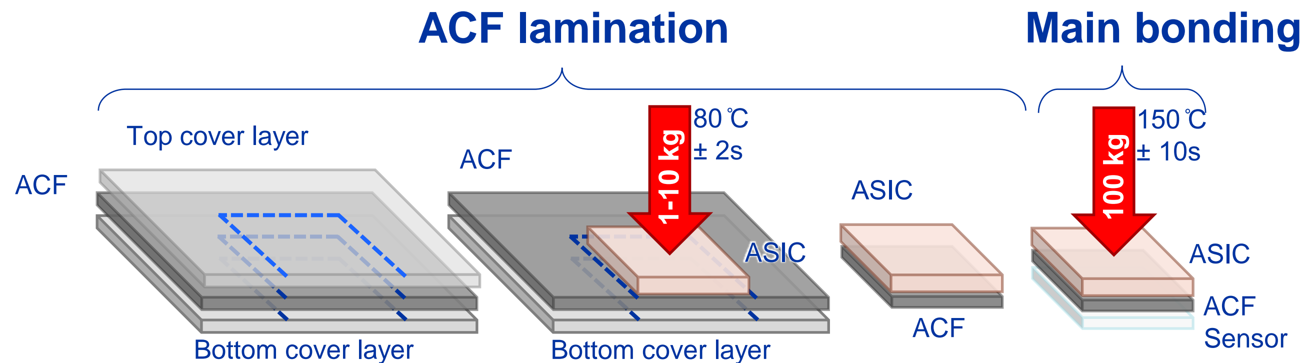
Anisotropic Conductive Adhesive (ACA) Bonding

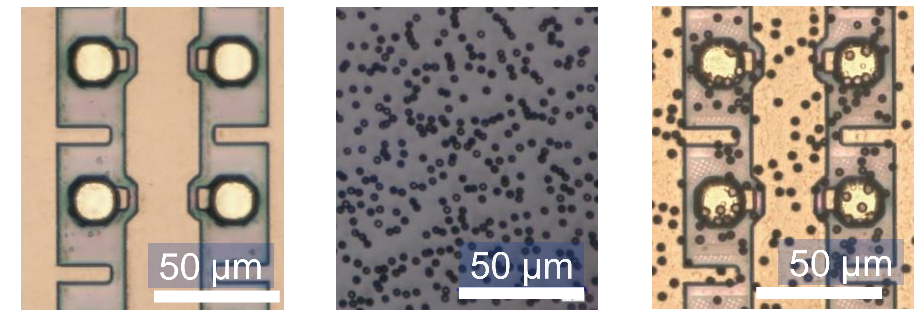
ACA technology investigated at Geneva University since 2017 using semi-automatic flip-chip bonder

- Precise temperature, pressure and alignment control
- Heating up to 400 ℃ and force applied by bonding arm up to 100 kgf
- Available for bonding with **a**nisotropic **c**onductive and **n**on-conductive **f**ilm/**p**aste – **ACF/ACP** or **NCF/NCP**

ACF bonding has two steps – lamination and bonding

- Pressure applied to displace and compress particles
- Epoxy cures at 150 ºC for a few seconds only



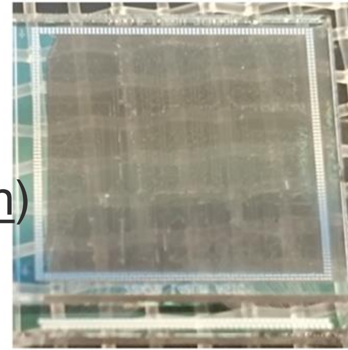


by Mateus Vicente

Dedicated daisy-chain studies

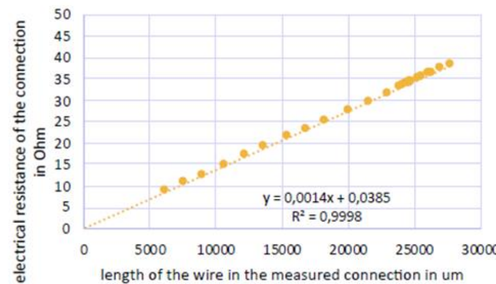
Different ACA type bonding

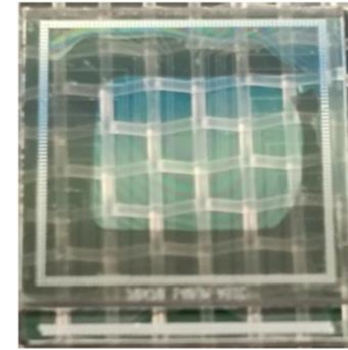
- Peripheral structure (2 rows, 140 µm pitch)
- Used two types of ACF and one ACP
- Consistent results, resistance less than 5 Ω per chain (8-9 connections)



3 µm particles

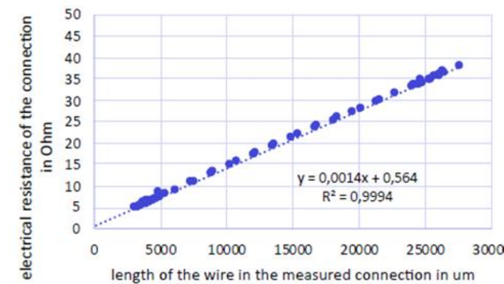
18 µm ACF – resistance measurement





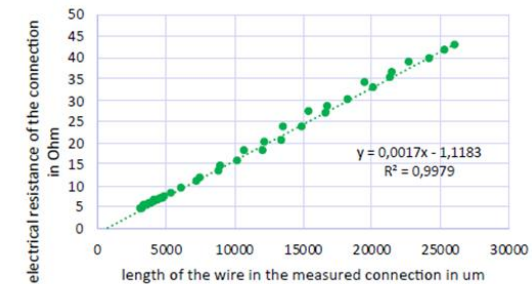
3 µm particles

14 µm ACF – resistance measurement



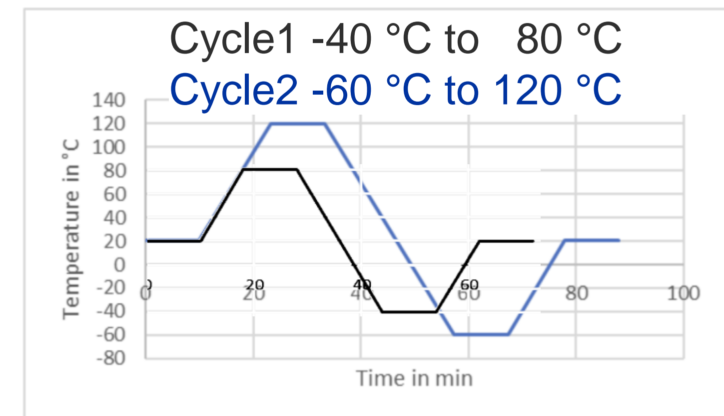
4 µm particles

ACP – resistance measurement



Degradation after thermal cycling

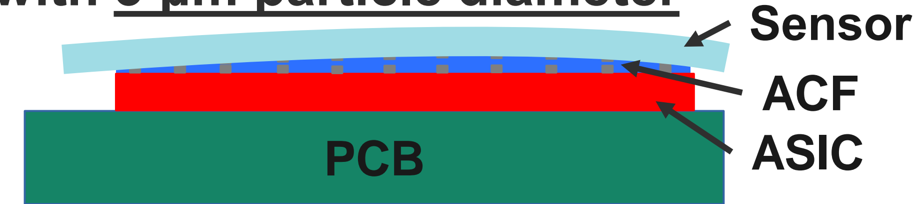
- 10x10 pixels with 1 mm pitch
- 20x thermal-cycled (3 different test suites x 2 plating types x 2 devices)
- *Only 9 of 100 connections tested on each device –> 108 tested total*
- 3 missing connections after bonding, 2 died in Cycle1 and 3 in Cycle2
- Resistance worsened by 0.2 Ω and 0.7 Ω after each set of cycles



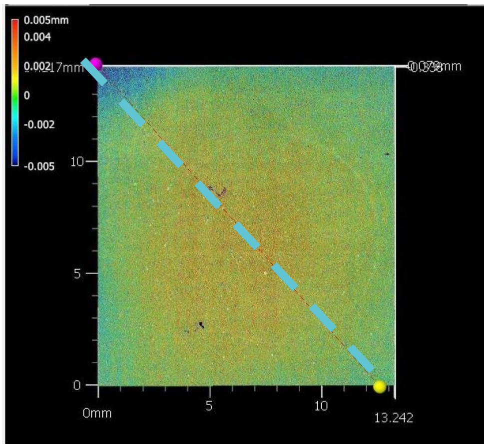
Timepix3 bonding evaluations

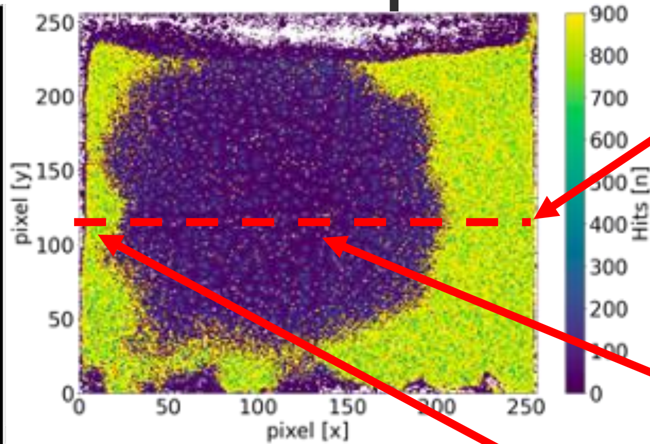
Evaluation of different ACF thickness (18 µm vs 14 µm), both with 3 µm particle diameter

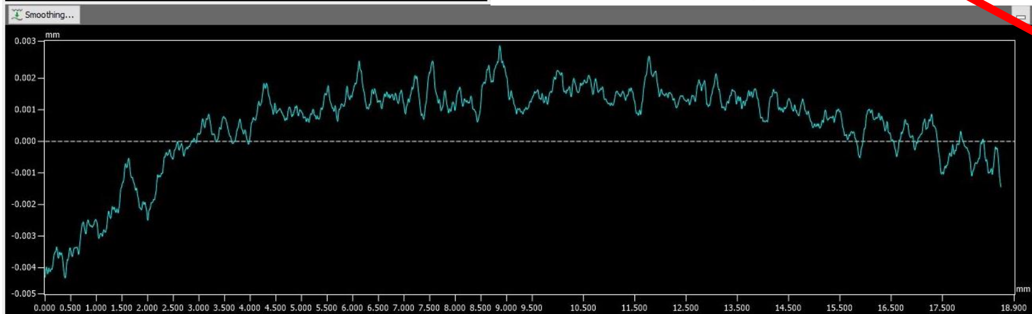
- Bent due to *insufficient bonding pressure* or *plating cavity volume*
- Plan to use higher force flip-chip machine in near future



ACF 18 µm







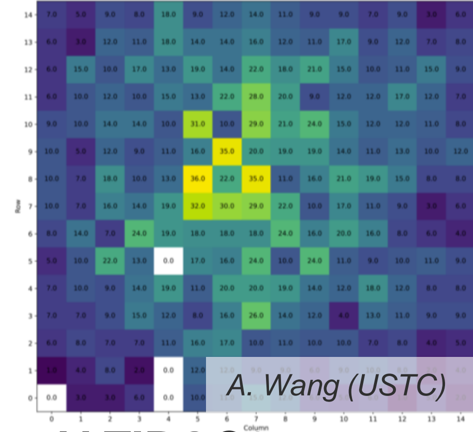
5.5 µm

Right	(1.54 ± 0.20) µm
Centre	(3.67 ± 0.19) µm
Left	(3.63 ± 0.10) µm

Other projects and applications

ALTIROC2/3

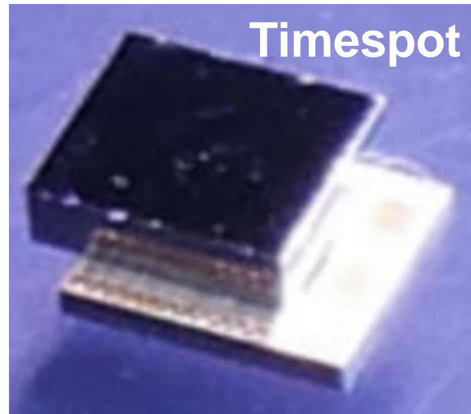
- 15x15 pixels, 1300 μm pitch
- LGAD sensor
  - ACP with 10 μm particles
  - **98.2% yield**
  - Successful lab and beam tests for ATLAS HGTD



ALTIROC2 response

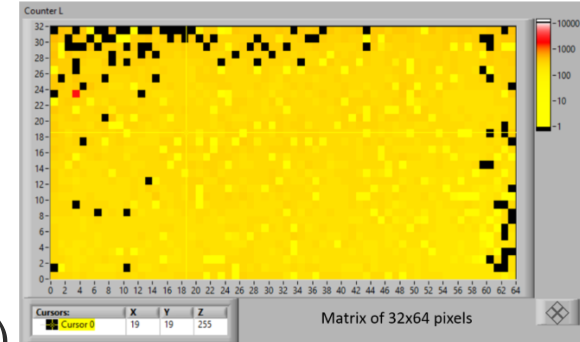
Timespot

- 32x32 pixels, 55 μm pitch
- Si 3D trench sensor
  - ACF 18 μm thick
  - **… to be tested …**
  - *Provided by A. Loi (INFN)*



SPHIRD

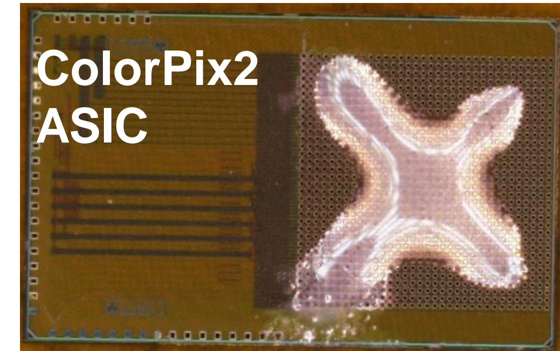
- 32x64 pixels, 50 μm pitch
- Si planar sensor
  - ACF 14 μm thick
  - **85% yield** (+7% weak response)
  - *Tested by M. Ruat (ESRF)*
- **CZT** sensor 2 mm thick
  - NCP
  - **… to be tested …**



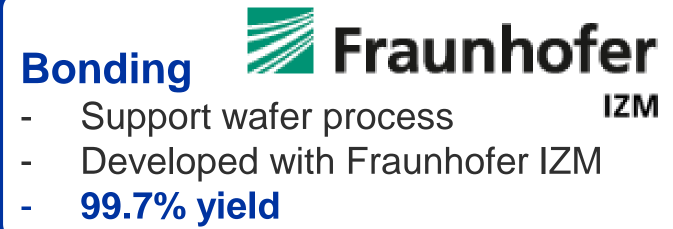
SPHIRD Si response

ColorPix2

- 32x32 pixels, 70 μm pitch
- **CZT** sensor 1.8 mm thick
  - NCP
  - **around 70% first yield** *(el. tests then failed)*
  - *Tested by J. Jirsa (FNSPE CTU)*

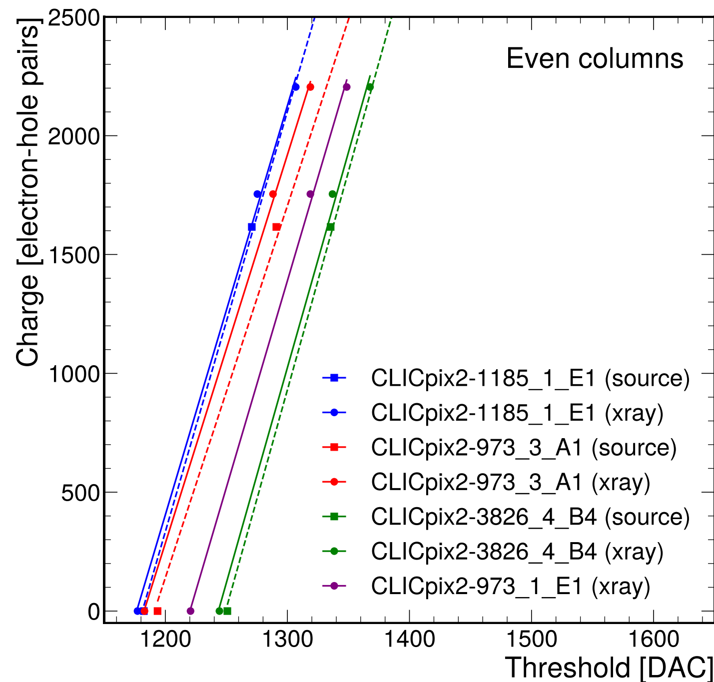


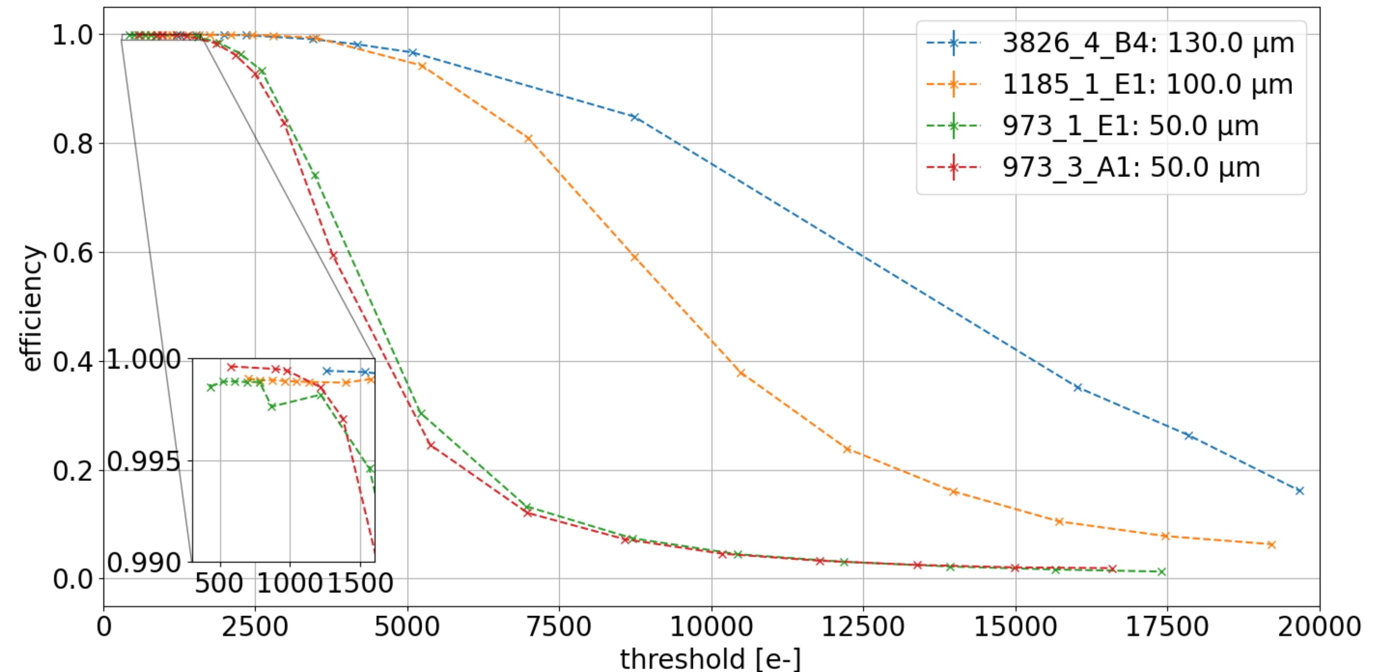
Single-die small pitch bump-bonding



Evaluation of single die bonded CLICpix2 assemblies (128x128 pixels with 25 µm pixel pitch)

- Performed calibration campaigns (lab sources and XRF) -> **1 DAC ~ 17.3 e⁻**
- Applied on previously taken pion beam data from CLICdp Timepix3 telescope at SPS North Area H6 line
- Shown full track detection efficiency up to 1500 e⁻ (even assemblies down to **50 µm** sensor thickness)





Outlook and plans

Optimisation of bonding parameters

- Bonding pressure, time, temperature
- Variation of adhesives (films/pastes; conductive/non-conductive; particle densities, …)

More stability testing of daisy-chain structures

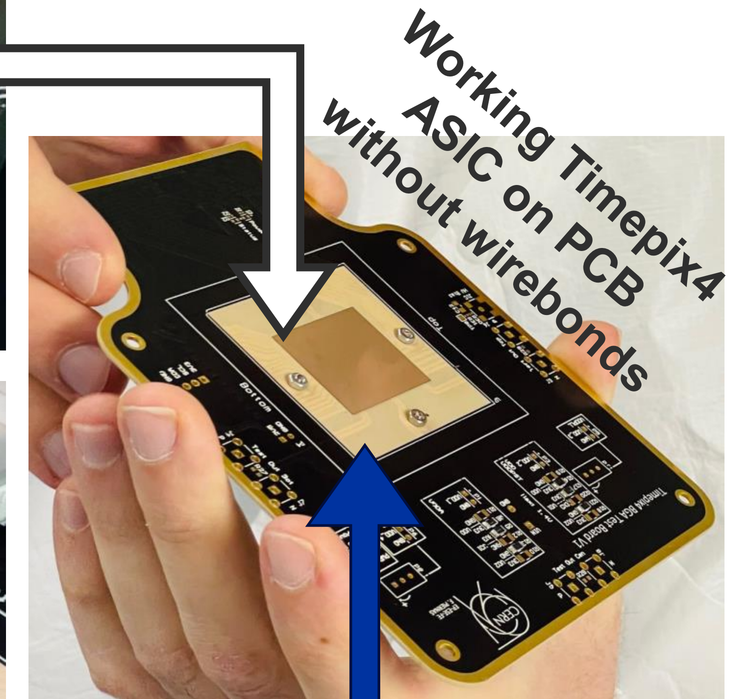
- Radiation hardness, electrical properties, mechanical strength, …

Already linked to multiple projects

- Expanding with testing of functional assemblies by us and partners

Need for an improved flip-chip machine

- Brings potential to reflow (such as Timepix4 Cu pillars) as well as higher force



TSVs with ACP now also investigated in WP5, see talk by Kostas and Davide

Introduction
D. Dannheim, P. Riedler

Plating
Ahmet Lale, Haripriya Bangaru

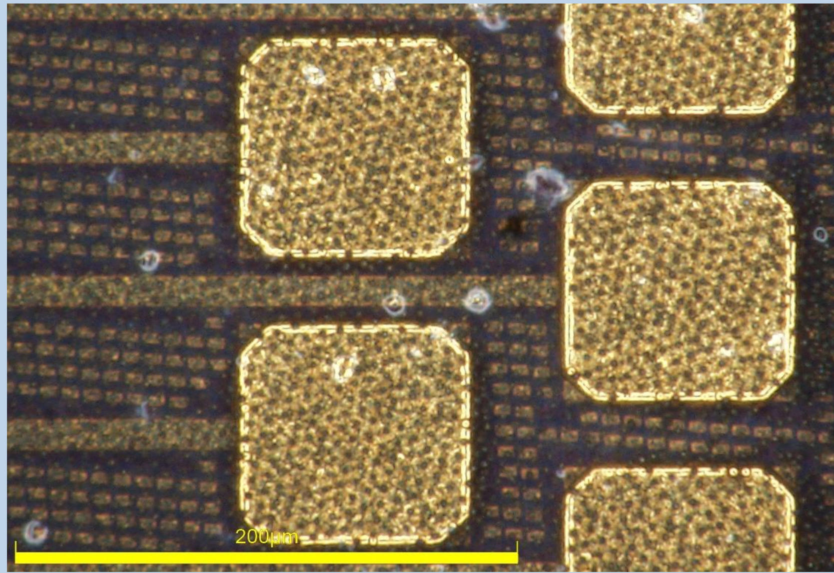
Hybridisation
Peter Švihra

Module interconnection, flex developments
Julian Weick, Abhishek Sharma

Plans and Conclusions
D. Dannheim, P. Riedler

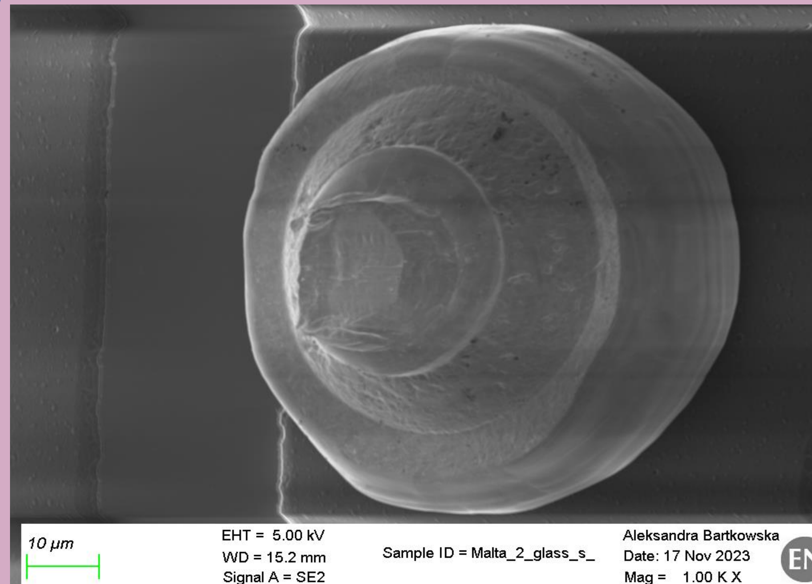
Interconnection technologies for modules

ACF



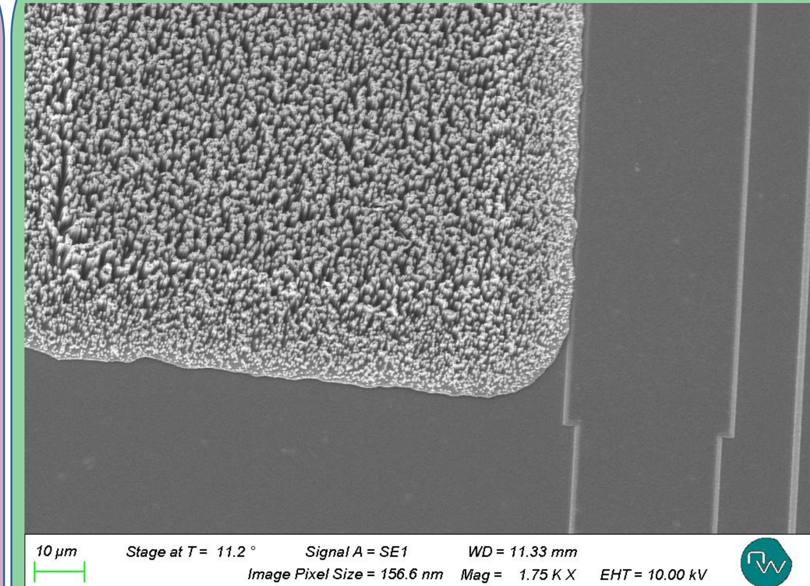
- **Cost effective**
- **In-house** processing
- **No mask** needed

Gold studs



- **Individual** pad selectable
- **Touch before** bond possible
- **No mask** needed

Nanowires (NW)

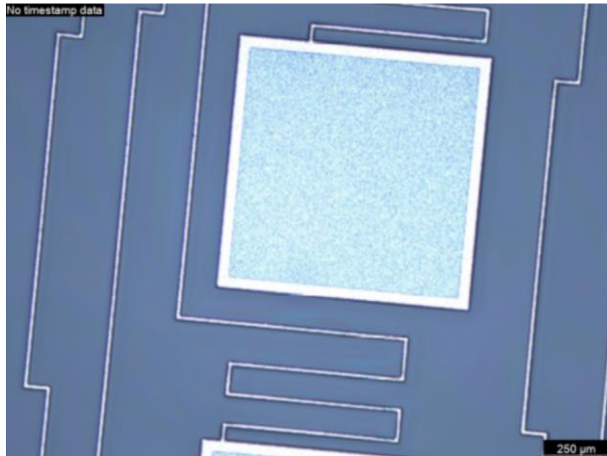


- **Low** resistance and parasitic
- **Glue-free** process available
- **Chip** and **wafer** level

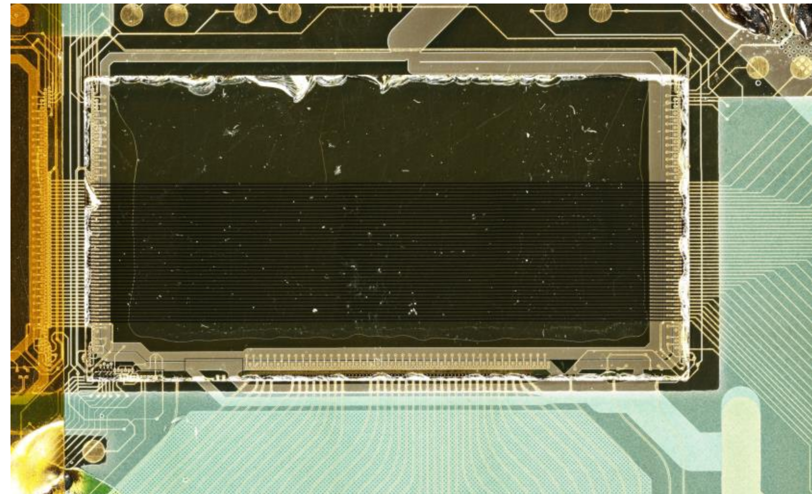
- **Scalable** on chip-chip or flex-chip
- **Glue support** for mechanical stability
- **Fast** interconnection
- Suitable for **large number of pads**

Test structures

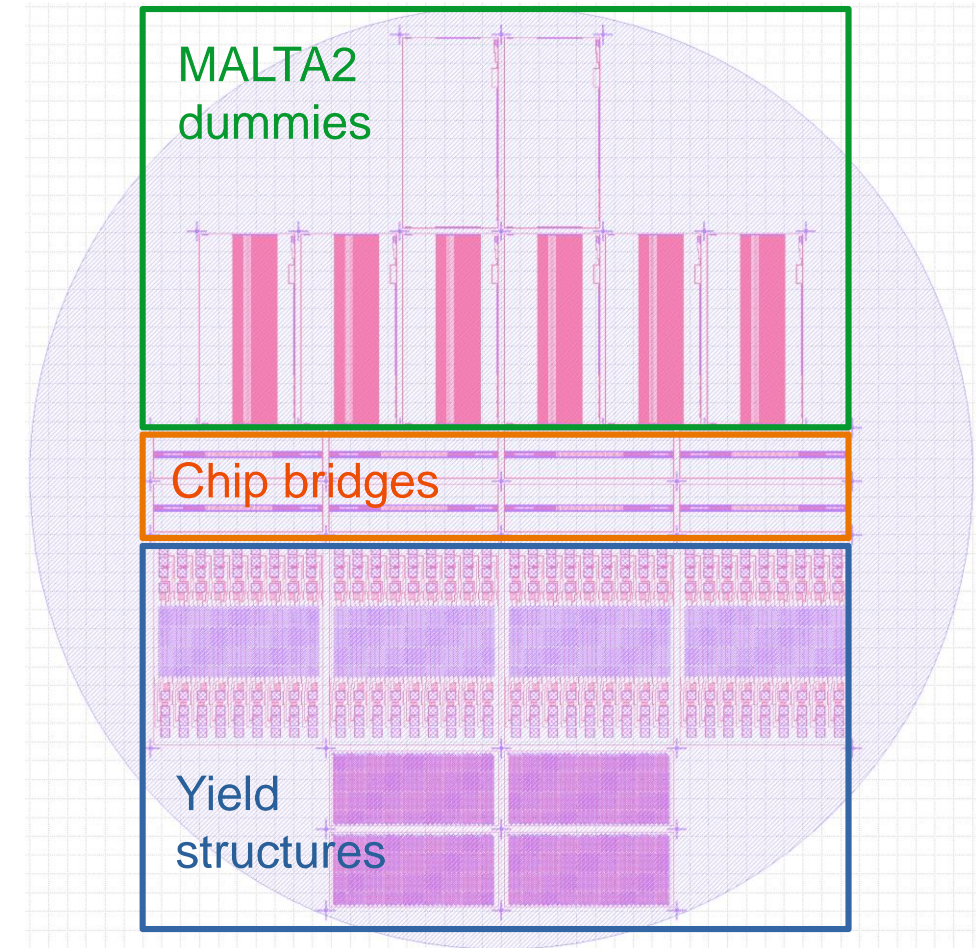
- Test structures have been produced by us at CMi in Lausanne
- 14 process steps
- Single layer Aluminium with SiO_2 passivation
- Evaluating connection yield, mechanical tests and bonding process optimization
- Produced 4 wafers with ~100 test structures



Test pad with SiO_2 opening



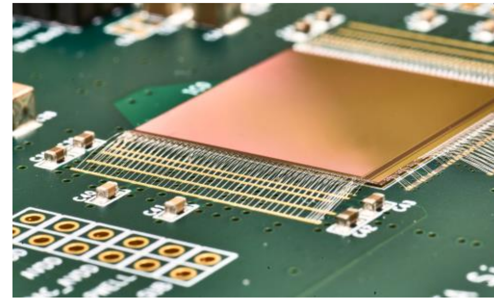
Bonded test structure on flex



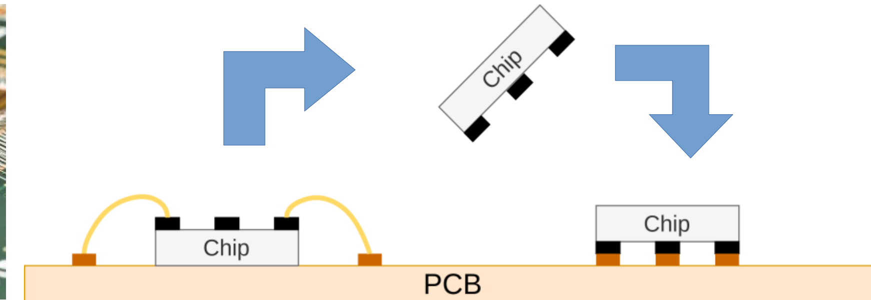
Ultra-thin module flex development

A flip chip mounted module provides:

- **No minimal spacing requirements between the chips**
- A **scalable interconnection**
- Interconnection is **not mechanically exposed**



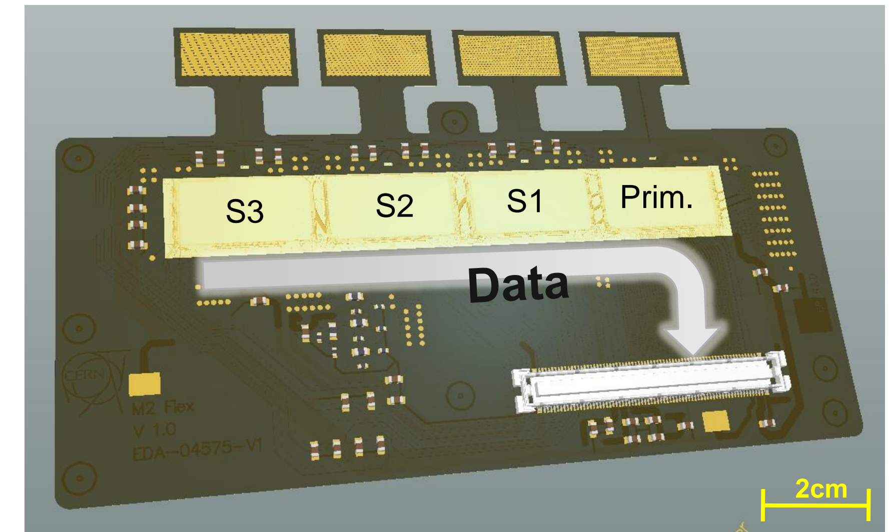
Wire bonding approach



Flip chip approach

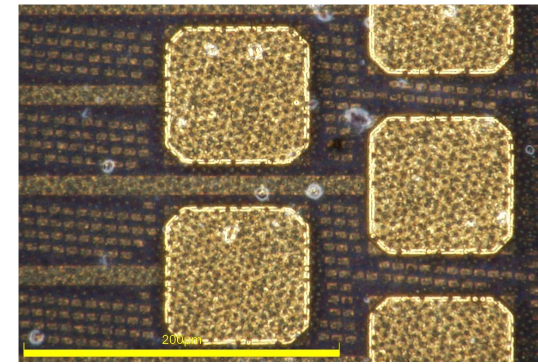
Designed dedicated flex PCB for a 4-chip module compatible with flip chip mounting.

- Design goals are **low-mass**, **large active area** module integration
- **Two-layer** layout ~30µm high with 17µm trace width and spacing

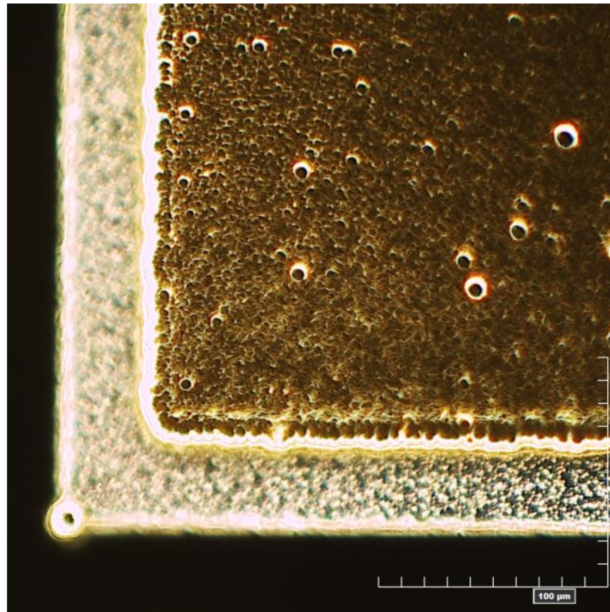


Data transfer from chip to chip

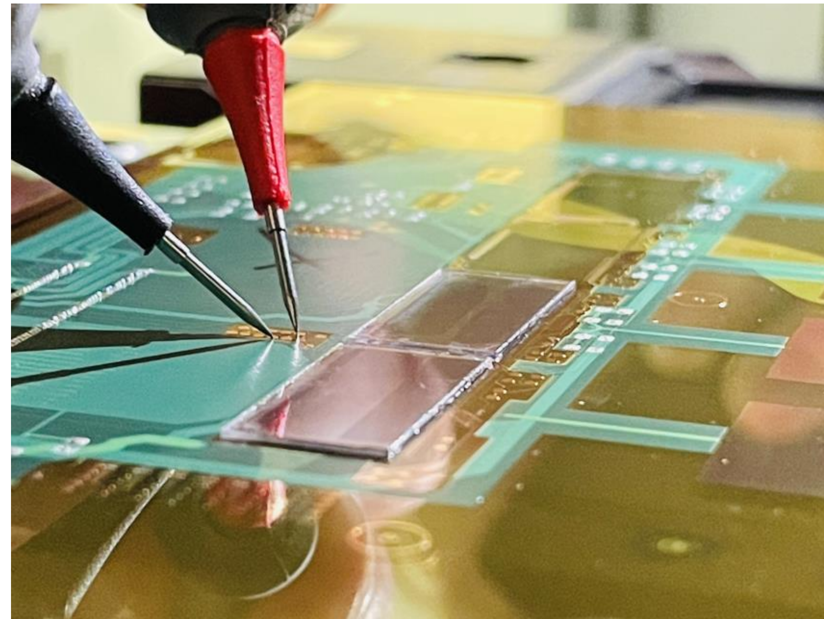
ACF bonding on flex



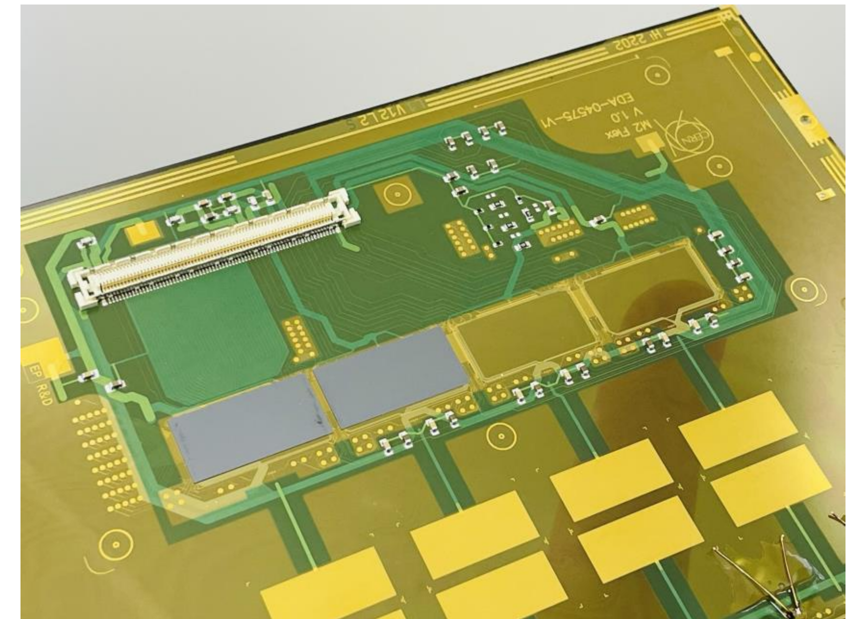
- Successfully bonded test structures and sensors using ACF
- Successful configuration of sensor and reference bit triggering
- In-house ENIG plating used as pad elevation for ACF process



In-house ENIG plating

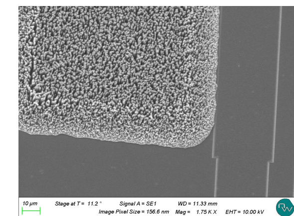


Electrical characterization of interconnection

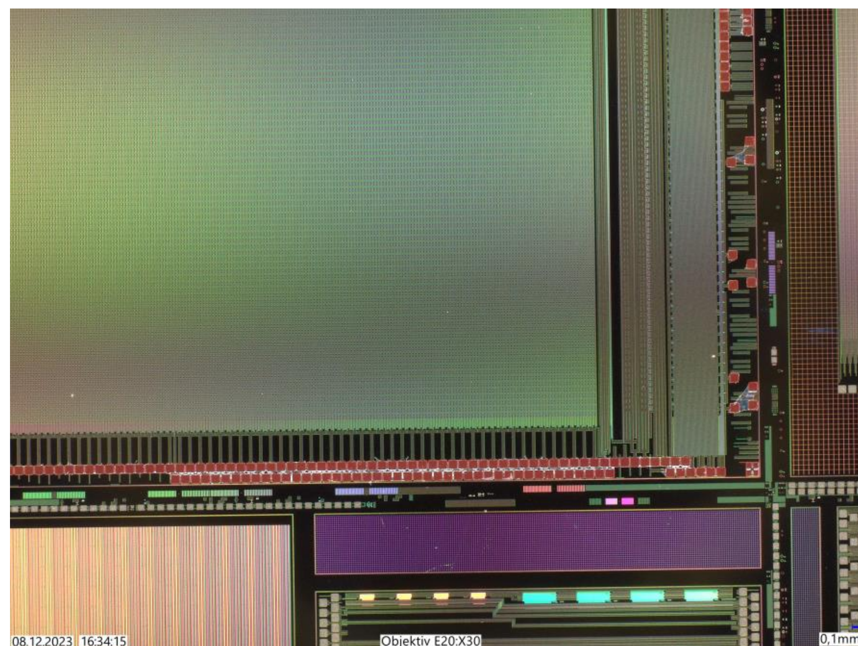


ACF-bonded chips on flex

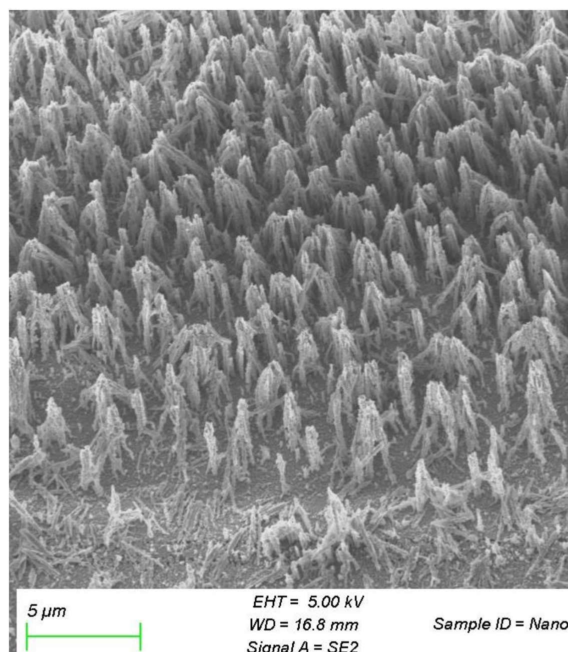
Nano-wires deposited on wafers



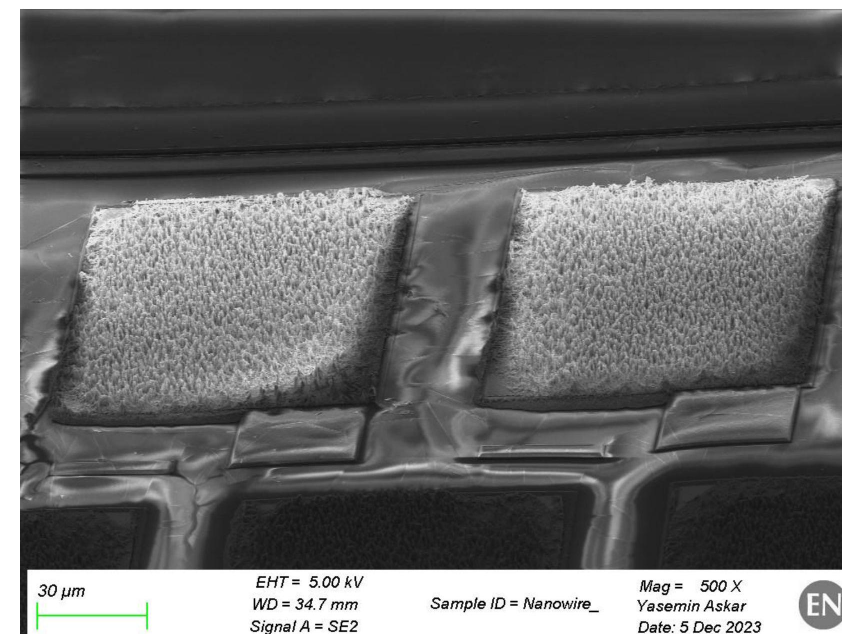
- MALTA2 **wafers** processed (88μm x 88μm aluminum pads with 32μm spacing)
- Currently **>90% pads** with perfect coverage, pads with **partial coverage that are still bond able** – no impact on MALTA2 performance
- Possible to **probe wired pads** with probe-card



Wafer scale wire deposition

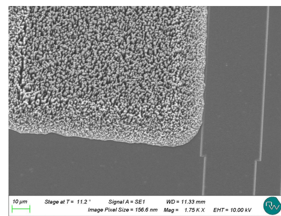


Close view



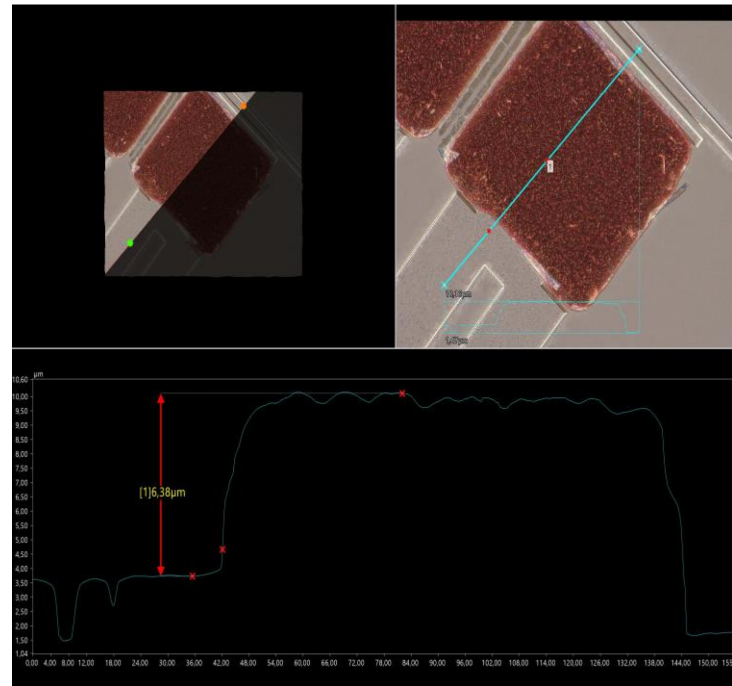
Nano-wires on chip pads

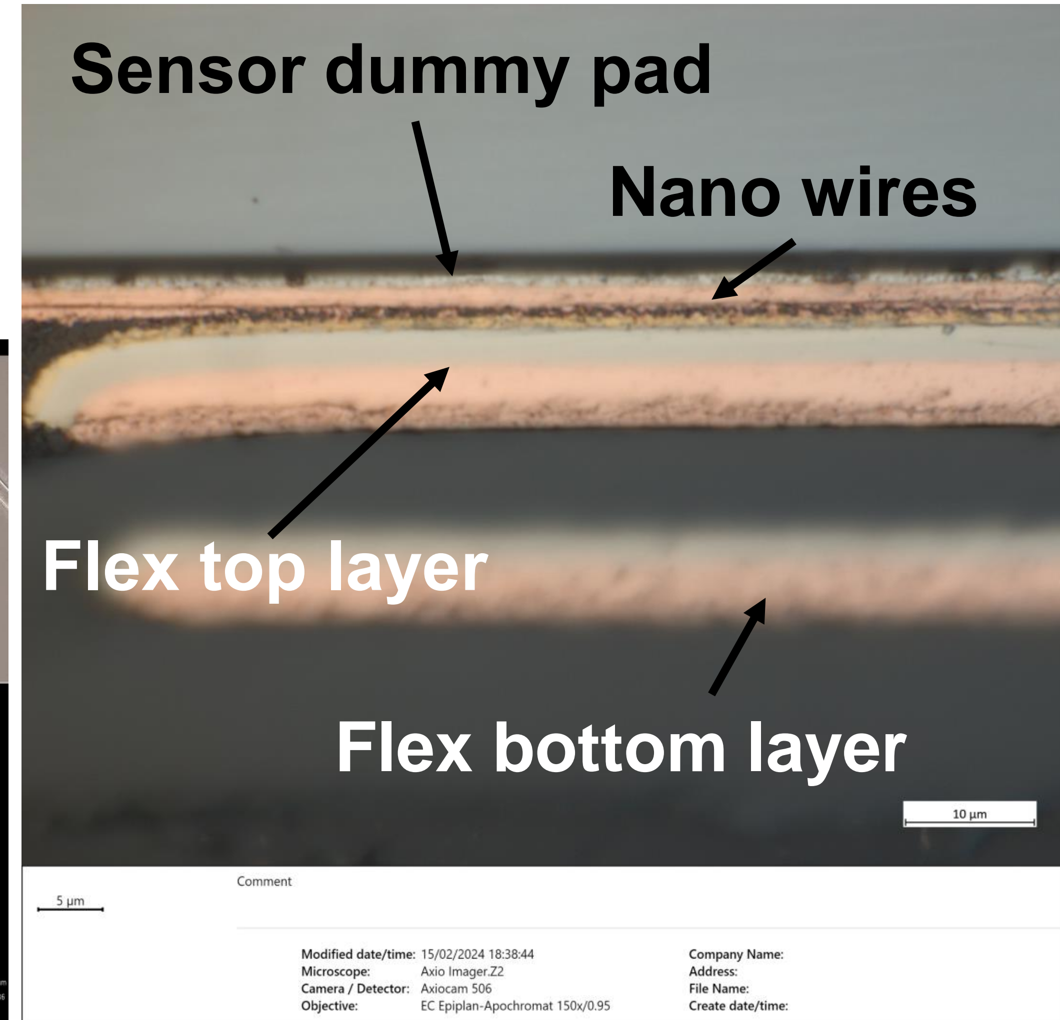
Nano-wire bonding of a chip on flex



- Successful **bonding** of nano-wired MALTA2 pads onto flex PCB pads using the **glue assisted process**
- Practically every **non-conductive glue** can be used for the bonding process

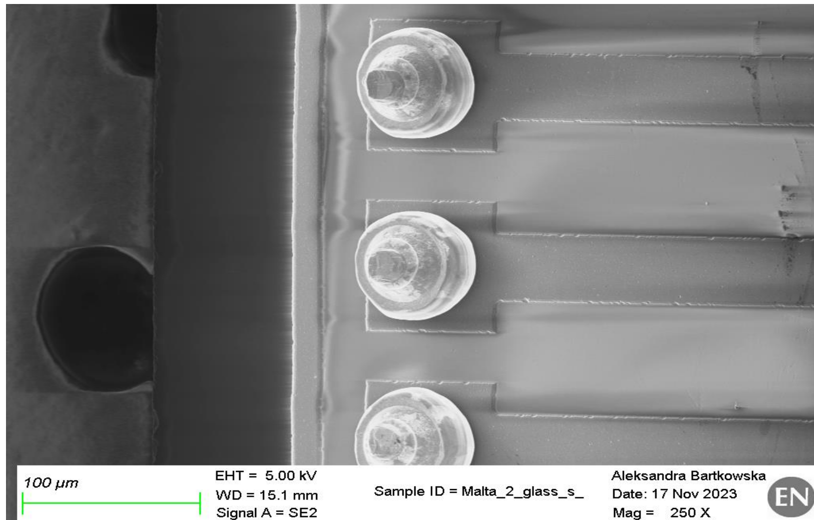
Different bonding options:
- **Sintering** (glue-free)
- **Cold welding** (glue-free)
- **Glue supported**





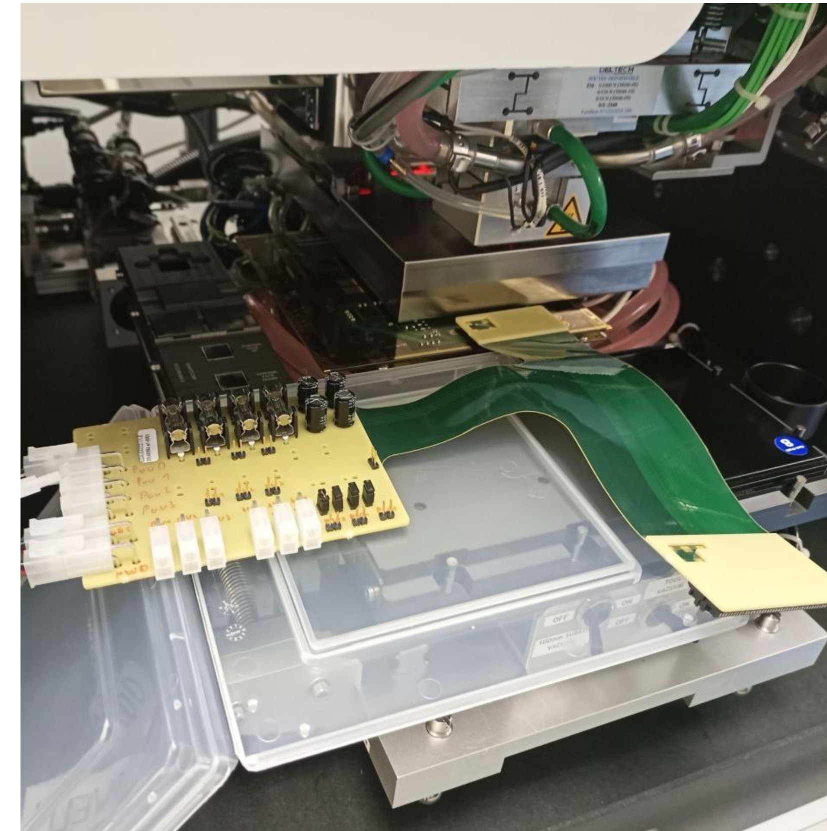
Gold studs

- **Individual pad** selection possible on application phase
- **Successful bonding** of test structures and MALTA2 sensors onto flex
- Verified **in situ pre-bonding verification**
- Bonded using **epoxy under-fill** Araldite 2011



Gold studs with flat head on test structure

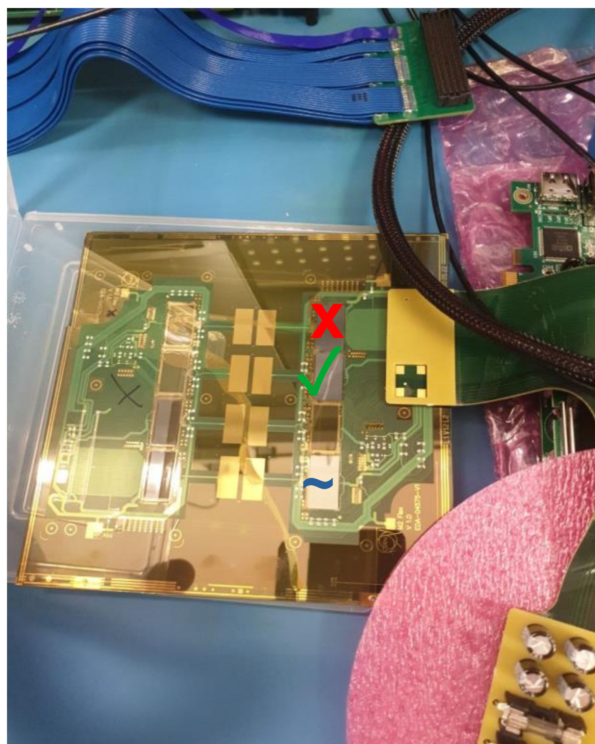
Test structure connected to flex using gold studs



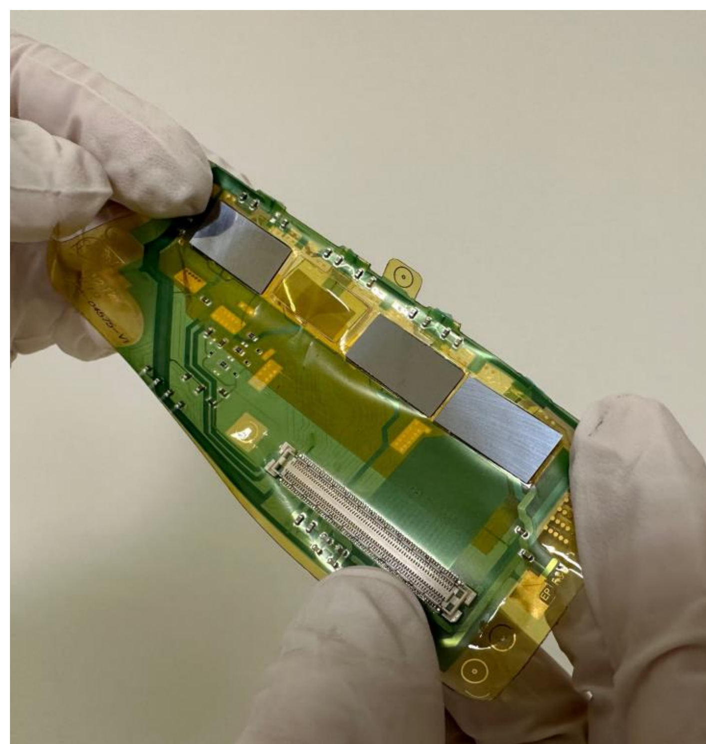
In situ pre-bond verification

Electrical testing and detached flex

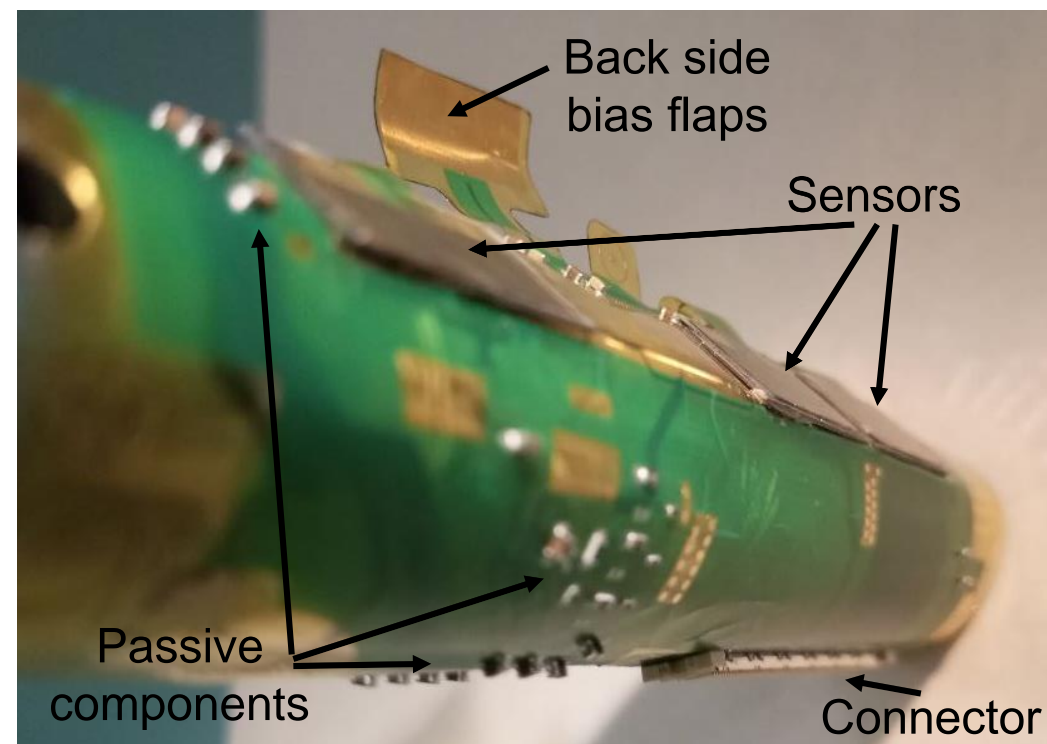
- Electrical tests verified the ability to **communicate** with the sensors
- Partial chip **read-out** conducted
- Peel of conducted **after flex assembly**



Electrical testing



Detached flex



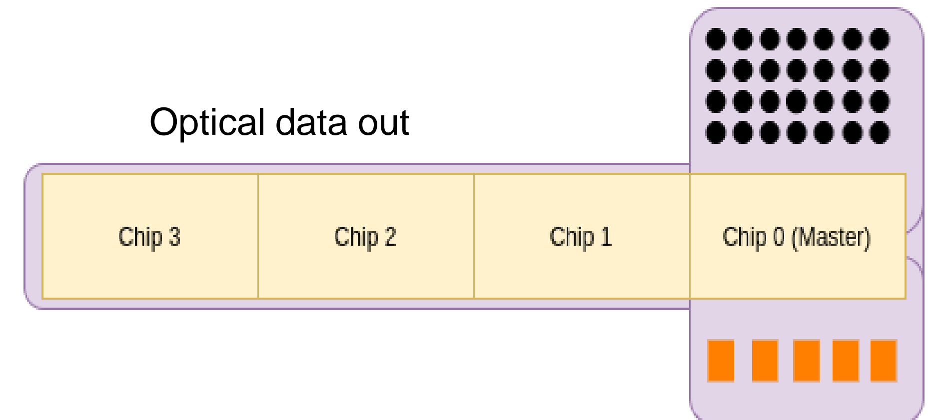
Detached flex

Future work

Next steps

- Build **demonstrator module** equipped for testing in lab and test beam
- **Interconnection toolbox** ready, next step is to develop more in **house process for manufacturing a flex**
- Enabling fast modularization with different chips, **hybrid and monolithic**.

Optical flex with WP6



Flex with integrated optical data link

Introduction
D. Dannheim, P. Riedler

Plating
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Hybridisation
Peter Švihra

Module interconnection, flex developments
Julian Weick, Abhishek Sharma

Plans and Conclusions
D. Dannheim, P. Riedler

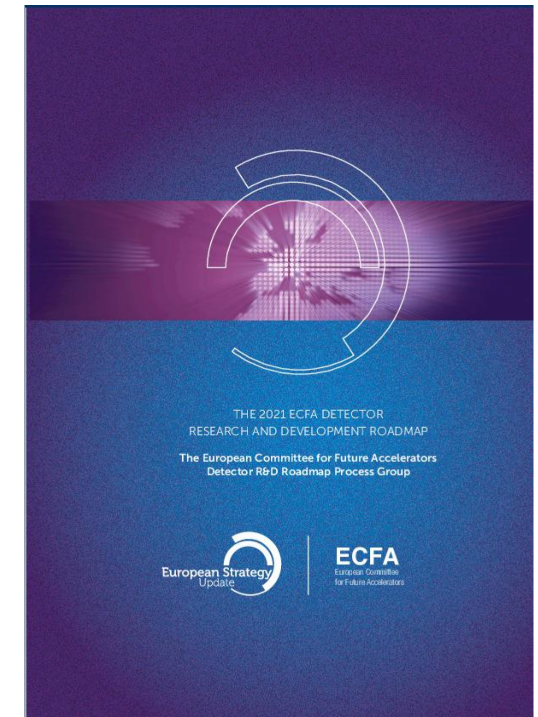
WP 1.3 in DRD3

- DRD3 collaboration on semiconductor detectors received preliminary approval from ECFA DRDC / Research Board
- Interconnect and modules activities are included in dedicated WG7 of DRD3
- Expressions of Interest for WG7 from 16 groups up to now: https://cernbox.cern.ch/s/QcJZDNdHNzctjNx

DRD3-WG7 expressions of interest (as of 21-May-2024):

Group	Topics of interest / ongoing work
ANL	Technologies for large-scale tracking devices
Bonn University	W2W bonding; fine-pitch (<50 um) bonding; in-house hybridisation
CERN	In-house plating and hybridisation; compact module studies with silicon photonics integration
FBK	3d-integration and interconnection of BSI-SiPMs for NUV/VUV; mask and mask-less UBM; W2W temporary bonding; chip-level solder-ball bonding >50 um; wafer-level micro bumps/pillars <50 um; in-house maskless interconnects
Geneva University	In-house flip-chip bonding: gold studs, ACP/ACF, Cu pillars; chip-to-flex
IMB-CNM-CSIC	RDL, TSV, interposers
INFN Bari	interconnection between bent sensors; stacking of several CMOS sensors for full 3d tracking
INFN Firenze	Novel interconnection techniques for future applications
INFN Milano	Indium bump bonding; in-house die-to-die and die-to-PCB bonding; hybridisation of RSD; multi-chip systems on PCB/bus tape
INFN Trieste	interconnects for bent and ultrathin chips (ALICE ITS3); aerosol jet printing for RDL and contactless interconnects; TSV and wafer-to-wafer for 3D stacking
IPHC Strasbourg	SOI
IP2I Lyon	wafer-to-wafer interconnect demonstrator
KIT Karlsruhe	in-house flip chip, gold studs, TSV processing, RDL
LPNHE Paris	interconnects: ACF, ACP, gold studs; characterisation techniques and devices; reliability testing; new interconnection techniques / scalability
MPG Halbleiterlabor	direct wafer bonding; 3D/2.5D systems with micro-channel cooling; W2W/C2W bonding
ORNL	in-house interconnect for hybridisation and module building: single-chip bumping, UBM, bonding; gold studs, ACP/ACF, Cu pillars; chip-to-flex, chip-to-interposer; interposer fabrication

ECFA Detector R&D Roadmap



- Many ongoing and planned projects with common interest or complementary to WP 1.3 activities
- Definition of (resource-loaded) WP-Projects ongoing – should we aim for common EP R&D approach?
- 1st DRD3 collaboration workshop June 17-21, 2024 at CERN

Conclusions + Plans

Achieved during phase I:

- Development of in-house plating and interconnection processes
  - Current focus: yield consolidation, reproducibility, documentation
- Proof-of-concept assembly + module prototypes across different projects
- Strong links to internal and external partners
- Shared infrastructure investments beneficial for the wider community

Plans for phase II:

- Further exploration and identification of alternative interconnect technologies
- Enlarged collaboration within DRD3 WG7
- Reliability testing – radiation hardness, thermomechanical stress
- Extend module studies to hybrid/monolithic chips developed in other WPs
- Scalability – larger-area assemblies and modules, demonstrators
- Fully-integrated low-mass modules: mechanical, electrical and photonics (WP6)

Presentations and publications in 2023/24

Presentations:

- M. Vicente, 100μPET: Ultra-high-resolution PET imaging with MAPS, TREDI 2023
- J. Schmidt, Pixel detector hybridisation with anisotropic conductive adhesives, TREDI 2023
- P. Svihra, Beam-test Evaluation of Single-die Bonded Hybrid Assemblies and Timepix3-iLGAD Devices, BTTB 11 Workshop
- P. Svihra, Single die hybridisation of small-pitch pixel detectors, VELO Upgrade II workshop 2023
- M. Van Rijnbach, Studies of multi-chip modules and test beam characterisation (WP1.3), EP R&D seminar July 2023
- A. Volker, Pixel detector hybridization and integration with anisotropic conductive adhesives, IPRD23
- F. Dachs, Module development with the MALTA monolithic pixel chip, PSD13 workshop 2023

Publications:

- J.V. Schmidt et al, *Pixel detector hybridisation with Anisotropic Conductive Films*, JINST 18 C01040, 2023
- P. Svihra et al., *Development of novel single-die hybridisation processes for small-pitch pixel detectors*, JINST 18 C03008, 2023,
- J. Weick et al, *Development of novel low-mass module concepts based on MALTA monolithic pixel sensors*, JINST 18 C04003, 2023
- F. Dachs et al, *Development of a large-area, light-weight module using the MALTA monolithic pixel detector*, NIMA 1047 (2023) 167809
- M. van Rijnbach et al., *Performance of the MALTA telescope*, EPJ-C 83(7) 571 (2023)
- F. Dachs et al., *Quad-Module characterization with the MALTA monolithic pixel chip*, NIMA 1064 (2024) 169306
- A. Volker et al., *Pixel detector hybridization and integration with anisotropic conductive adhesives*, JINST 19 C05024, 2024
- D. Dannheim and P. Riedler, *Silicon-detector modules for future experiments*, EP Newsletter March 2024

Additional Material

WP 1.3 Silicon Modules – Plans 2024-2028

2024	2025	2026	2027	2028
Explore interconnection technologies (ACF, nanowires, jet-printing, Ni/Au in-house processing line)		Interconnection in-house process (establish and validate process available for range of applications and prototypes)		
Compact module layout studies (el. and mechan. connections, integrate optical data transmission (working with WP6), scalability to large areas)				
Validation tests in laboratory +	Radiation / reliability testing of interconnection structures and modules (validation of concepts, performance and reliability)			
			Testbeam validation (scalable large area modules before and after irradiation w + w/o optical data transmission)	

Plans for the next phase:

- Further exploration of **alternative interconnect technologies**
- **Scalability** – larger-area assemblies and modules
- Addressing **reliability** requirements (robustness, radiation hardness)
- **Fully-integrated** low-mass modules: mechanical, electrical and photonics
- Shared **infrastructure investments** to support the R&D
- Activities are part of **ECFA DRD3** collaboration (WG 7)

Date	Deliverable
Q4/25	Identification of in-house low cost interconnection techn.
Q4/26	Module concept study for integrating photonics chips
Q4/27	Radiation testing of interconnection structures and modules
Q4/28	Test-beam validation of a module concept with photonic chip
Q4/28	Demonstration of a scalable in-house interconn. process

Test structures – process steps

- Fused silica wafer
- 14 steps
- 2 lithography steps
- Aluminum pads
- SiO_2 passivated
- Fully working
- Process time ~3 days

Step	Process description	Cross-section after process
01	**Substrate**: fused silica, ***thickness > 300um*** *Piranha cleaning* Machine: *UFT Piranha*	
02	*Ti + Al evaporation* Machine: *EVA760* Ti: 0.01 *μm* Al: 3 *μm*	
03	*HMDS + Photolith PR coat* Machine: YES 310TA (Z1) + *EVG150* PR : AZ1512 – *1.1 μm*	
04	*Photolith PR expo* Machine: MLA150 405 nm, 55 mJ/cm2 *CD > 10 um*	
05	*PR develop (manual)* Machine: AZ developer (Z13) *+ short O2 plasma Descum* *(10s Tepla low – Z2)*	
06	*Aluminum + Ti wet-etch* Machine: *Plade Metal (Z2)* Depth : 3.01 *μm*	
07	*Resist Strip on UFT* Material: AZ1512 – *1.1 μm* Machine: UFT Remover	
08	*Sputtering 0.5um SiO2 deposition* *Machine: Pfeiffer Spider 600*	
09	*HMDS + Photolith PR coat* *Machine: YES 310TA (Z1)* *+ EVG150* *PR : AZ1512 PR with HMDS – 1.5 μm*	
10	*Photolith PR expo + develop* *Machine: MLA150 + EVG150* *CD ~ 5 um* 405 nm, 240 mJ/cm2 *+ short O2 plasma Descum* *(10s Tepla low – Z2)*	
11	*SiO2 wet-etch with BHF 7:1* *Machine: Plade Oxide (Z2)*	
12	*Resist Strip* *Material: AZ1512 PR with HMDS – 1.5 μm* *Machine: UFT*	
14	*Dicing* *Front-side interfacing dicing tape*	

Nano wire bonding principle

Main process steps for growing the nano wires on the desired chip pads:

MALTA2 Pad

Flex Pad

Photolithography opening of pad

MALTA2 Pad

Flex Pad

Apply seed layer

MALTA2 Pad

Flex Pad

Apply nano-structure on chip pad

MALTA2 Pad

Glue

Flex Pad

Glue addition possible in flip-chip process

MALTA2 Pad

Flex Pad

Connection through pressure and heat

Pads can be interconnected using nano-structure with different bonding principles:

- **Sinter** process (glue-free)
- **Cold welding** with nano-structuration on one or both, chip and flex (glue-free)
- **Glue supported** bonding for more mechanical stability and lower pressure and heat needed during bonding