EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

WP 5 – IC TECHNOLOGIES

EP R&D day

CERN

22 May 2024

WP5 - IC Technology activities organization

Research novel solutions for ASIC design, powering, and interconnects

&

Develop an infrastructure to sustain them in advanced technology nodes

Lead by K. Kloukinas, D. Ceresa (deputy)

5.1 Technology Evaluation	5.2 IP block development	5.3 Intelligence on Detector (IoD)	5.4 Powering solutions	5.5 3D Interconnect solutions NEW!
G. Borghello	*R. Ballabriga*	*A. Caratelli, D. Ceresa*	*S. Michelis*	*K. Wyllie*
D. Ceresa	F. Bandi	M. Andorno	P. Antoszczuk,	M. Campbell
G. Bergamin	T. Hoffman	F. Brambilla	G. Bantemits	K. Kloukinas
R. Pejasinovic	M. Piller	B. Denkinger	S. Koseoglou	F. Piernas Diaz
F. Piernas Diaz		J. Dhaliwal	G. Ripamonti	J. Alozy
		A. Nookala	N. Van Der Blij	
		R. Pejasinovic	M. Macaluso	
		K. Kloukinas	A. Ocarino	

WP5.1 TECHNOLOGY EVALUATION

Qualify advanced technologies in terms of performance and radiation hardness

&

Select the node for future ASIC design (~2023-2033)

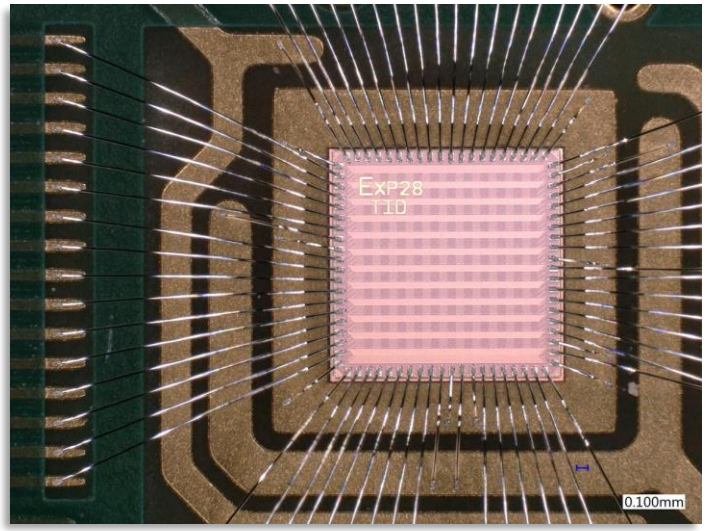
Design several test-chips to qualify technologies with:

- Performance, Power, and Area metrics
- Total Ionizing Dose (TID) studies
- Single Event Effects (SEE) studies

Test with a common and flexible test system, including:

- X-Ray for TID studies
- Heavy-Ion testing, proton, and laser testing for SEE studies

Analyze and Share the results!



EXP28-TID chip photo

WP5.1 TECHNOLOGY EVALUATION

Qualify advanced technologies in terms of performance and radiation hardness

&

Select the node for future ASIC design (~2023-2033)

Selected a 28nm bulk CMOS technology

as the mainstream process for future Rad-Tol designs:

- High-k gate oxide is not a problem
- Lower degradation than 65nm
- Short transistors are more radiation hard

Extensive reports for tech. users distributed by ASIC support:

https://asic-support-28.web.cern.ch/tech-docs/radtol/

Ionizing Radiation Effects
On 28 nm CMOS Technology

~64 pages

SEE Characterization
Of A Commercial
28nm CMOS Technology

~50 pages

Publications

Submitted to RADiation Effects on Components and Systems (RADECS) Conference

ELDRS in a commercial 28nm CMOS technology

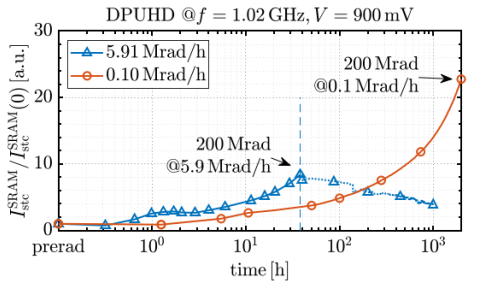


Fig. 1. Static current in DPUHD SRAMs irradiated to 200 Mrad(SiO_2) at different DRs.

*Enhanced Low Dose Rate Sensitivity

WP5.1 TECHNOLOGY EVALUATION

Qualify advanced technologies in terms of performance and radiation hardness

&

Select the node for future ASIC design (~2023-2033)

WHAT'S NEXT?

Continue Technology survey and evaluation (*at a much slower pace*)

- Advanced IC technologies; acquire access and performance evaluation
  - FinFET (radiation evaluation, develop design expertise)
  - FD-SOI (non Rad-Tol applications)
- Specialty & Emerging IC devices; evaluation, customization
  - ReRAM (Resistive Non-Volatile Memories)
  - MRAM (Magnetoresistive Non-Volatile Memories)
  - Ultra low leakage SRAM

WP5.2 IP Blocks development

Design and characterize the components enabling chip development

&

Create an infrastructure to share design across the community

IP block design	Status
Bandgap voltage reference	Tested
8-bit Digital-to-Analog Converter	Tested
Differential Driver & Receiver ~1.28 Gbps	Tested
Rail-to-rail Operational Amplifier	Tested
Rad-Tol ESD protection (SOFICs)	Tested
CMOS bi-directional pad (SOFICs)	Tested
Analog-Digital PLL	To be tested
Analog-to-Digital Converter	Under design

Make it available to the community!

Complete the IP-block packaging by providing:

- Datasheet according to template
- Digital-on-Top integration files (abstract + lib files)
- Verilog model for simulation

Load on the ClioSoft repository managed by the ASIC support

Experience gathered in a ***Designer's guide*** available on the ASIC Support website:
https://asic-support-28.web.cern.ch/tech-docs/designers-guide/

WP5.2 IP Blocks development

Design and characterize the components enabling chip development

&

Create an infrastructure to share design across the community

WHAT'S NEXT?

- Expect to complete and deliver all IP blocks by 2024-25
- Maintain IP block repository by CERN ASIC support service
- No further IP block development is foreseen within the EP R&D WP5
- HEP community is invited to contribute with IP blocks
- Aim to establish an IP block sharing mechanism

WP5.3 Intelligence on Detector

Develop a Rad-Tol System-on-Chip – SoC Ecosystem

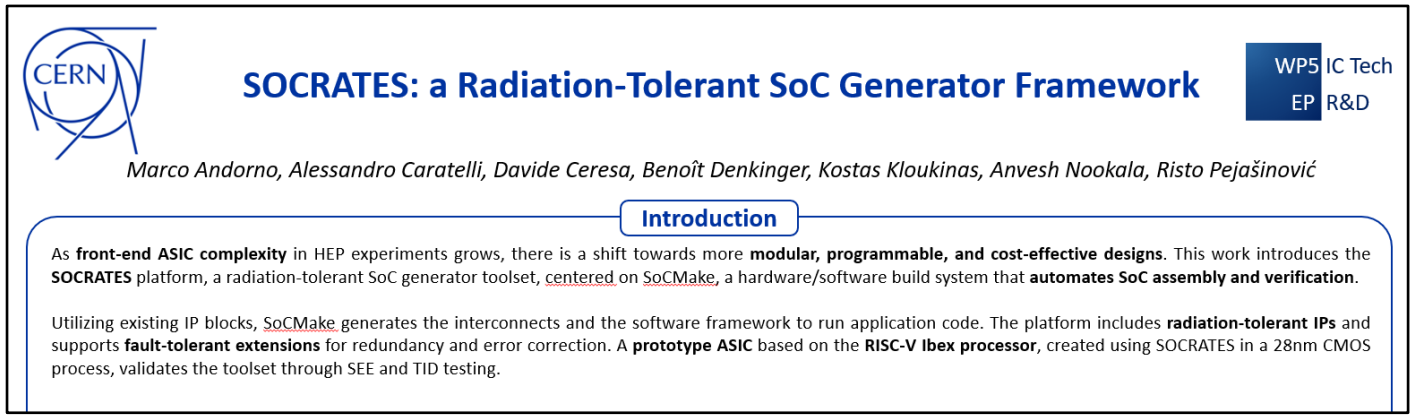
&

Explore On-chip data processing solution

SOCRATES framework:

- A radiation-tolerant SoC generator toolset
- Based on SoCMake, a hw/sw build system for automated SoC assembly and verification
- RISC-V processor-based architecture

Poster # 29



CERN

SOCRATES: a Radiation-Tolerant SoC Generator Framework

WP5 IC Tech EP R&D

Marco Andorno, Alessandro Caratelli, Davide Ceresa, Benoît Denkinger, Kostas Kloukinas, Anvesh Nookala, Risto Pejašinović

Introduction

As **front-end ASIC complexity** in HEP experiments grows, there is a shift towards more **modular, programmable, and cost-effective designs**. This work introduces the **SOCRATES** platform, a radiation-tolerant SoC generator toolset, centered on SoCMake, a hardware/software build system that **automates SoC assembly and verification**.

Utilizing existing IP blocks, SoCMake generates the interconnects and the software framework to run application code. The platform includes **radiation-tolerant IPs** and supports **fault-tolerant extensions** for redundancy and error correction. A **prototype ASIC** based on the **RISC-V Ibex processor**, created using SOCRATES in a 28nm CMOS process, validates the toolset through SEE and TID testing.

WP5.3 Intelligence on Detector

Develop a Rad-Tol System-on-Chip – SoC Ecosystem

&

Explore On-chip data processing solution

WHAT'S NEXT?

TriglaV – Rad-hard demonstrator SoC :

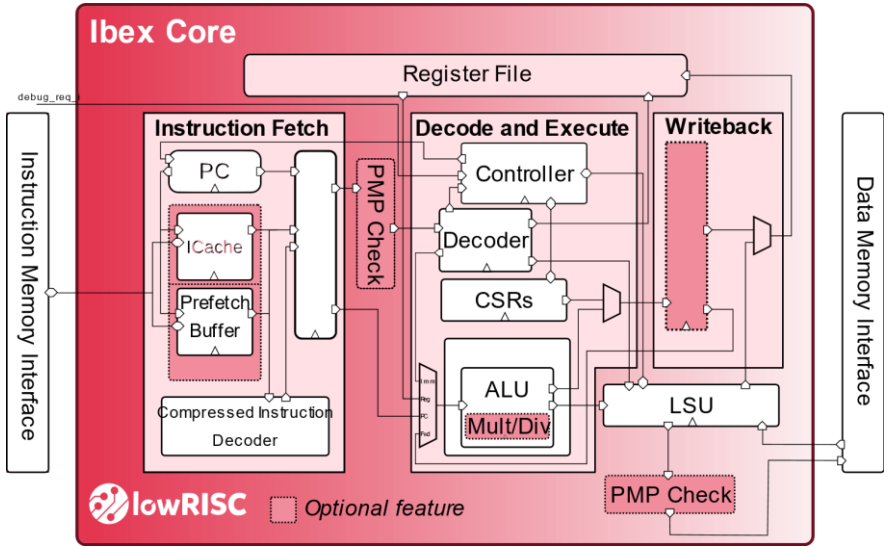
Processor: Full-TMR Ibex Core RV32IMC

Technology: 28nm bulk CMOS

Memory: Multi Bit Upset (MBU)-robust Memory

Interconnect: Rad-Tol Interconnects

Prototype submission foreseen in Q4-2024!



Ibex core by lowRISC

WP5.3 Intelligence on Detector

Develop a Rad-Tol System-on-Chip – SoC Ecosystem

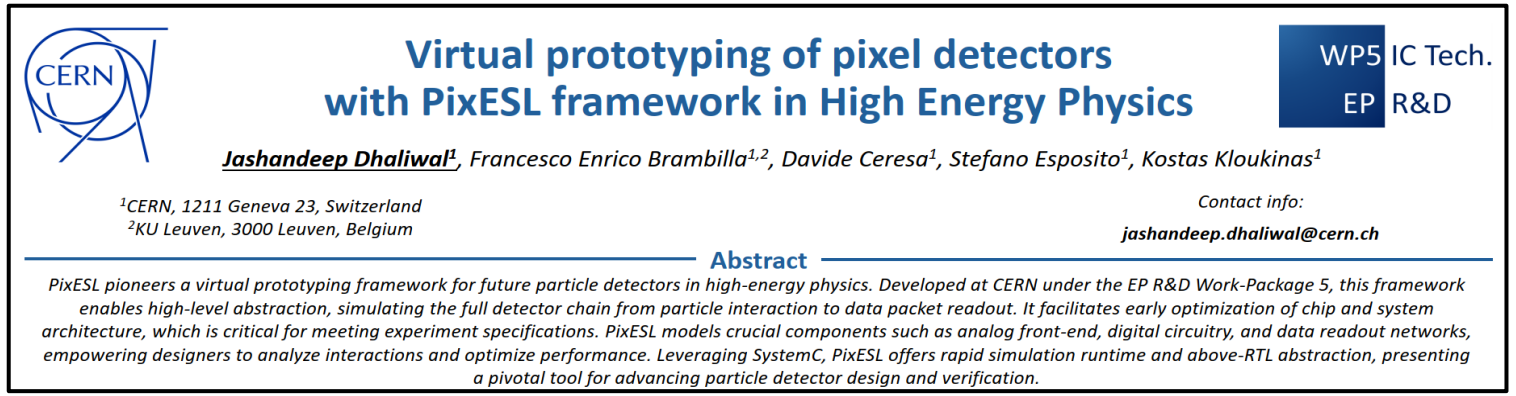
&

Explore On-chip data processing solution

PixESL framework:

- Virtual prototyping framework for particle detectors design
- System-C/C++ simulation from analog front-end to back-end
- Used for LHCb VeLo upgrade II architecture exploration [ref]

Poster # 28



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Virtual prototyping of pixel detectors with PixESL framework in High Energy Physics

WP5 IC Tech. EP R&D

Jashandeep Dhaliwal[1], Francesco Enrico Brambilla[1,2], Davide Ceresa[1], Stefano Esposito[1], Kostas Kloukinas[1]

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Abstract

PixESL pioneers a virtual prototyping framework for future particle detectors in high-energy physics. Developed at CERN under the EP R&D Work-Package 5, this framework enables high-level abstraction, simulating the full detector chain from particle interaction to data packet readout. It facilitates early optimization of chip and system architecture, which is critical for meeting experiment specifications. PixESL models crucial components such as analog front-end, digital circuitry, and data readout networks, empowering designers to analyze interactions and optimize performance. Leveraging SystemC, PixESL offers rapid simulation runtime and above-RTL abstraction, presenting a pivotal tool for advancing particle detector design and verification.

WP5.3 Intelligence on Detector

Develop a Rad-Tol System-on-Chip – SoC Ecosystem

&

Explore On-chip data processing solution

WHAT'S NEXT?

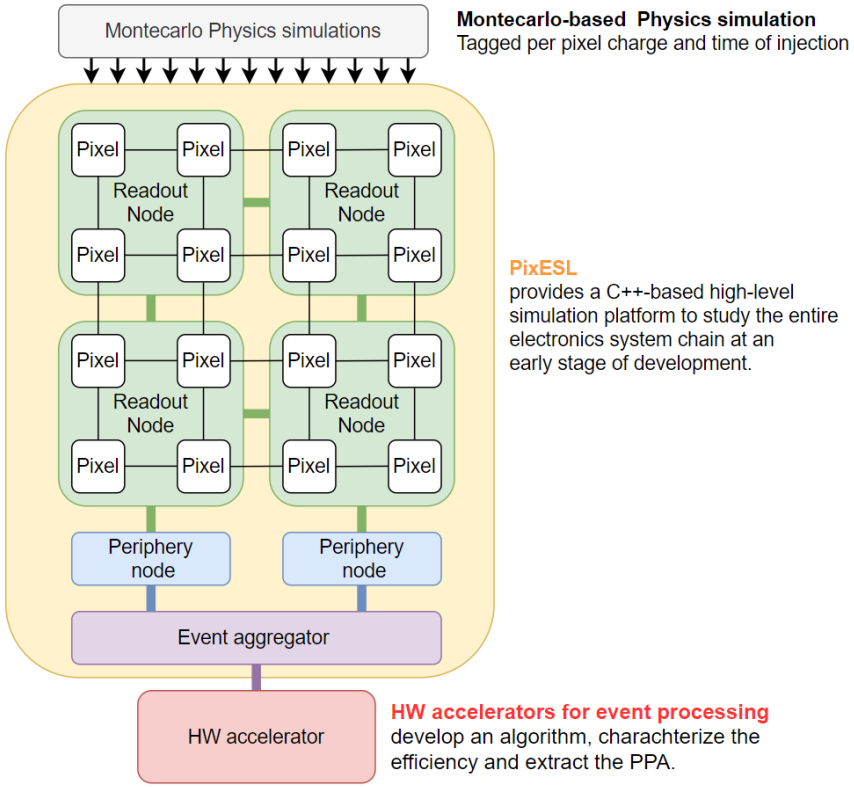
Develop HW accelerators for event processing :

Applications: Particle clustering, Particle filtering or recognition

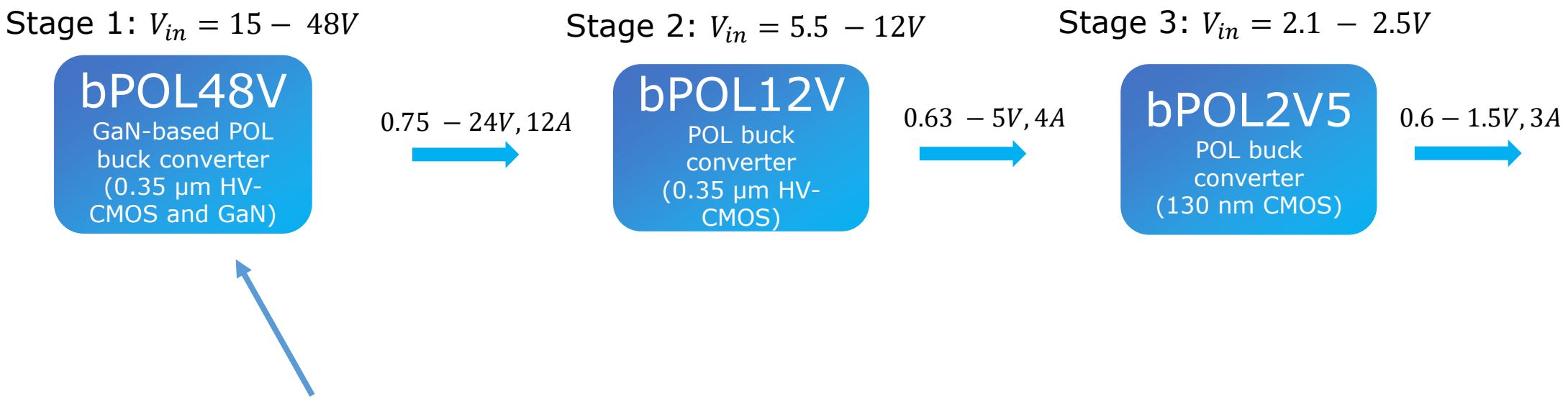
Architecture: Periphery processing vs Distributed processing

Technology: Explore edge-computing solution

- Neural network
- ASIP (Application Specific Instruction Processors)
- …

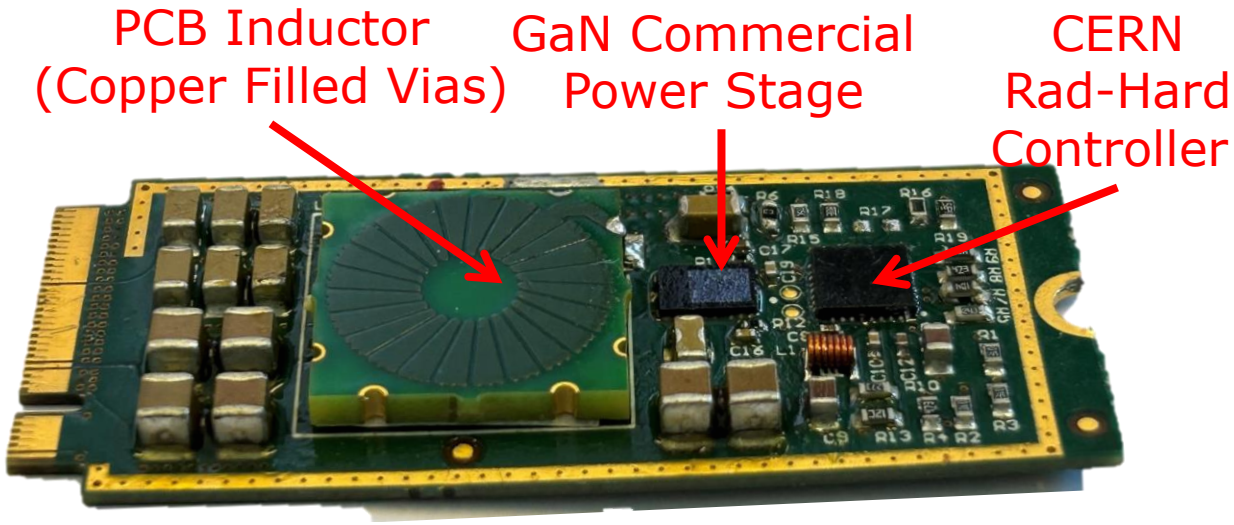


Available power distribution scheme (WP5.4)



bPOL48V developed with first EP-R&D WP5.2

48V DCDC module converter development (WP5.4)



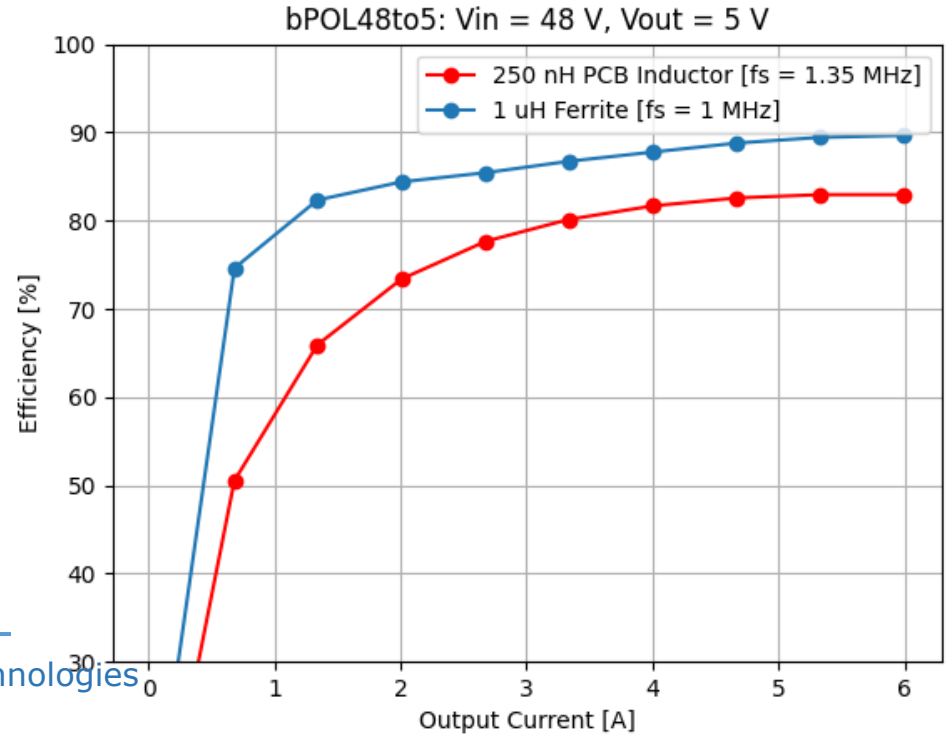
Using available stock of bPOL48V (~70K dies)

Volume optimized bPOL48 modules:

- bPOL48to12 (EPC2152): 48V to 12V with 6A out
- Dimensions: 24 x 55 x 4 mm

PCB Inductor:

- Inductance: 100-400 nH
- Size: 15 x 15 x 3 mm
- Similar performance to wire wound air-core inductors



R&D for future power distribution schemes (WP5.4)

(production fab closed for both technologies)

Stage 1: $V_{in} = 15 - 48V$

bPOL48V developed with first EP-R&D WP5.2

$0.75 - 24V, 12A$

Stage 2: $V_{in} = 5.5 - 12V$

$0.63 - 5V, 4A$

Stage 3: $V_{in} = 2.1 - 2.5V$

bPOL2V5
POL buck converter (130 nm CMOS)

$0.6 - 1.5V, 3A$

NEW RD

Stage 1: $V_{in,max} = 48V$

Gen2 GaN-based 48V DC-DC
Input, output voltage and load current range are being defined

5V or 2.3V

Stage 2 on chip

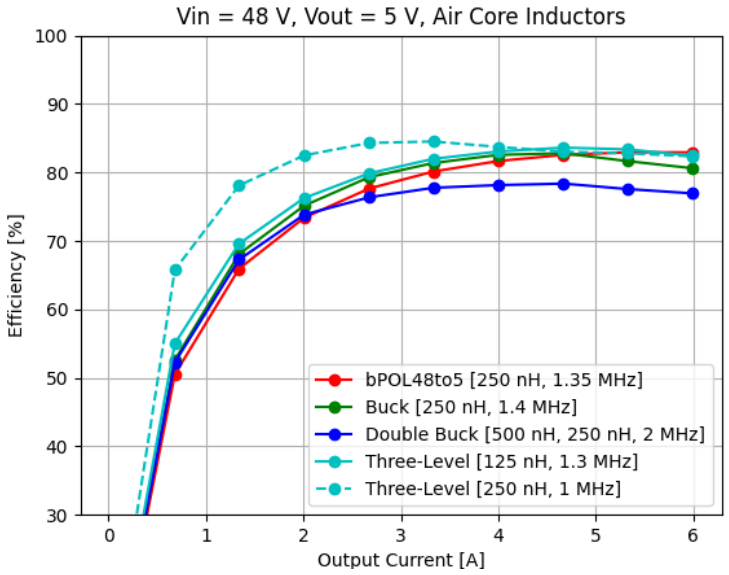
Smart powering in front-end ASICs

Stage1: 48V new converter R&D (WP5.4)

Converter topology

- Optimization algorithms in Python
- Different prototypes with microcontroller

Promising topologies: Buck, 3 and 5 -Level Buck, (Berkely) Series Capacitor Buck



ASIC design

- New CMOS High Voltage (HV) technology selected
- Design of the new controller started
- We have already all linear regulators designed

Stage2: smart power and 28nm On-chip regulation (WP5.4)

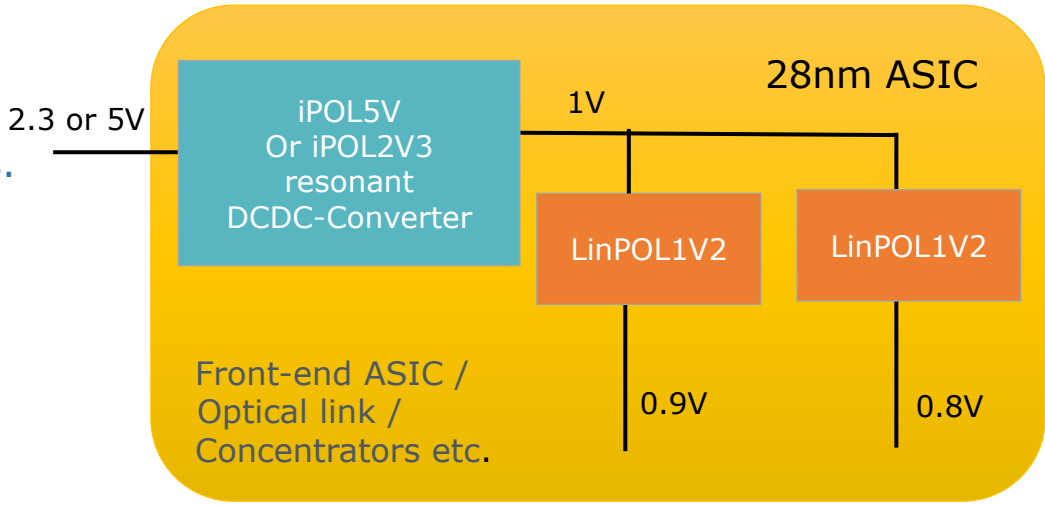
Smart distribution on chip is necessary to limit the power requirements.

A fully integrated DCDC will provide a ~1V on chip from 2.3V or 5V power bus.

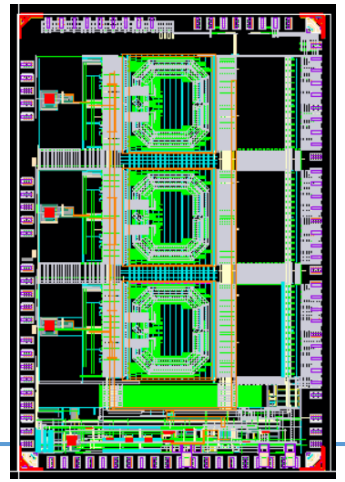
Different part of the circuit can be supplied with different voltages with full integrated LDO

This innovative power distribution scheme do not require additional external components: input-output capacitors and inductors are fully integrated

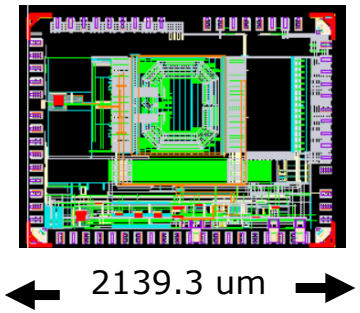
3 ASICS have been submitted in Nov2023 and today under testing



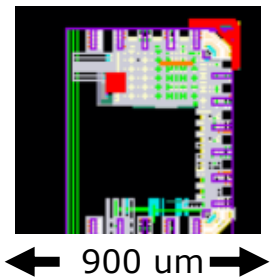
iPOL5V
Resonant
5V to 0.9V-1V



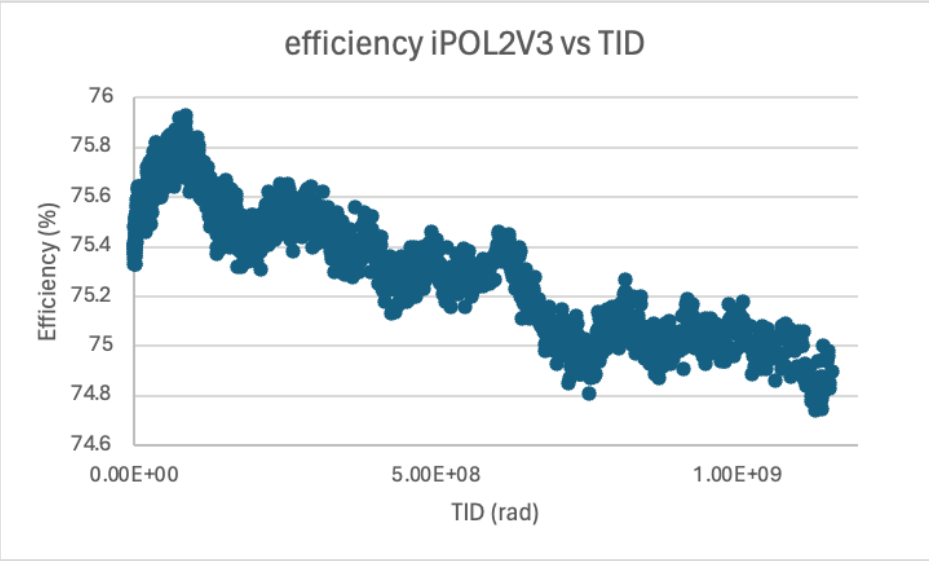
iPOL2V3
Resonant
2.3V to 0.9V-1V

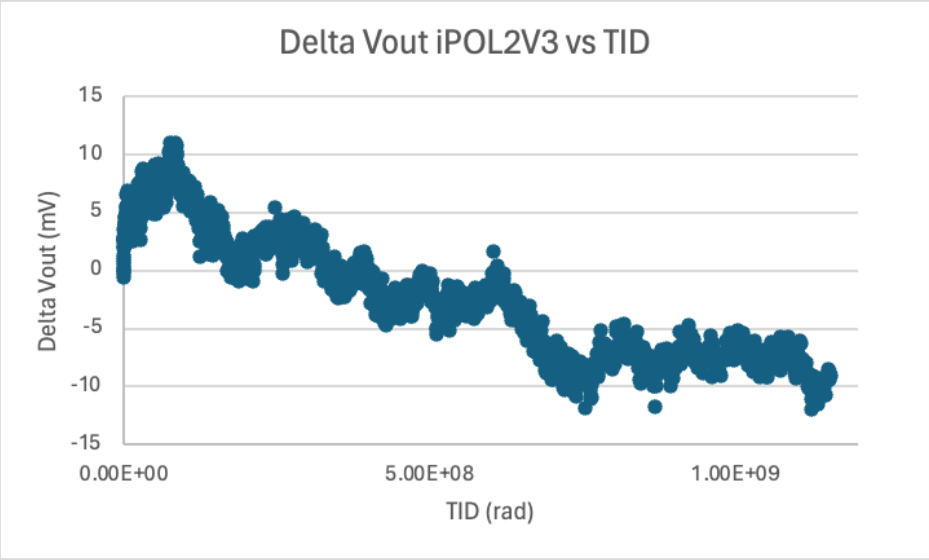


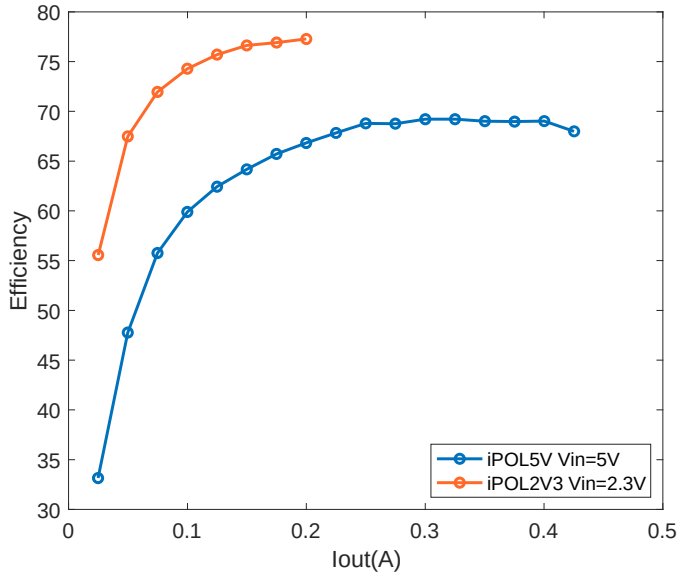
linPOL1V2
Linear regulator
1V to 0.8V-0.9



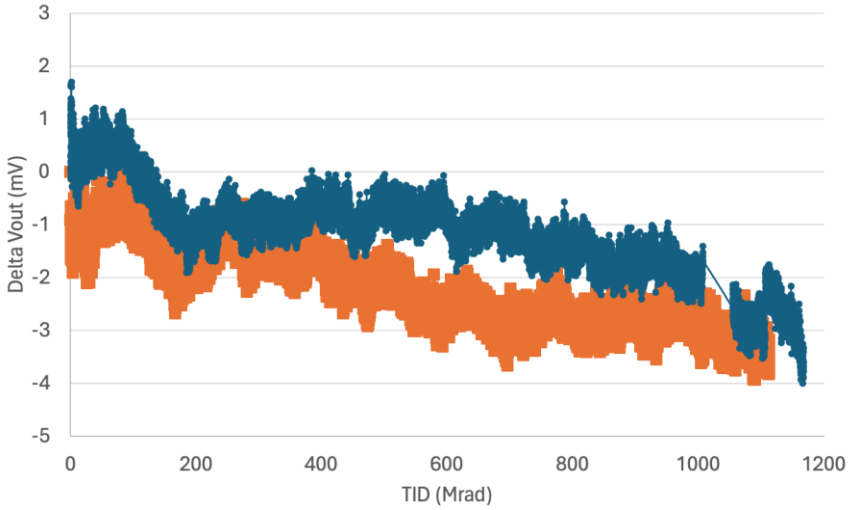
Stage 2 ASICs results





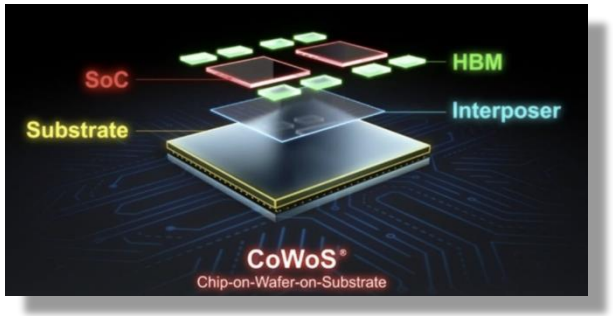


Delta Vout LinPOL1V2 vs TID

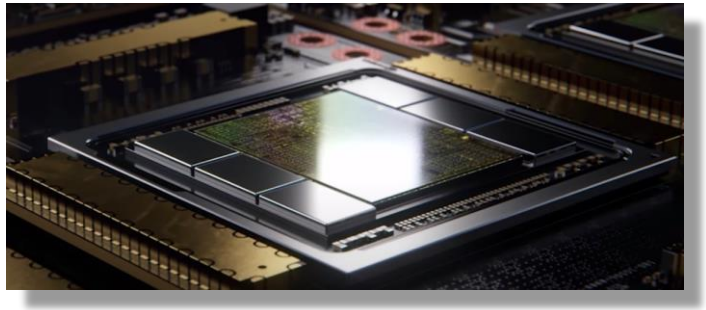


WP5.5 Advanced Packaging and 3D Interconnects

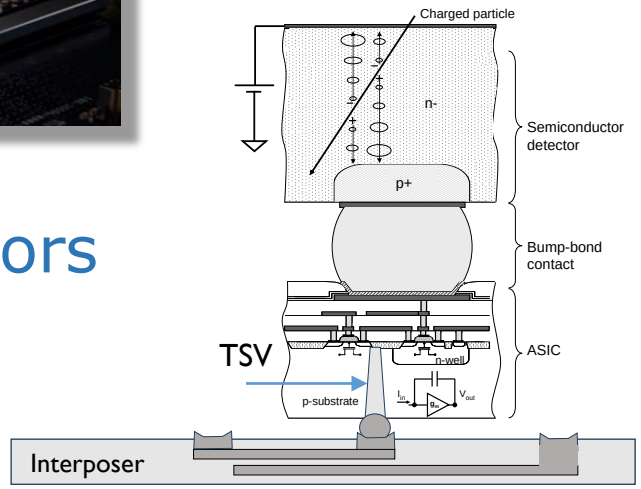
- 3D-IC: Die stacking technology offering new levels of PPA[1] efficiency.
  - Accommodate multiple heterogeneous die integration (logic, memory, analog, SiPh, etc)
  - Promise more than Moore integration postponing an expensive move to advanced nodes
  - Vast Ecosystem of solutions (microbumping, TSVs, silicon interposers, wafer-to-wafer, wafer-to-die, die-to-wafer bonding,…)



Powering AI



- TSVs: an enabler for many applications in HEP detectors
  - Hybrid pixel detectors
  - Cover large areas butting detectots on all 4-sides
  - Solid powering and global signal interconnect solutions

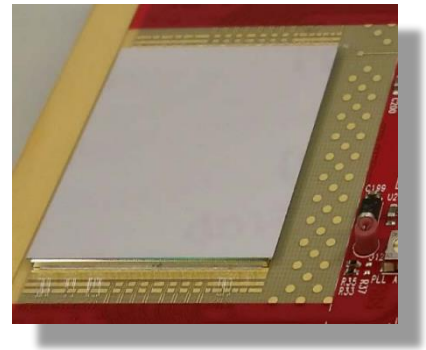


[1](Power, Performance, Area)

3D-IC: TSV solutions

Ken Wyllie (WP5.5 leader)
Michael Campbell
Kostas Kloukinas

- Scope: Find vendors offering reliable and affortable TSV solutions

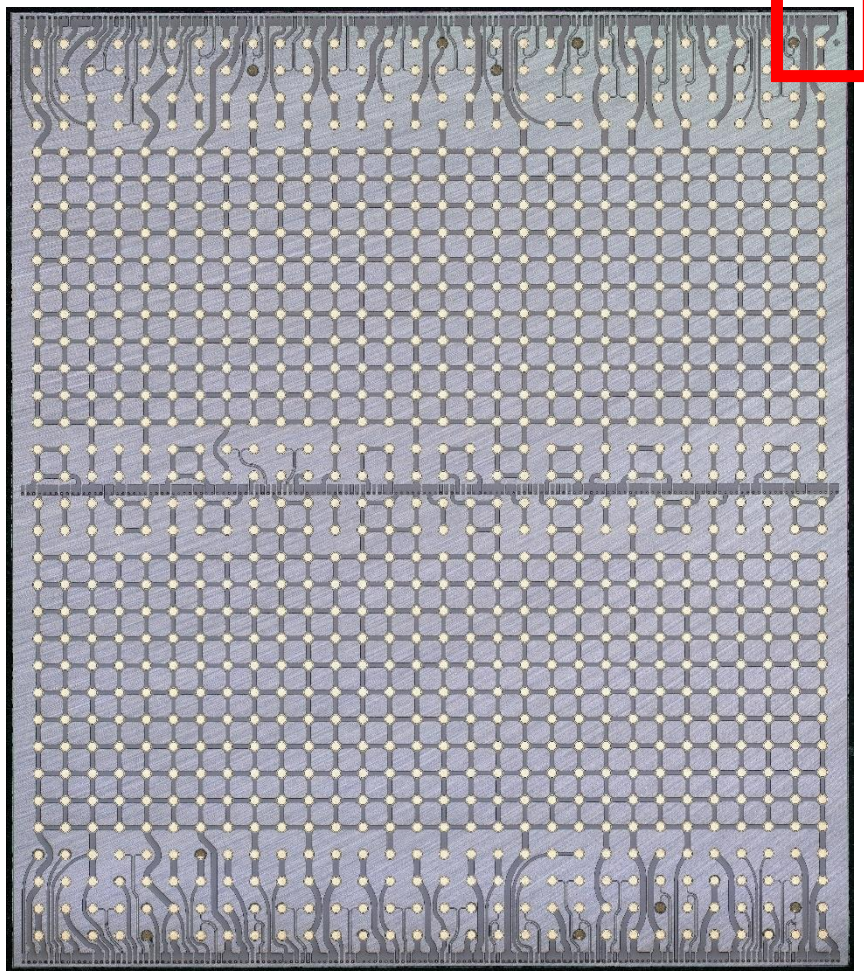


- Use the Timepix4[1] pixel readout ASIC as a test vehicle to qualify TSV processes
- Three vendors expressed interest in working with CERN on TSVs
  - Two in Europe (one with limited support for 200mm wafers)
  - One in Taiwan (support for 300mm wafers)
- Currently discussing technical details with them and planning to make orders in the coming months

[1] *X. Llopart et al*

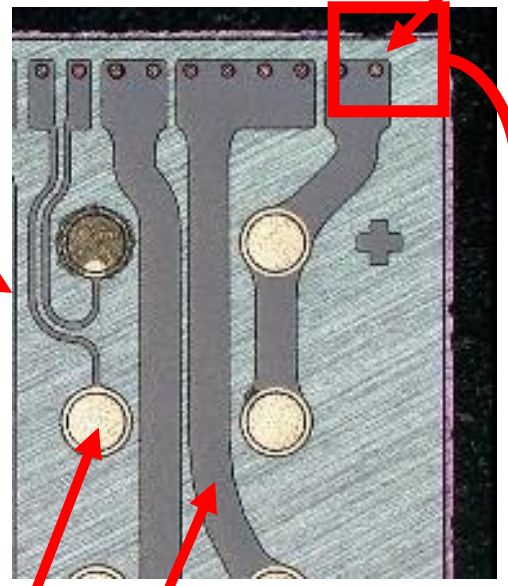
For WP5.5: Francisco Piernas Diaz
Jerome Alozy

First prototypes from wafers cored to 200mm



TIMEPIX 4[1]
Bottom side

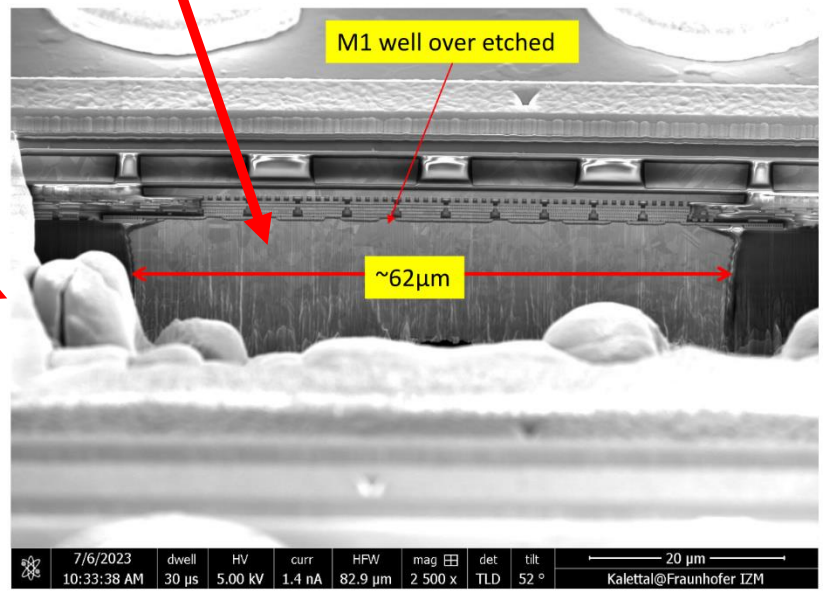
[1] *X. Llopart et al*



Through Silicon Via (TSV)

BGA Pad

Redistribution Layer (RDL)



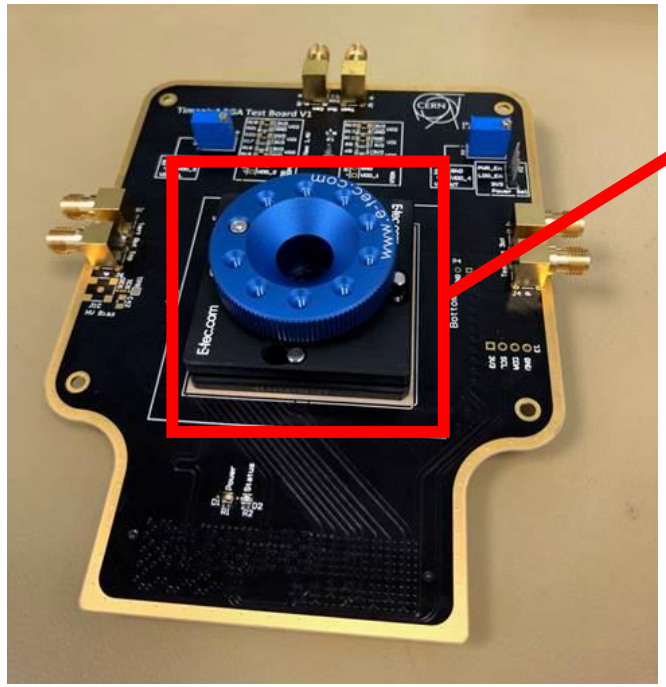
TSV cross section under SEM (Fraunhofer IZM)

- Researching TSV as replacement for wirebonding
- Allows better signal integrity with less parasitics
- Allows better power integrity when accessing the whole bottom area

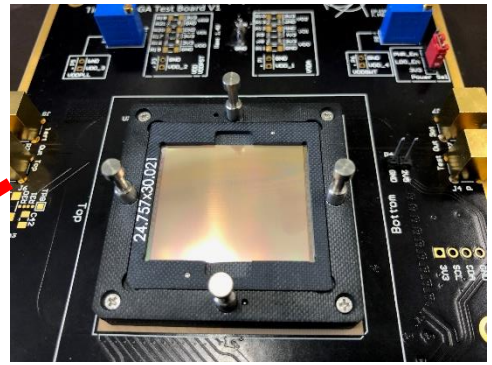
The bondpads are diced out -> 4 side butting

Testing the TSV options

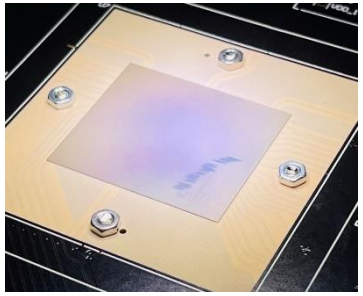
For WP5.5: Francisco Piernas Diaz
Jerome Alozy



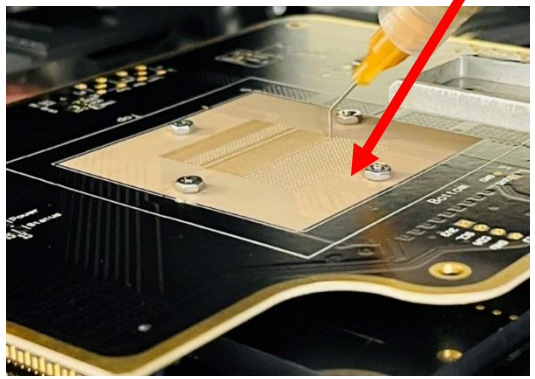
Test socket PCB



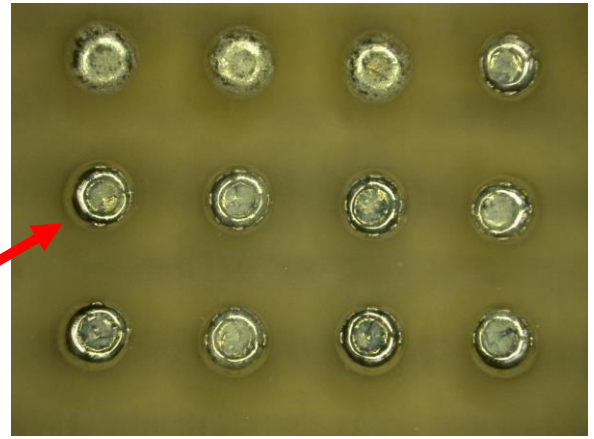
Pogo-pin based socket that allows validating TSV-processed chips



Chip to PCB soldering trials

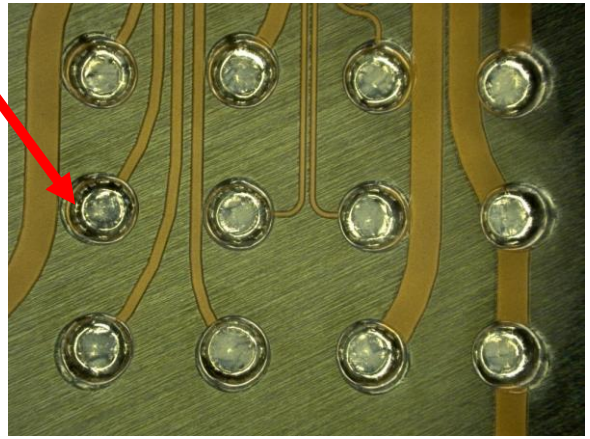


A. Balling the PCB first then solder:



OR

B. Balling the chip first then solder:

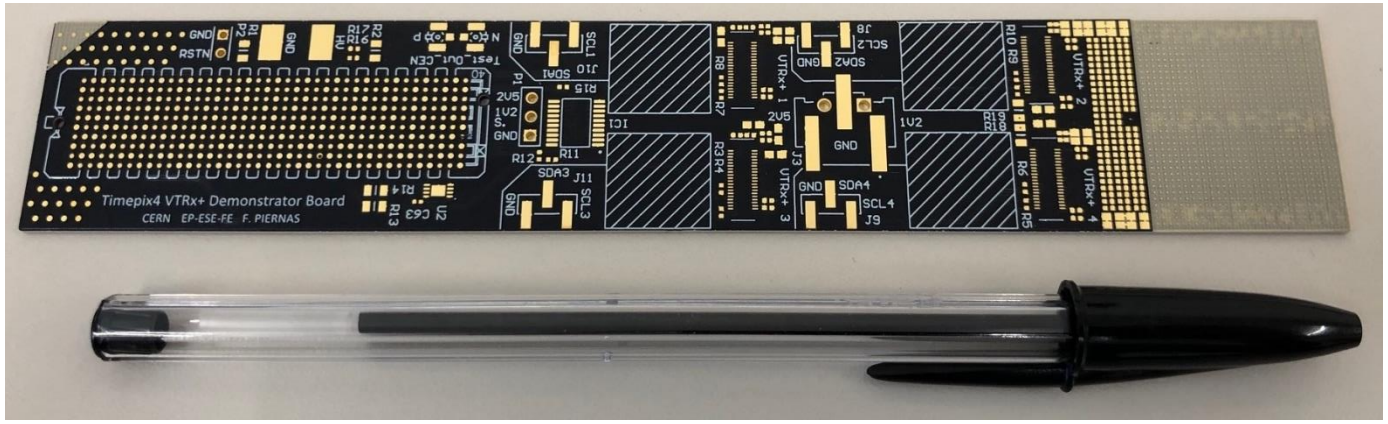


C. Anisotropic Conducting Paste at UniGE

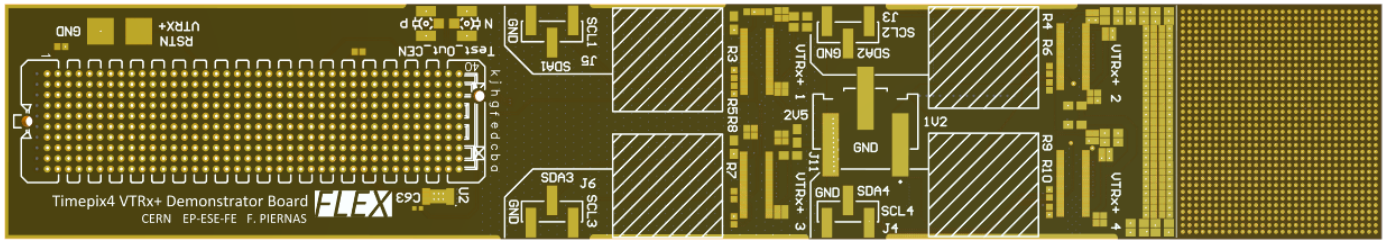
Mix of glue and tiny metal spheres.
Bonding by thermocompression.

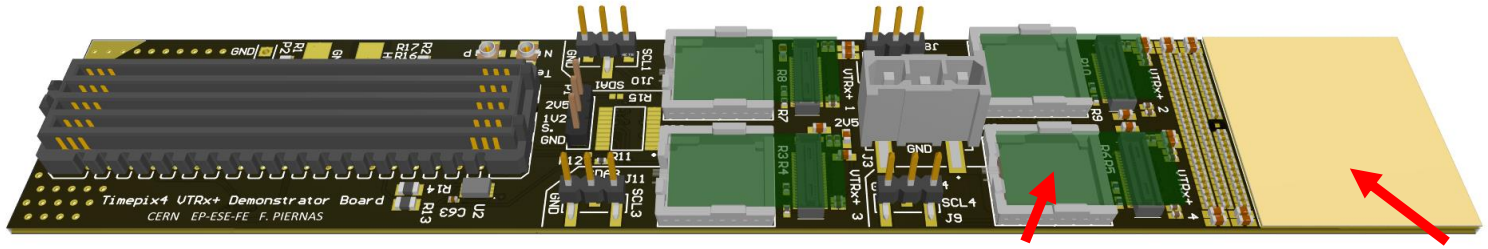
Opto-electronics and silicon photonics

For WP5.5: Francisco Piernas Diaz
Jerome Alozy



2-Side buttable demonstrator module integrating Timepix4 TSV processed and four VTRx+ opto-electronics modules

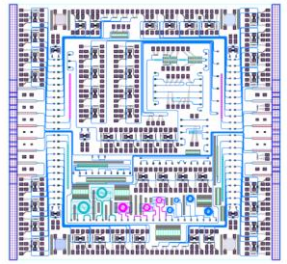




VTRx+ module in transparency

Timepix4 TSV

Proposal to make the future **Velopix/Picopix** able to drive SiPho @25Gbps, or VTRx+ @12.5Gbps.



EP-ESE-BE, PICv2

EP R&D WP5 Phase II

- Activity 5.1: Technology Survey and Evaluation (decelereted pace)
  - Advanced processes, beyond 28nm CMOS
  - Specialty and emerging 28nm devices
- Activity 5.2: IP blocks (phasing out)
  - Deliver CERN developments and invite HEP community to contribute with IP blocks
- Activity 5.3: Intelligence on Detector (phasing in)
  - Risc-V based Rad-Tol SoC Ecosystem for the implementation of future FE ASICs
  - On-detector data processing architectures and system level modelling
- Activity 5.4: Powering Solutions (continues)
  - Stage 1; 48V → 5V: To replace the recently discontinued technology of the HL-LHC DC/DC converters
  - Stage 2; 5V → 0.9V: Finalize the development of the DC/DC converter in 28nm TSMC technology
- Activity 5.5: Advanced Packaging and 3D Interconnects (new activity)
  - Technology survey, acquire access and build expertise
  - Use on-going FE ASIC projects to demonstrate feasibilty and industrialization of the advanced packaging and 3D interconnect technologies

EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

THANKS!

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