Flex-PCB board design for SiPM readout at cryogenic temperatures

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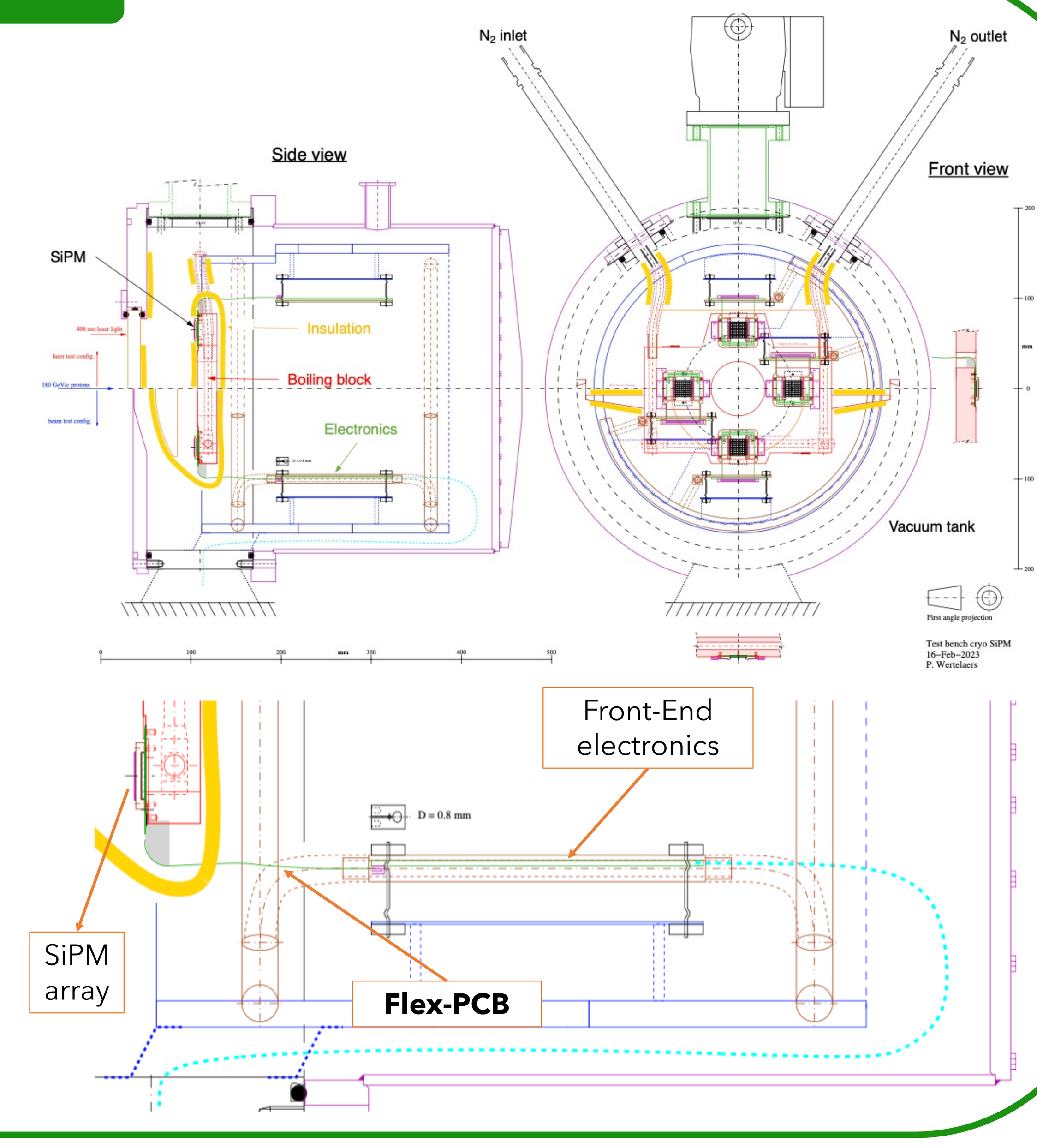
Introduction and motivation

- During the **High-Luminosity LHC phase**, the LHCb RICH detector will face challenges due to increased **particle multiplicity and high occupancy**. [1][2]
- The LHCb RICH collaboration is exploring **new photodetection options** with improved time resolution (<100ps) and smaller pixel size.
- **Silicon Photomultipliers (SiPMs)** are strong candidates for LHC Run 5. However, radiation damage to SiPMs poses a significant challenge, necessitating operation at cryogenic temperatures. [3][4]
- A small-scale test bench to study SiPM arrays at **cryogenic temperatures** is being designed at CERN.
- The **proposed Flex-PCB prototype** is designed to bring signals from an SiPM array to the front-end (FE) electronics with the implementation of long PCB traces, allowing for two different cooling systems:
  - SiPM down to cryogenic (~150k) temperature.
  - Font-End (FE) cooling at room temperature.
- The board will be used to evaluate the impact of high-density long traces between SiPM and FE on the **sensor performance and signal integrity.**

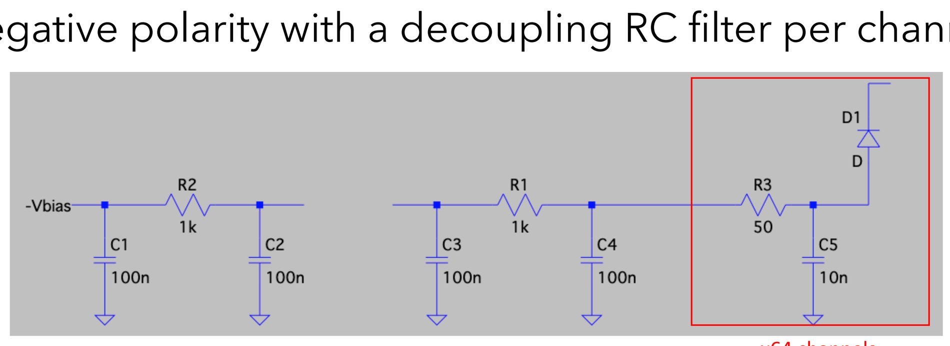
Cryostat demonstrator

- The SiPM will be mounted on a boiling block made of a solid copper piece with a channel for nitrogen flow. [5]
- Two entrance window options:
  - Borosilicate glass for laser light source;
  - Aluminium plate and thinner foil central region for operation in the charged particle beam.
- Secondary cooling system for the FE electronics.
- FE electronics will be based on the FastRICH and lpGBT/VTRX+. [2]



Flex-PCB specifications

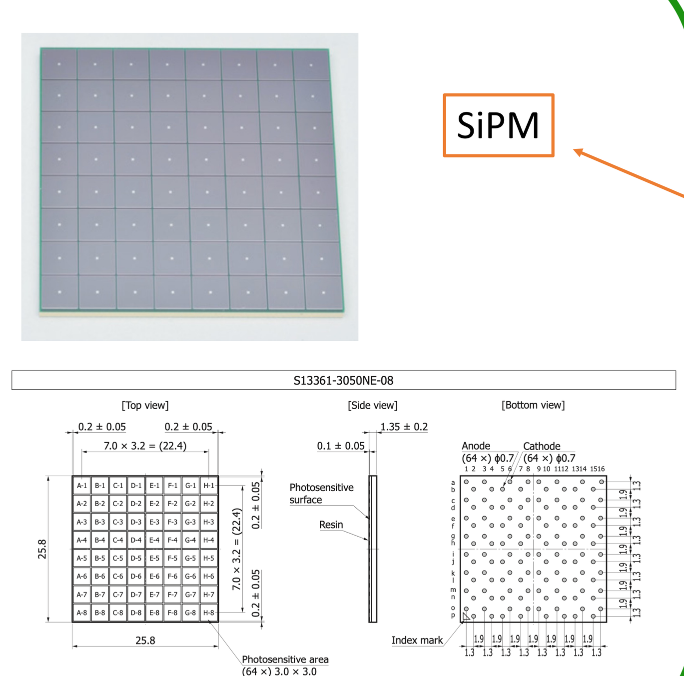
- **Fully flexible 3-layer PCB** for the readout of an SiPM array.
  - High density of channels to be read out.
  - Minimal use of connectors
  - Thin PCB for thermal coupling between sensor and cold block.
- **High-density long traces** for the SiPM channels: 200µm width, 200µm spacing, and ranging from 140 to 170 mm in length.
- Negative polarity with a decoupling RC filter per channel:



- The stack-up (Table) is designed to match 50-100Ω impedance, and it guarantees a bending radius down to 20mm.
- Ground plane and bias distribution were carefully designed to guarantee board symmetry and robustness.
- Test injection circuits and temperature sensor are implemented in the design.

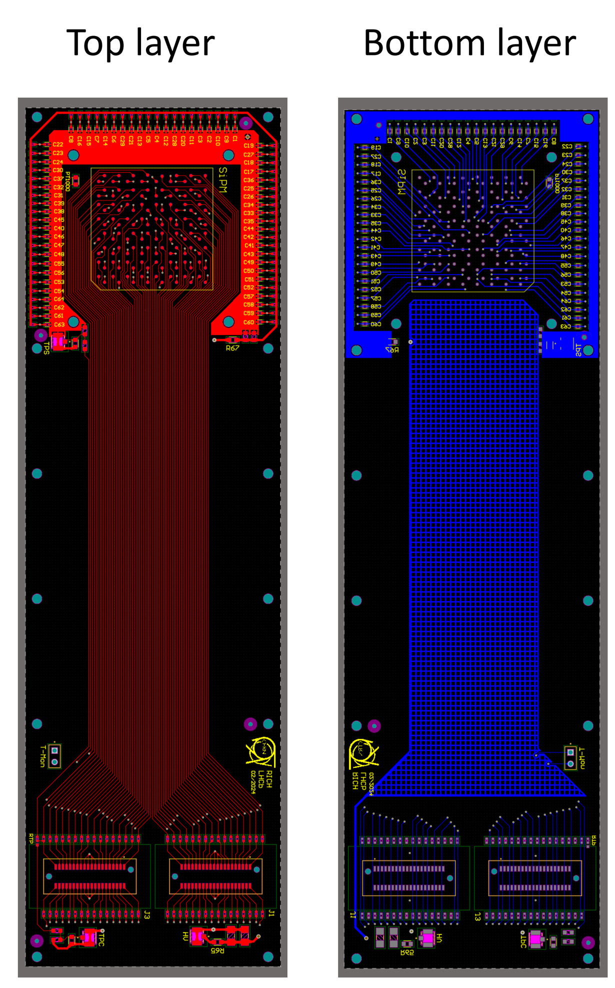
Layer	Thickness	Material	Functionality
Soldermask top	30µm	-	-
Top layer	35µm	Copper	Signal
Dielectric	100µm	Polyimide (Kapton)	-
Glue	50µm	Epoxy glue	-
Inner layer	17µm	Copper	Ground
Glue	50µm	Epoxy glue	-
Dielectric	100µm	Polyimide (Kapton)	-
Bottom layer	35µm	Copper	Bias
Soldermask bot.	30µm	-	-

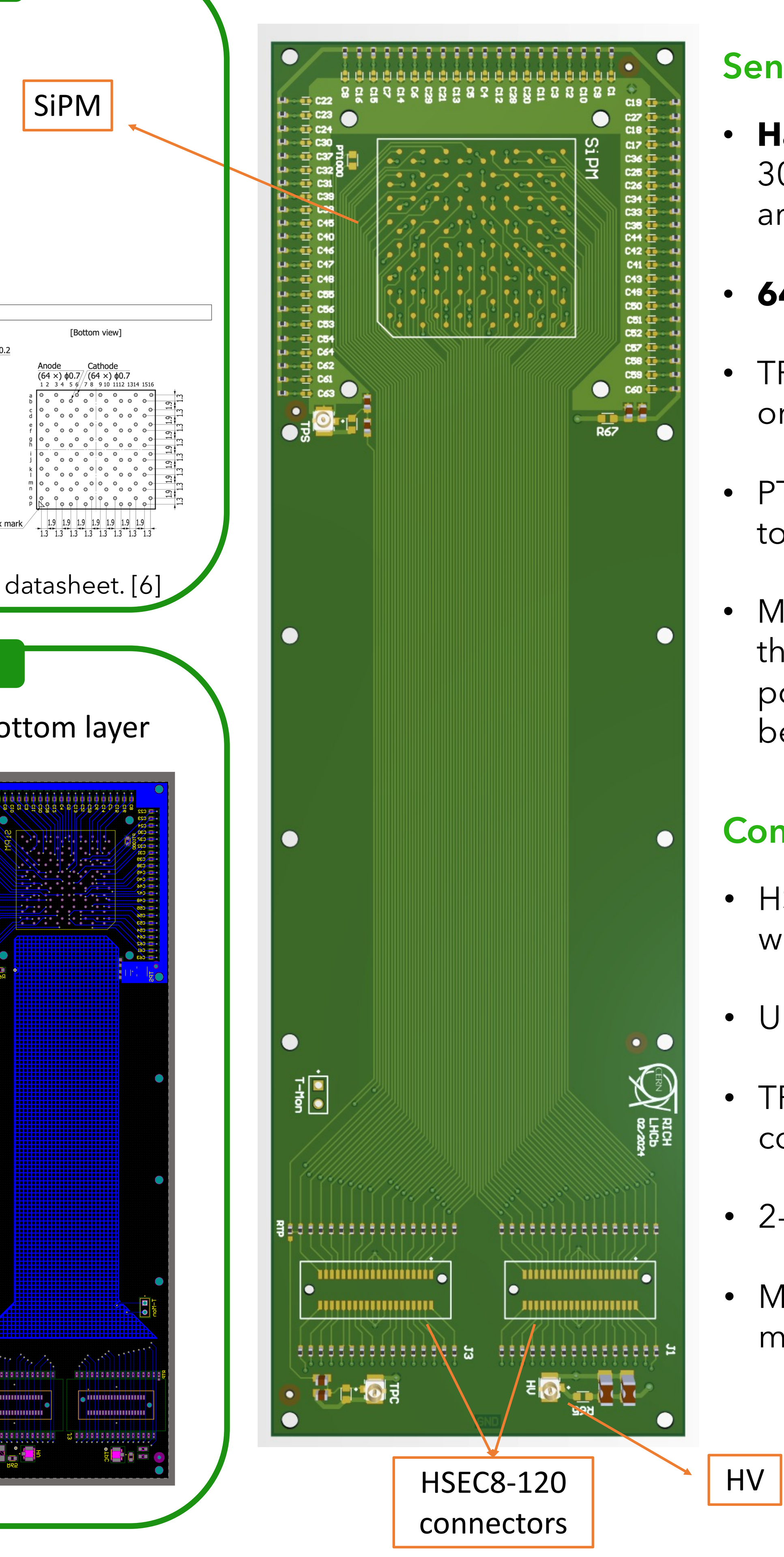
Sensor



Pictures from Hamamatsu datasheet. [6]

Layout





Sensor side

- **Hamamatsu 64- channels** S13361-3050NE-08 **SiPM**. The channels active area is 3x3mm^2, with 50µm SPAD size. [6]
- **64 RC filters** for channel bias decoupling.
- TPS: **test pulse injection circuit** placed on this side to emulate a long trace.
- PT1000 **temperature sensor** placed close to the SiPM.
- Mounting holes at the edges and around the SiPM for mechanical purposes and potentially incorporating a metallic plate beneath the SiPM for heat dissipation.

Connector side

- HSEC8-120 edge connectors compatible with RICH testbeam electronics.
- UMCC connector for the high voltage bias.
- TPC: test pulse injection circuit close to the connector to emulate a short trace.
- 2-header pin for PT1000 readout.
- Mounting holes at the edges for mechanical purposes .

Outlook

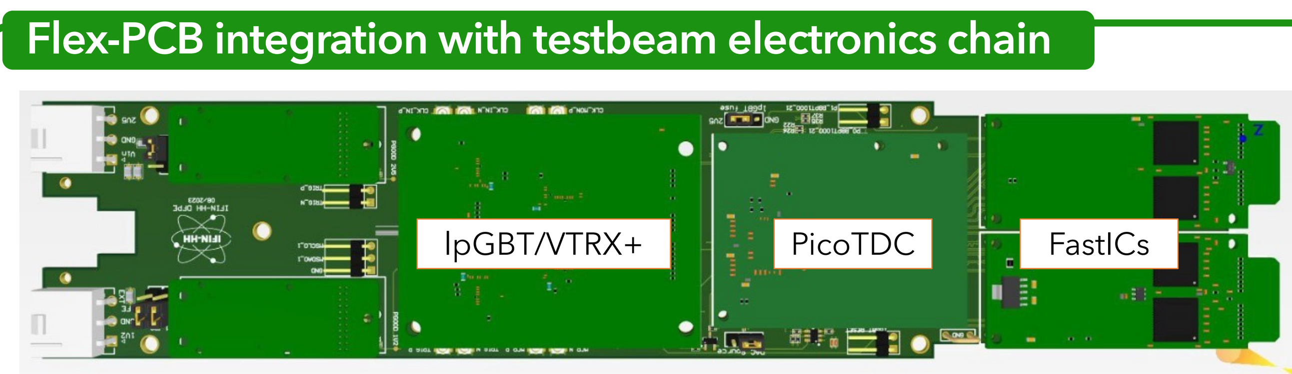
Lab testing and measurements

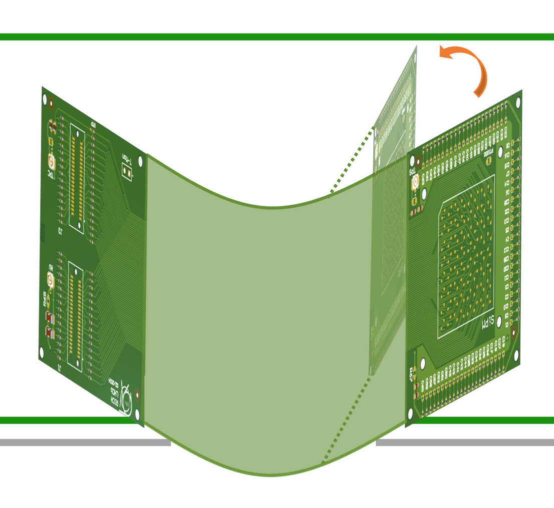
- **Test pulse injection** measurements will be conducted to study the difference between long and short traces on **signal integrity**.
- Dark current and dark count rate (DCR) studies of the SiPM.
- Measurements using a **picosecond pulsed laser** setup will include coupling the board with the RICH testbeam electronics chain (FastIC+picoTDC-based readout) and will involve:
  - SiPM integration with FE;
  - Signal integrity and crosstalk study;
  - **Time resolution**.
- Same measurements will be repeated in a **refrigeration chamber**, with controlled temperature and cooling (down to -20°C).
- Integration of the board in the **testbeam setup** at the CERN SPS facility to test beam effects on the flexible PCB technology and on the high-density long traces.

Cryostat measurements

- The cryostat demonstrator will be used to investigate critical questions regarding the behaviour of the **SiPM at cryogenic temperatures**:
  - **Sensor coupling** to the cold volume;
  - Effect of high-density long traces on the **analogue signal integrity**.
  - Operation of the front-end in vacuum and in vicinity of cold block.
  - **Heat losses** and thermal distribution.
  - **SiPM DCR** behaviour and performance, focusing on **time resolution**.
- Initially, the cryostat will be integrated into a **laser setup**, and then it will be installed in the CERN SPS facility for **beam tests**.

Flex-PCB integration with testbeam electronics chain





References

[1] CERN-LHCC-2021-012, LHCB-TDR-023.
[2] CERN-LHCC-2023-005, LHCB-TDC-024.
[3] Gundaker et al., Physics in Medicine & Biology, 2020.
[4] Acerbi et al., IEEE Transactions on Electron Devices, 2017.
[5] CERN-EP-RDET-2024-001
[6] Hamamatsu Photonics, S13361-3050 series, Cat. No. KAPD1054E06, Dec. 2023.